MEC1609/MEC1609i

Mixed Signal Mobile Embedded Flash ARC EC BC-Link/ VLPC Base Component

Product Features

- 3.3V Operation
- ACPI Compliant
- LPC Interface
  - LPC I/O and Trusted Cycles Decoded
- VTR (standby) and VBAT (Power Planes)
  - Low Standby Current in Sleep Mode
- Configuration Register Set
  - Compatible with ISA Plug-and-Play Standard
  - EC-Programmable Base Address
- ARC-625D Embedded Controller (EC)
  - 16 KB Single Cycle 32-bit Wide Dual-ported SRAM, Accessible as Closely Coupled Data Memory and Instruction Memory
  - 2 KB Instruction Cache and AHB Memory-mapped SPI Flash Read Controller
  - 32 x 32 x 64 Fast Multiply
  - Divide Assist and Saturation Arithmetic
  - Maskable Interrupt Aggregator/Accelerator Interface
  - Maskable Hardware Wake-Up Events
  - Sleep mode
  - JTAG Debug Port, Includes JTAG Master
  - MCU Serial Debug Port
  - 8-Channel DMA Interface Supports SMBus Controllers and EC/Host GP-SPI Controllers
- Embedded Flash
  - 192 KB user space + 2kB info block, 32-bit Access, 35ns Access Time, 1 K Cycles Endurance
  - Programmable by LPC, EC and JTAG Interfaces
  - Flash Security Enhancements
    - 4K Boot Block Protection
    - Direct JTAG and Direct LPC-protected (2) Pages at or Near Top of Memory for Password Protection
- Legacy Support
  - Fast GATEA20 & Fast CPU_RESET
- System to EC Message Interface
  - 8042 Style Host Interface
  - Embedded Memory Interface
    - Host Serial or Parallel IRQ Source
    - Provides Two Windows to On-Chip SRAM for Host Access
    - Two Register Mailbox Command Interface
    - Host Access of Virtual Registers Without EC Intervention
  - Mailbox Registers Interface
    - Thirty-two 8-Bit Scratch Registers
    - Two Register Mailbox Command Interface
    - Two Register SMI Source Interface
  - ACPI Embedded Controller Interface
    - Four Instances
    - 1 or 4 Byte Data transfer capable
  - ACPI Power Management Interface
    - SCI Event-Generating Functions
- Battery Backed Resources
  - Power-Fail Status Register
  - 32 KHz Clock Generator
  - Week Alarm Timer Interface with Programmable Wake-up from 1ms to 45 Days
  - VBAT-Powered Control Interface
  - VBAT-Backed 64 Byte Memory
- Three EC-based SMBus 2.0 Host Controllers
  - Allows Master or Dual Slave Operation
  - Controllers are Fully Operational on Standby Power
  - DMA-driven I^2C Network Layer Hardware
  - I^2C Datalink Compatibility Mode
  - Multi-Master Capable
  - Supports Clock Stretching
  - Programmable Bus Speeds
  - 400 KHz Capable
  - Hardware Bus Access “Fairness” Interface
  - SMBus Time-outs Interface
  - 8 x 3 x 3 Port Multiplexing
- PECI Interface 2.0
- 18 x 8 Interrupt Capable Multiplexed Keyboard Scan Matrix
- Three independent Hardware Driven PS/2 Ports
  - Fully functional on Main and/or Suspend Power
  - PS/2 Edge Wake Capable
- 115 General Purpose I/O Pins
  - 8 GPIO Pass-Through Port (GPTP)

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- 3-pin LED Interface
  - Programmable Blink Rates
  - Breathing LED Output
  - Operational in EC Sleep State
- Programmable 16-bit Counter/Timer Interface
  - Four Wake-capable 16-bit Auto-reloading Counter/Timer Instances
  - Four Operating Modes per Instance: Timer, One-shot, Event and Measurement.
  - 4 External Inputs, 4 External Outputs
- Hibernation Timer Interface
  - Two 32.768 KHz Driven Timers
  - Programmable Wake-up from 0.5ms to 128 Minutes
- System Watch Dog Timer (WDT)
- Input Capture and Compare Timer
  - 32-bit Free-running timer
  - Six 32-bit Capture Registers
  - Two 32-bit Compare Registers
  - Capture, Compare and Overflow Interrupts
- Microchip's Multipoint VLPC™ Serial Interconnect Bus Master
  - Forwards LPC transactions to VLPC peripherals
  - Forwards ARC transactions to VLPC peripherals
- BC-Link™ Interconnection Bus
  - Three High Speed and one Low Speed Bus Masters Controllers
- Two General Purpose Serial Peripheral Interface Controllers (ECGP-SPI)
  - One 3-pin EC-driven Full Duplex Serial Communication Interface
  - One 4-pin EC/Host-driven Full Duplex Serial Communication Interface to SPI Flash Interface
  - Flexible Clock Rates
  - SPI Burst Capable
- SPI Flash Read Controller
  - 4 MB AHB Memory-Mapped address space
  - Supports 2 KB EC Instruction Cache
- FAN Support
  - 8 Programmable Pulse-Width Modulator Outputs
    - Multiple Clock Rates
    - 16-Bit 'On' & 16-Bit 'Off' Counters
  - Four Fan Tachometer Inputs
  - 6 x 2 Capture/Compare Timer Interface
- ADC Interface
  - 10-bit Conversion in 10µs
  - 16 Channels
  - Integral Non-Linearity of ±0.5 LSB; Differential Non-Linearity of ±0.5 LSB
- Two Pin Debug Port with Standard 16C550A Register Interface
  - Accessible from Host and EC
  - Programmable Input/output Pin Polarity Inversion
  - Programmable Main Power or Standby Power Functionality
  - Standard Baud Rates to 115.2 Kbps, Custom Baud Rates to 2 Mbps
- Resistor/Capacitor Identification Detection (RC_ID)
  - Single Pin Interface to External Inexpensive RC Circuit
  - Replacement for Multiple GPIO's
  - Provides 8 Quantized States on One Pin
- Integrated Standby Power Reset Generator
- Clock Generator
  - 32.768 KHz-input Clock
  - operational on Suspend Power
  - Programmable Clock Power Management Control & Distribution
  - 64.52 MHz ±2% Accuracy
- Packages
  - 144 Pin LFBGA RoHS Compliant package
  - 144 Pin TFBGA RoHS Compliant package
- Operating Temperature
  - The MEC1609 supports the commercial temperature range of 0^{o} C to $+70^{o}$ C
  - The MEC1609i supports the industrial temperature range of -40^{o} C to $+85^{o}$ C

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Description

The MEC1609/MEC1609i is the mixed signal base component of a multi-device advanced I/O controller architecture. The MEC1609/MEC1609i incorporates a high-performance 32-bit ARC 625 embedded microcontroller with a 192 Kilobyte embedded Flash subsystem, 16 Kilobytes of SRAM and 2 Kilobytes of instruction cache with an AHB memory-mapped SPI Flash Read Controller. The MEC1609 communicates with the system host using the Intel® Low Pin Count bus.

There are two distinct protocols that provide communication between the MEC1609/MEC1609i base component and companion components: BC-Link™ and VLPC™. BC-Link™ in the MEC1609/MEC1609i can access up to four companion components. The BC-Link™ protocol is peer-to-peer providing communication between the MEC1609/MEC1609i embedded controller and registers located in a companion. VLPC™ is a multi-drop protocol that matches the MEC1609/MEC1609i with up to three untrusted companion components and one trusted companion component. The MEC1609/MEC1609i accepts LPC Host (ICH/PCH) transactions targeting blocks internal to the MEC1609/MEC1609i and blocks physically located in VLPC™ companions. The ARC 625 embedded microcontroller can also access blocks that are physically located in VLPC™ companion components.

The MEC1609/MEC1609i is directly powered by two separate suspend supply planes (VBAT and VTR) and senses a third runtime power plane (VCC) to provide “instant on” and system power management functions. The MEC1609/MEC1609i also contains an integrated VTR Reset Interface and a system Power Management Interface that supports low-power states and can drive state changes as a result of hardware wake events as defined by the MEC1609/MEC1609i Wake Interface.

The MEC1609/MEC1609i defines a software development system interface that includes an MCU Serial Debug Port, a two pin serial debug port with a 16C550A register interface that is accessible to the EC or to the LPC host and can operate up to 2 MB/s, a flexible Flash programming interface and a JTAG interface. The EC can also drive the JTAG interface as a master.

A top-level block diagram of the MEC1609/MEC1609i is shown in FIGURE 1: MEC1609/MEC1609i Top-Level Block Diagram on page 5. An example of system level connection is shown in FIGURE 2: Example of MEC1609/MEC1609i’s Connections to System Components on page 6.

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BLOCK DIAGRAM

FIGURE 1: MEC1609/MEC1609i TOP-LEVEL BLOCK DIAGRAM

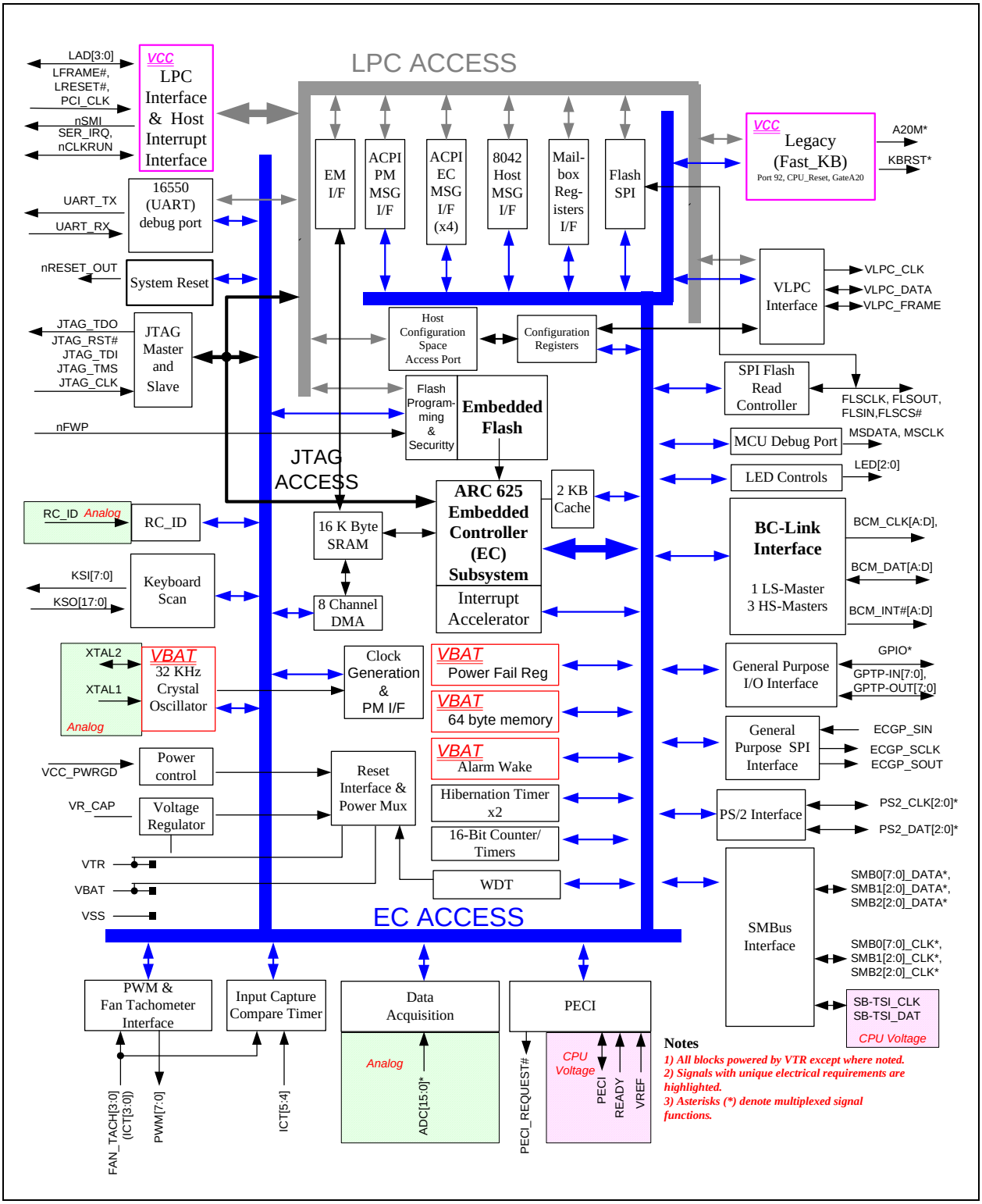
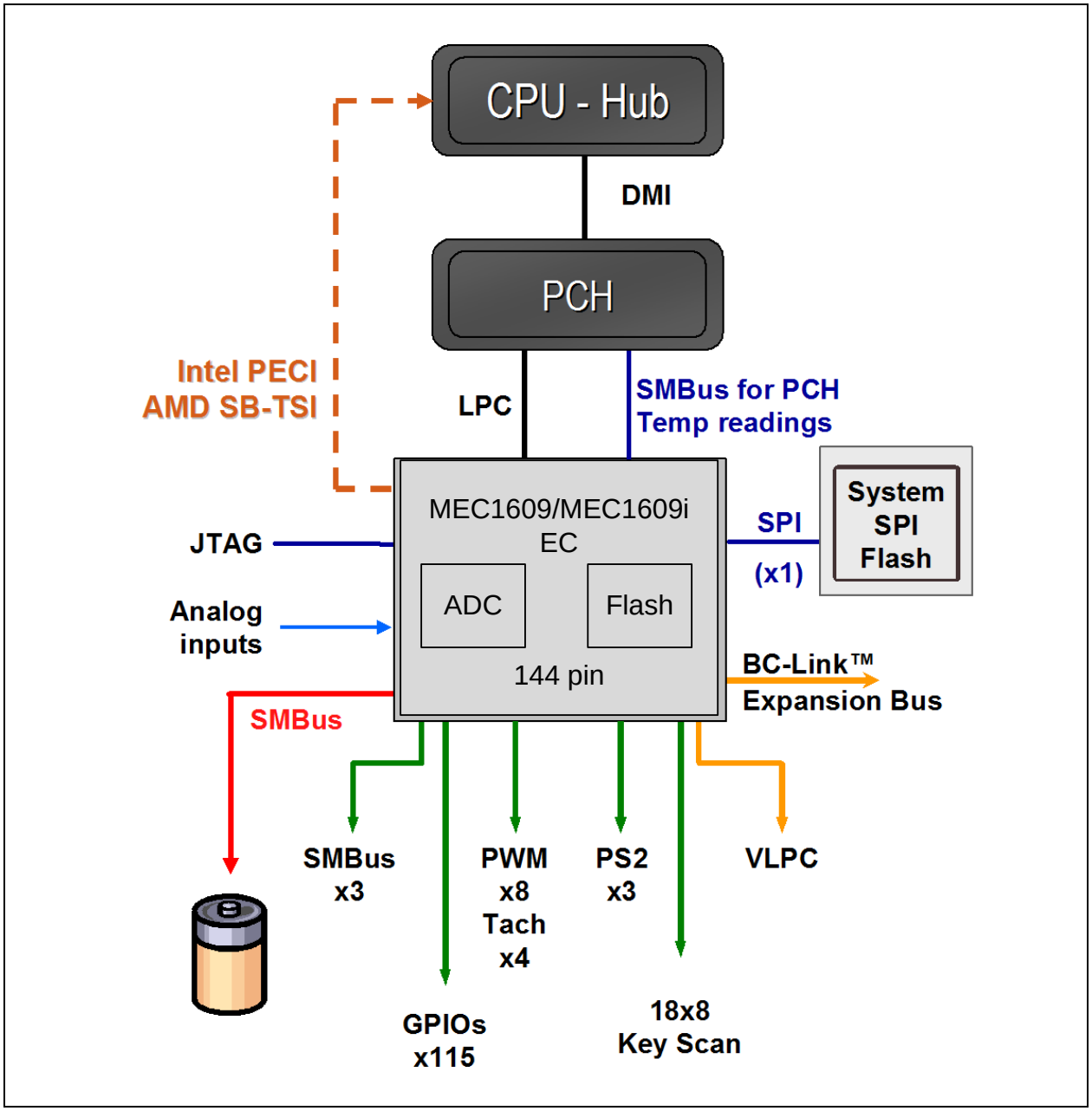


FIGURE 2: EXAMPLE OF MEC1609/MEC1609i'S CONNECTIONS TO SYSTEM COMPONENTS



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PACKAGE OUTLINES

Note: For the most current package drawings, see the Microchip Packaging Specification at http://www.microchip.com/packaging.

FIGURE 3: 144-PIN LFBGA 10X10X0.8 MM PACKAGE OUTLINE (1.4 MM HEIGHT)

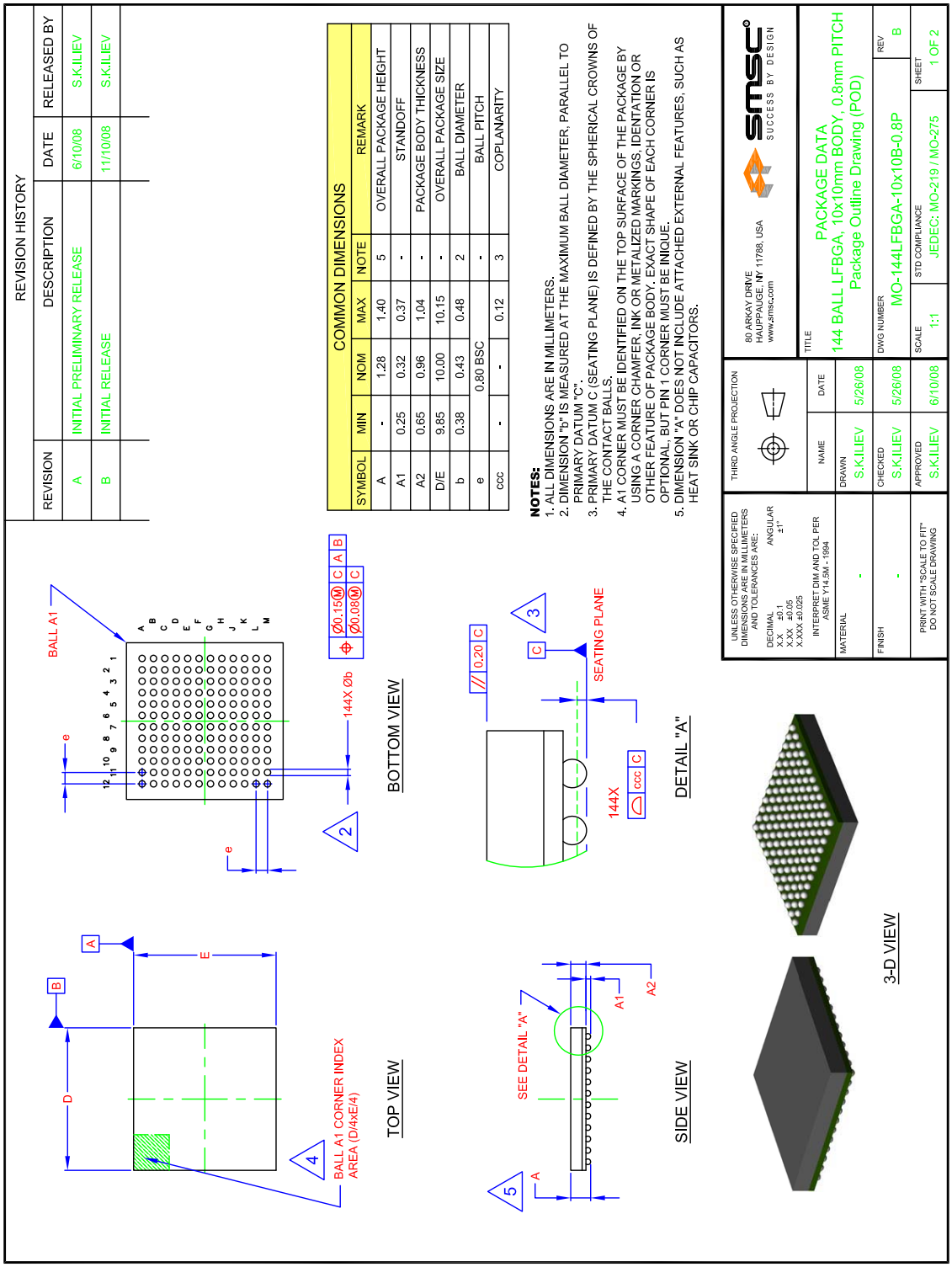
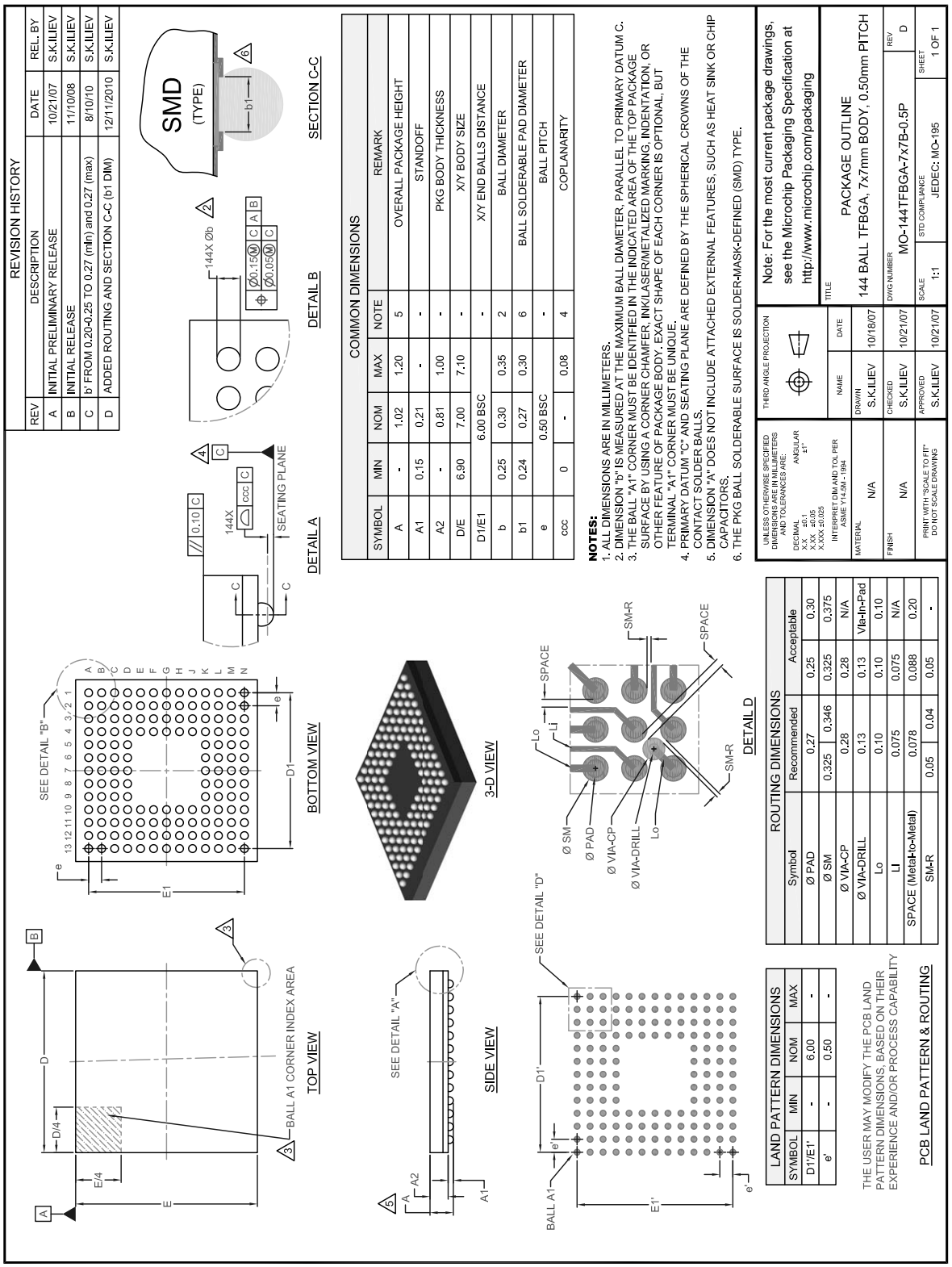


FIGURE 4: 144-PIN TFBGA 7X7X0.5 MM PACKAGE OUTLINE (1.2 MM HEIGHT)



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APPENDIX A: PRODUCT BRIEF REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00001769A (06-03-14)	Document Release	

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PART NO.	[X]	-	XXX	-	[X](1)
Device	Temperature Range		Package		Tape and Reel Option

Device:	MEC1609, MEC1609i	
Temperature Range:	Blank = 0°C to +70°C i = -40°C to +85°C	(Extended Commercial) (Industrial)
Package:	PZV = 144-pin TFBGA PZP = 144-pin LFBGA	
Tape and Reel Option:	Blank = Standard packaging (tray) TR = Tape and Reel(1)	

Examples:

a) MEC1609-PZV
144-pin TFBGA (7mm x 7mm, 0.5 pitch)
RoHS Compliant package

b) MEC1609-PZP
144-pin TFBGA (10mm x 10mm, 0.8 pitch)
RoHS Compliant package

c) MEC1609i-PZV
Industrial temperature,
144-pin TFBGA (7mm x 7mm, 0.5 pitch)
RoHS Compliant package

d) MEC1609i-PZP
Industrial temperature,
144-pin TFBGA (10mm x 10mm, 0.8 pitch)
RoHS Compliant package

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