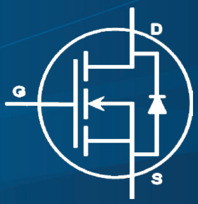
EPC2023 – Enhancement Mode Power Transistor

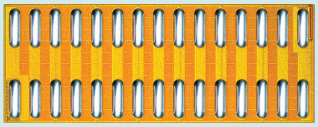
V_{DS} , 30 V
$R_{DS(on)}$, 1.45 mΩ
I_D , 90 A



Gallium Nitride is grown on Silicon Wafers and processed using standard CMOS equipment leveraging the infrastructure that has been developed over the last 60 years. GaN's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Maximum Ratings

V_{DS}	Drain-to-Source Voltage (Continuous)	30	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150˚C)	36	
I_D	Continuous (T_A = 25˚C, $R_{θJA}$= 6˚C/W)	90	A
	Pulsed (25˚C, T_{PULSE} = 300 µs)	590	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	˚C
T_{STG}	Storage Temperature	-40 to 150	



EPC2023 eGaN® FETs are supplied only in passivated die form with solder bumps.
Die Size: 6.05 mm x 2.3 mm

Applications:

- High Frequency DC-DC Conversion
- Point-of-Load (POL) Converters
- Motor Drive
- Industrial Automation

www.epc-co.com/epc/Products/eGaNFETs/EPC2023.aspx

Static Characteristics (T_J= 25˚C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 1.3 mA	30			V
I_{DSS}	Drain Source Leakage	V_{DS} = 24 V, V_{GS} = 0 V		0.1	1	mA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		1	9	mA
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		0.1	1	mA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 20 mA	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 5 V, I_D = 40 A		1.15	1.45	mΩ
V_{SD}	Source-to-Drain Forward Voltage	I_S = 0.5 A, V_{GS} = 0 V		1.5		V

All measurements were done with substrate connected to source.

Thermal Characteristics

		TYP	UNIT
$R_{θJC}$	Thermal Resistance, Junction to Case	0.4	˚C/W
$R_{θJB}$	Thermal Resistance, Junction to Board	1.1	˚C/W
$R_{θJA}$	Thermal Resistance, Junction to Ambient (Note 1)	42	˚C/W

Note 1: $R_{θJA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Dynamic Characteristics (T_J= 25˚C unless otherwise stated)						
PARAMETER		**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
C_{ISS}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V		2150	2600	pF
C_{RSS}	Reverse Transfer Capacitance			100		
C_{OSS}	Output Capacitance			1530	2300	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	V_{DS} = 0 to 15 V, V_{GS} = 0 V		1850		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			2020		
R_G	Gate Resistance			0.3		Ω
Q_G	Total Gate Charge	V_{DS} = 15 V, V_{GS} = 5 V, I_D= 40 A		19	25	nC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 15 V, I_D = 40 A		5.7		
Q_{GD}	Gate-to-Drain Charge			3.2		
$Q_{G(TH)}$	Gate Charge at Threshold			4		
Q_{OSS}	Output Charge	V_{DS} = 15 V, V_{GS} = 0 V		30	45	
Q_{RR}	Source-to-Drain Recovery Charge			0		

Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

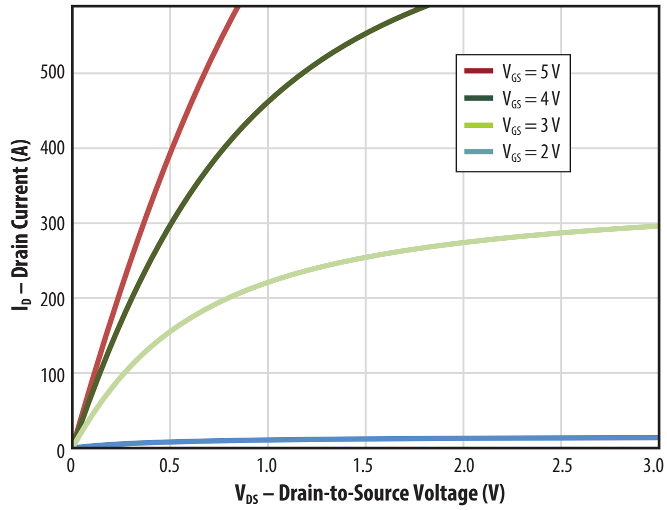


Figure 2: Transfer Characteristics

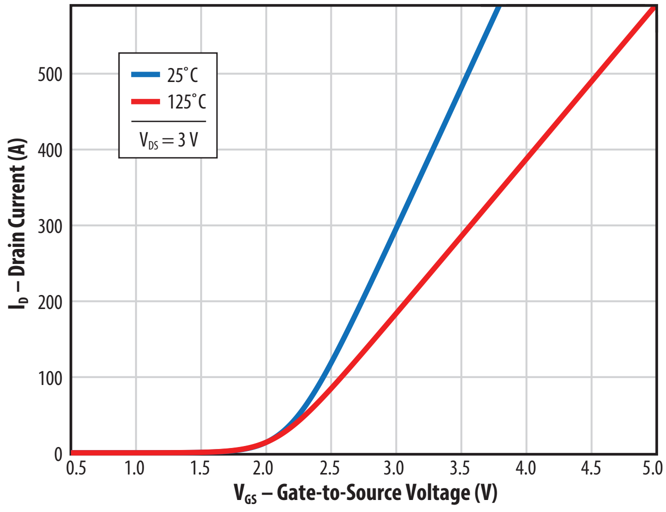


Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

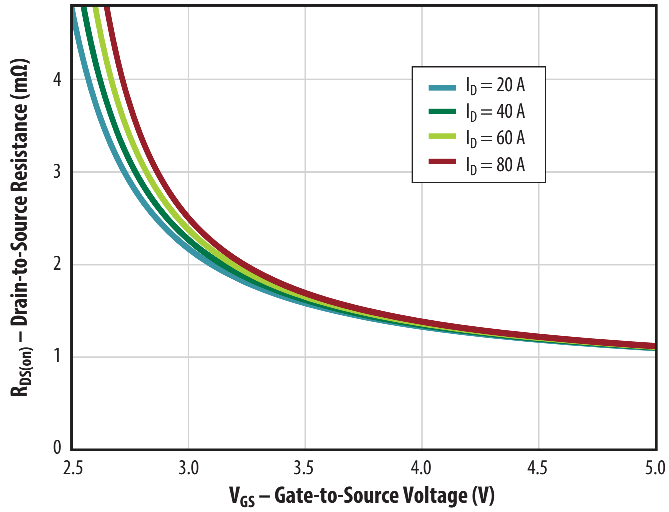


Figure 4: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

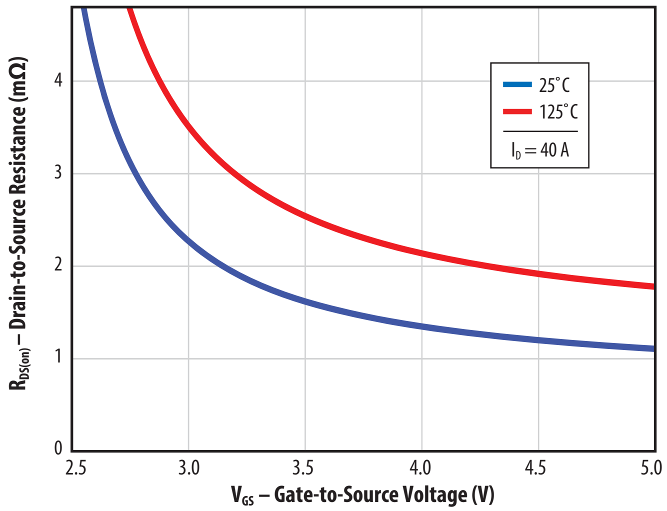


Figure 5a: Capacitance (Linear Scale)

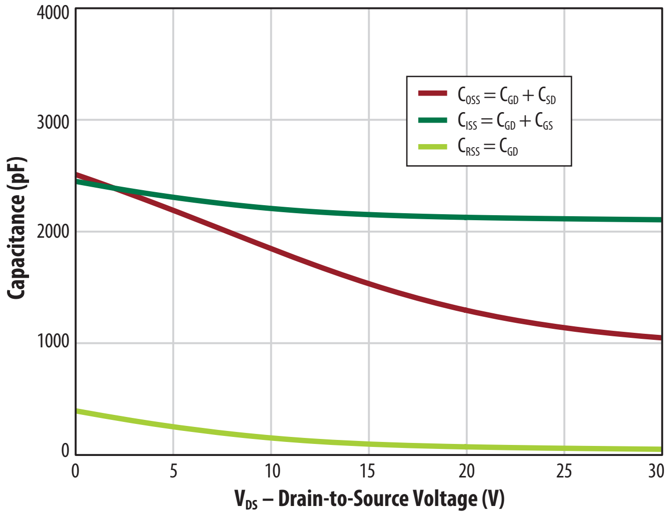


Figure 5b: Capacitance (Log Scale)

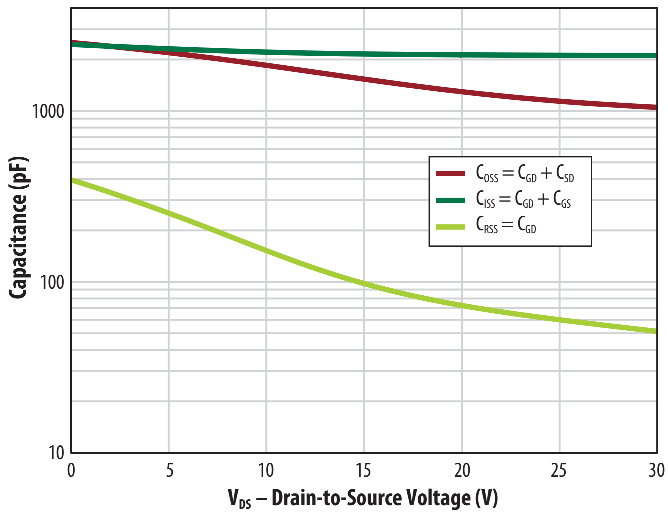


Figure 6: Output Charge and C_{OSS} Stored Energy

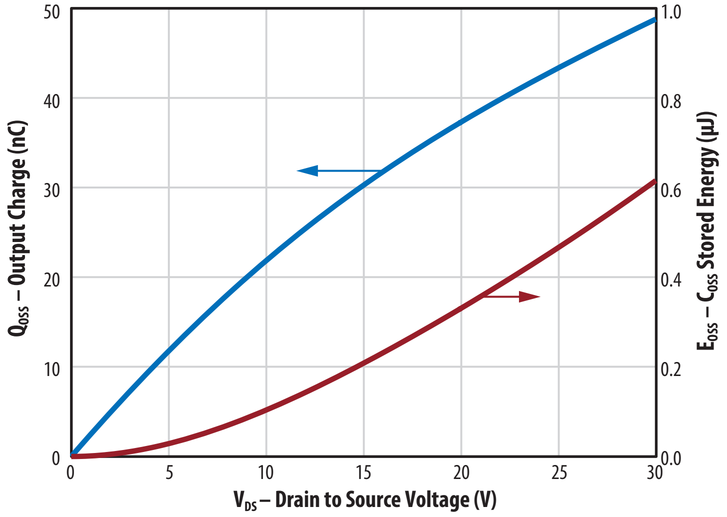


Figure 7: Gate Charge

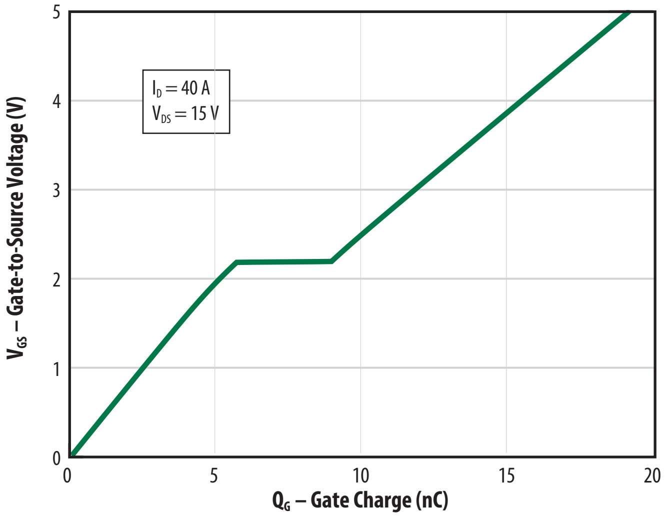


Figure 8: Reverse Drain-Source Characteristics

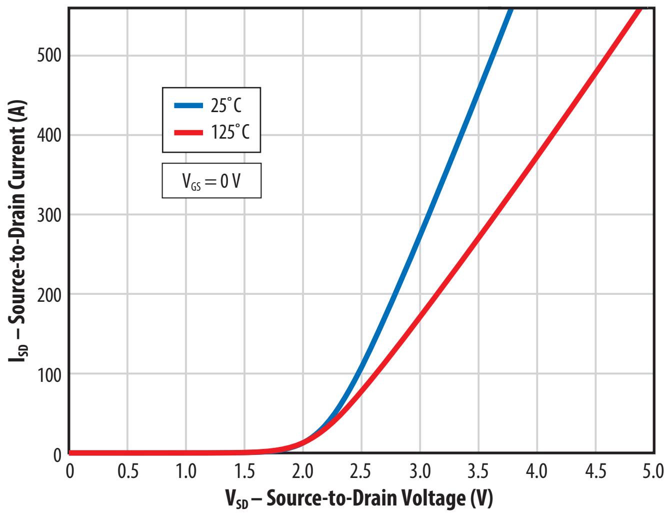
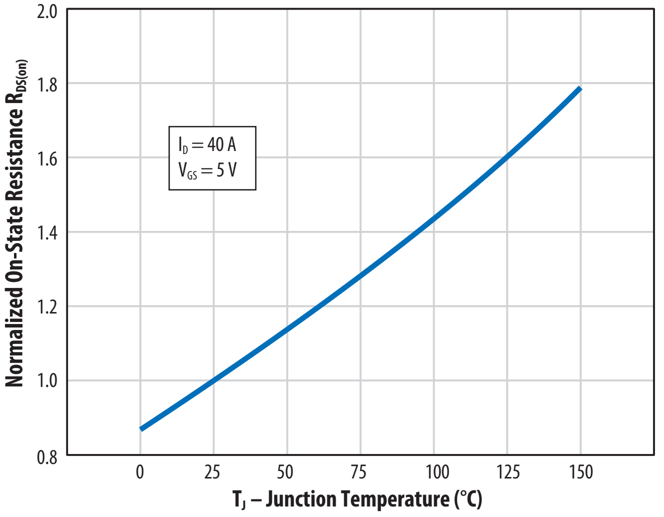


Figure 9: Normalized On-State Resistance vs. Temperature



All measurements were done with substrate shortened to source.

Figure 10: Normalized Threshold Voltage vs. Temperature

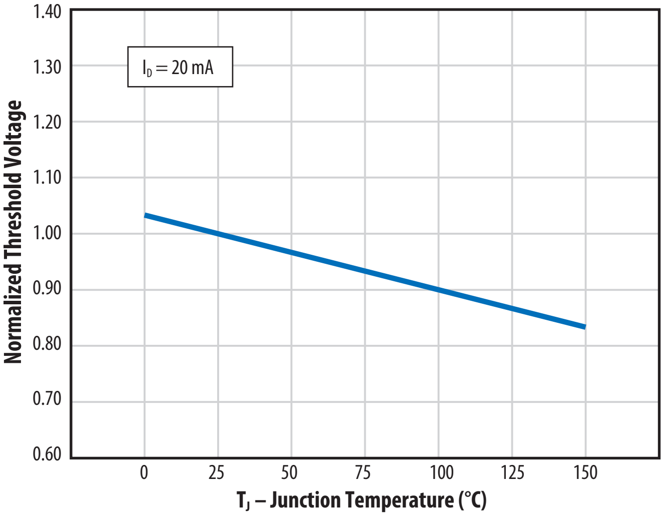


Figure 11: Safe Operating Area

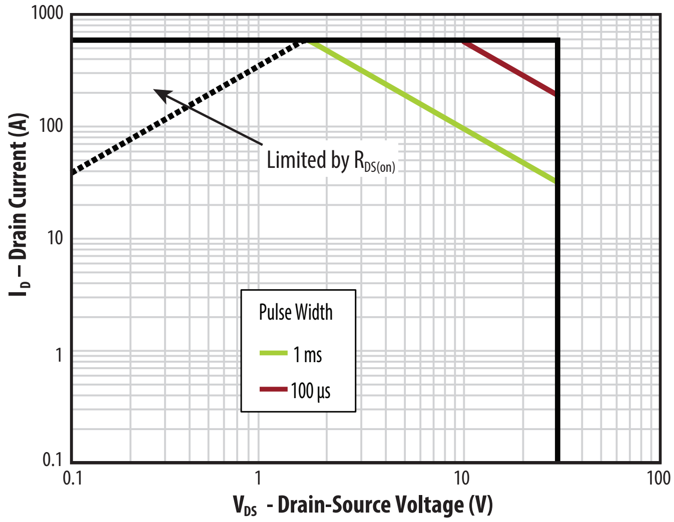
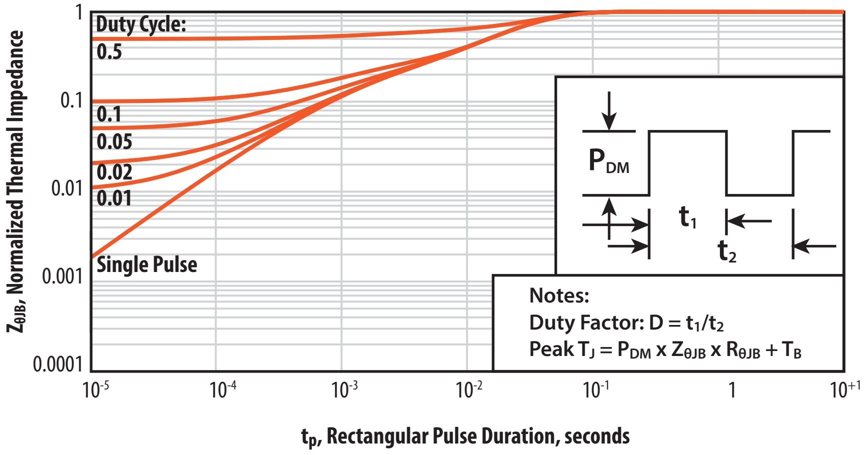


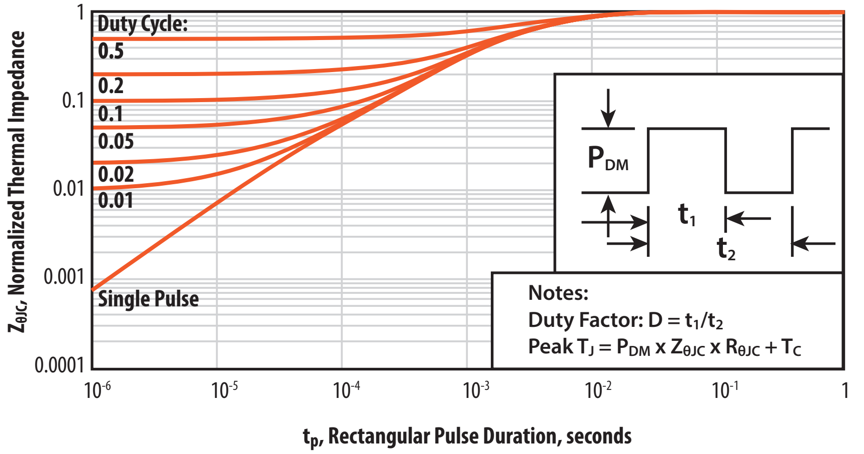
Figure 12: Transient Thermal Response Curves

Junction-to-Board



Notes:
Duty Factor: $D = t_1/t_2$
Peak $T_J = P_{DM} \times Z_{\theta JB} \times R_{\theta JB} + T_B$

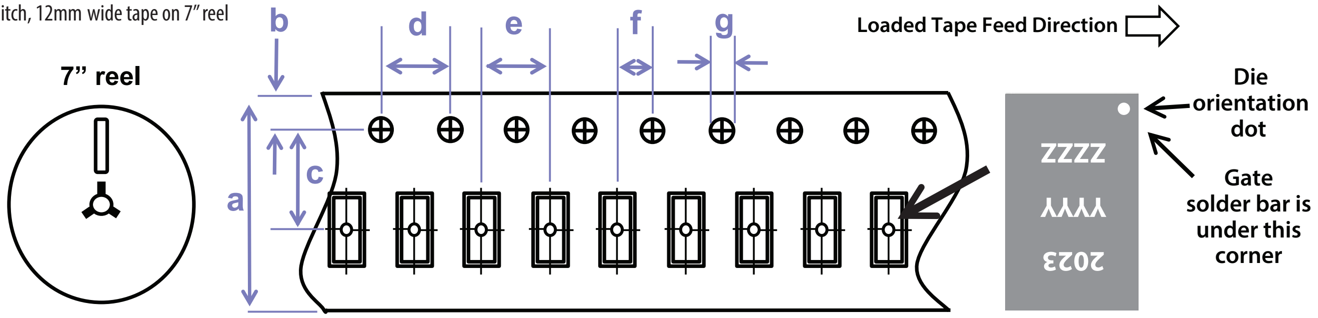
Junction-to-Case



Notes:
Duty Factor: $D = t_1/t_2$
Peak $T_J = P_{DM} \times Z_{\theta JC} \times R_{\theta JC} + T_C$

TAPE AND REEL CONFIGURATION

4mm pitch, 12mm wide tape on 7" reel

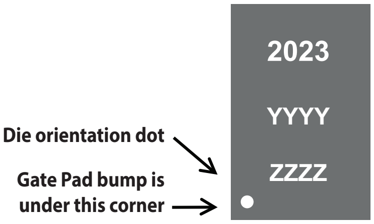


Die is placed into pocket solder bar side down (face side down)

	EPC2023 (note 1)		
Dimension (mm)	**target**	**min**	**max**
a	12.00	11.70	12.30
b	1.75	1.65	1.85
c (see note)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.50	1.50	1.60

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

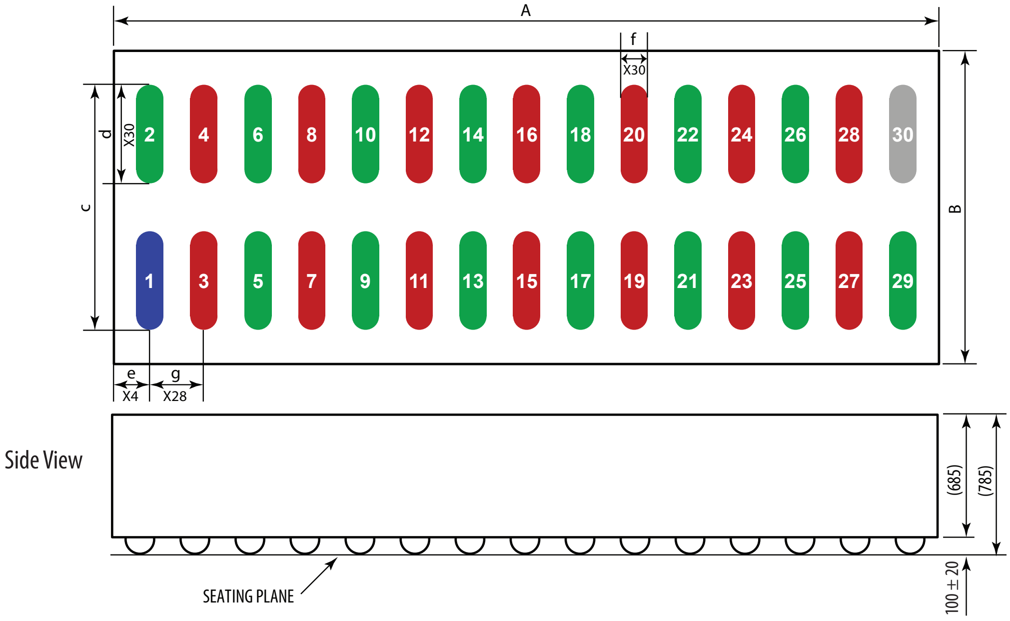
DIE MARKINGS



Part Number	Laser Marking		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2023	2023	YYYY	ZZZZ

DIE OUTLINE

Solder Bump View



DIM	Micrometers		
	MIN	Nominal	MAX
A	6020	6050	6080
B	2270	2300	2330
c	2047	2050	2053
d	717	720	723
e	210	225	240
f	195	200	205
g	400	400	400

Pad 1 is Gate

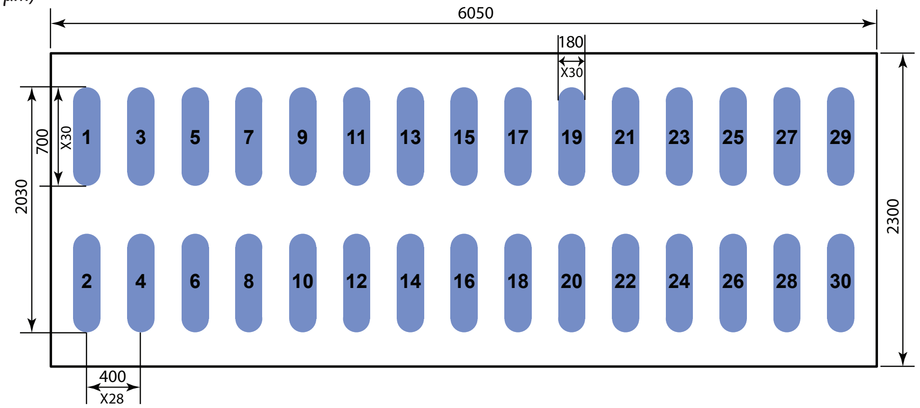
Pads 2,5,6,9,10,13,14,17,18,21,22,25,26,29 are Source

Pads 3,4,7,8,11,12,15,16,19,20,23,24,27,28 are Drain

Pad 30 is Substrate

RECOMMENDED LAND PATTERN

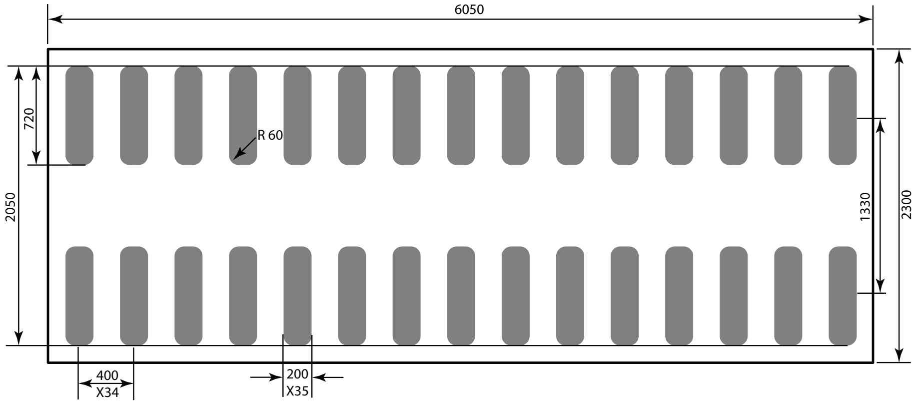
(units in µm)



Land pattern is solder mask defined
Solder mask opening is 180 µm
It is recommended to have on-Cu trace
PCB vias

RECOMMENDED STENCIL DRAWING

(units in µm)



Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 3 solder, reference 88.5% metals content.

Additional assembly resources available at http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx

U.S. Patents 8,350,294; 8,404,508; 8,431,960; 8,436,398; 8,785,974; 8,890,168; 8,969,918; 8,853,749; 8,823,012

Information subject to change without notice.
Revised August, 2017