NCP3232N

High Current Synchronous Buck Converter

The NCP3232N is a high current, high efficiency voltage−mode synchronous buck converter which operates from 4.5 V to 21 V input and generates output voltages down to 0.6 V at up to 15 A.

Features

- Wide Input Voltage Range from 4.5 V to 21 V
- 0.6 V Internal Reference Voltage
- 500 kHz Switching Frequency
- External Programmable Soft−Start
- Lossless Low−side FET Current Sensing
- Output Over−voltage Protection and Under−voltage Protection
- System Over−temperature Protection using a Thermistor or Sensor
- Hiccup Mode Operation for all Faults
- Pre−bias Start−up
- Adjustable Output Voltage
- Power Good Output
- Internal Over−temperature Protection
- These Devices are Pb−Free and are RoHS Compliant*

Typical Application

- Cellular Base Stations
- ASIC, FPGA, DSP and CPU Core and I/O Supplies
- Telecom and Network Equipment
- Server and Storage System

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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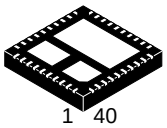
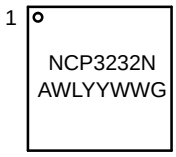


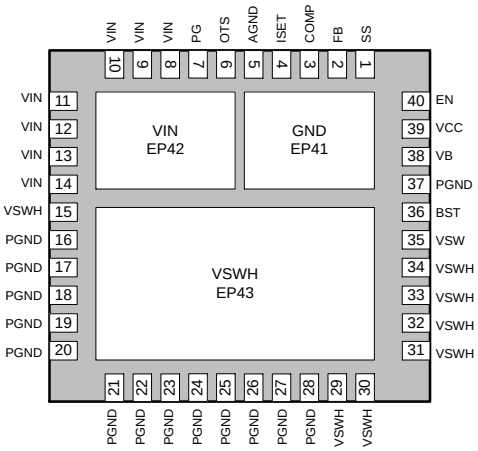
QFN40 6x6, 0.5P
CASE 485CM

MARKING DIAGRAM



A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

PIN CONNECTIONS



(TOP VIEW)

ORDERING INFORMATION

Device	Package	Shipping†
NCP3232NMNTXG	QFN−40 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

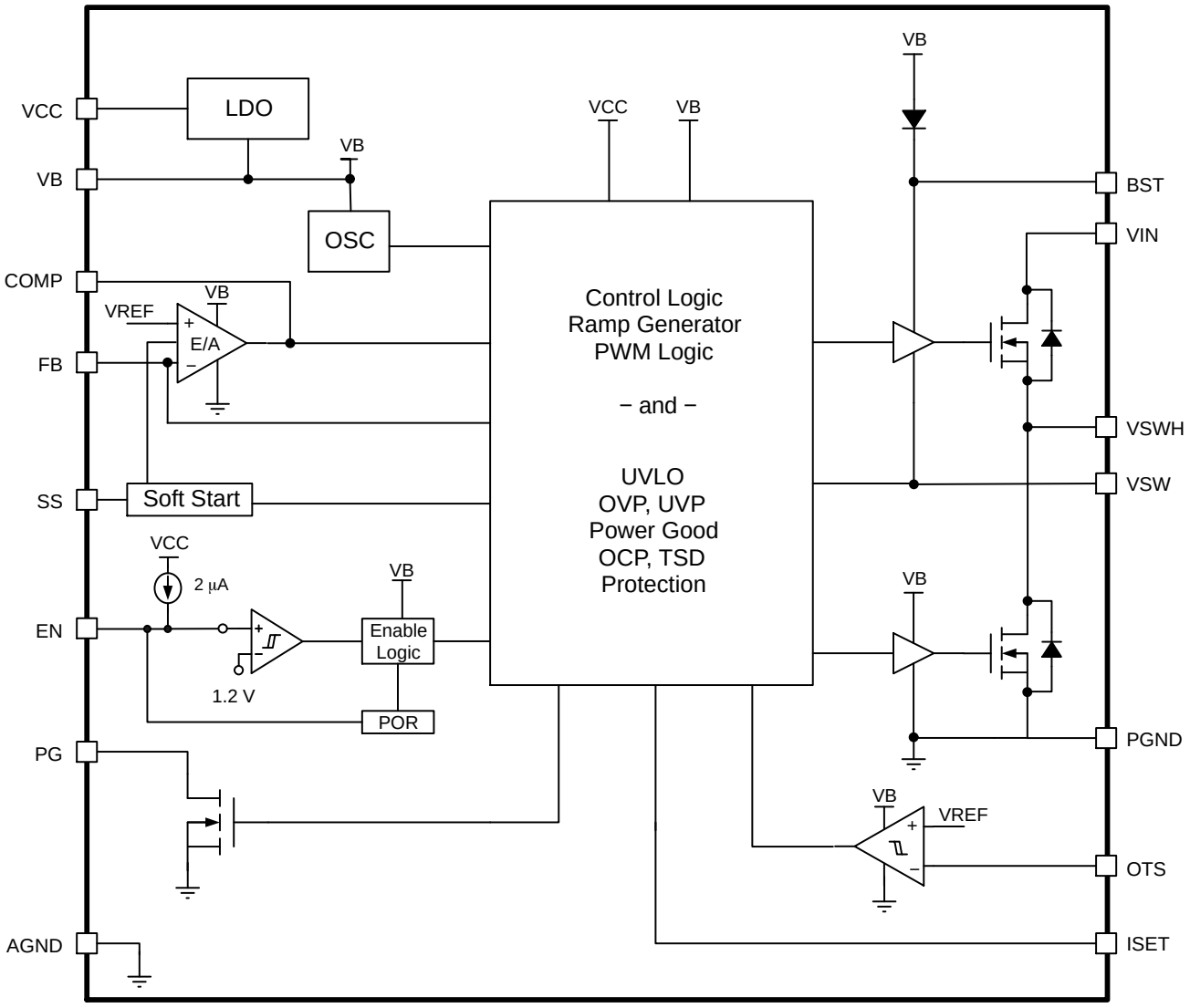


Figure 1. NCP3232N Block Diagram

PIN DESCRIPTION

Pin No.	Symbol	Description
1	SS	A capacitor from this pin to GND allows the user to adjust the soft−start ramp time.
2	FB	Output voltage feedback.
3	COMP	Output of the error amplifier.
4	ISET	A resistor from this pin to ground sets the over−current protection (OCP) threshold.
5	AGND	Analog ground.
6	OTS	Negative input of internal thermal comparator. Tie this pin to ground if not in use.
7	PG	Power good indicator of the output voltage. Open−drain output. Connect PG to VDD with an external resistor.
8−14, EP42	VIN	The VIN pin is connected to the internal power NMOS switch. The VIN pin has high di/dt edges and must be decoupled to ground close to the pin of the device.
15, 29−34, EP43	VSWH	The VSWH pin is the connection of the drain and source of the internal NMOS switches. At switch off, the inductor will drive this pin below ground as the body diode and the NMOS conducts with a high dv/dt.
16−28, 37	PGND	Ground reference and high−current return path for the bottom gate driver and low- side NMOS
35	VSW	IC connection to the switch node between the top MOSFET and bottom MOSFET. Return path of the high−side gate driver.
36	BST	Top gate driver input supply, a bootstrap capacitor connection between SWN and this pin.
38	VB	The internal LDO output and input supply for the charge pump. Connect a minimum of 4.7uF ceramic capacitor from this pin to ground.
39	VCC	Input Supply for IC. This pin must be connected to VIN.
40	EN	Logic control for enabling the switcher. An internal pull−up enables the device automatically. The EN pin can also be driven high to turn on the device, or low to turn off the device. A comparator and precision reference allow the user to implement this pin as an adjustable UVLO circuit.
EP41	GND	Exposed Pad. Connect GND to a large copper plane at ground potential to improve thermal dissipation.

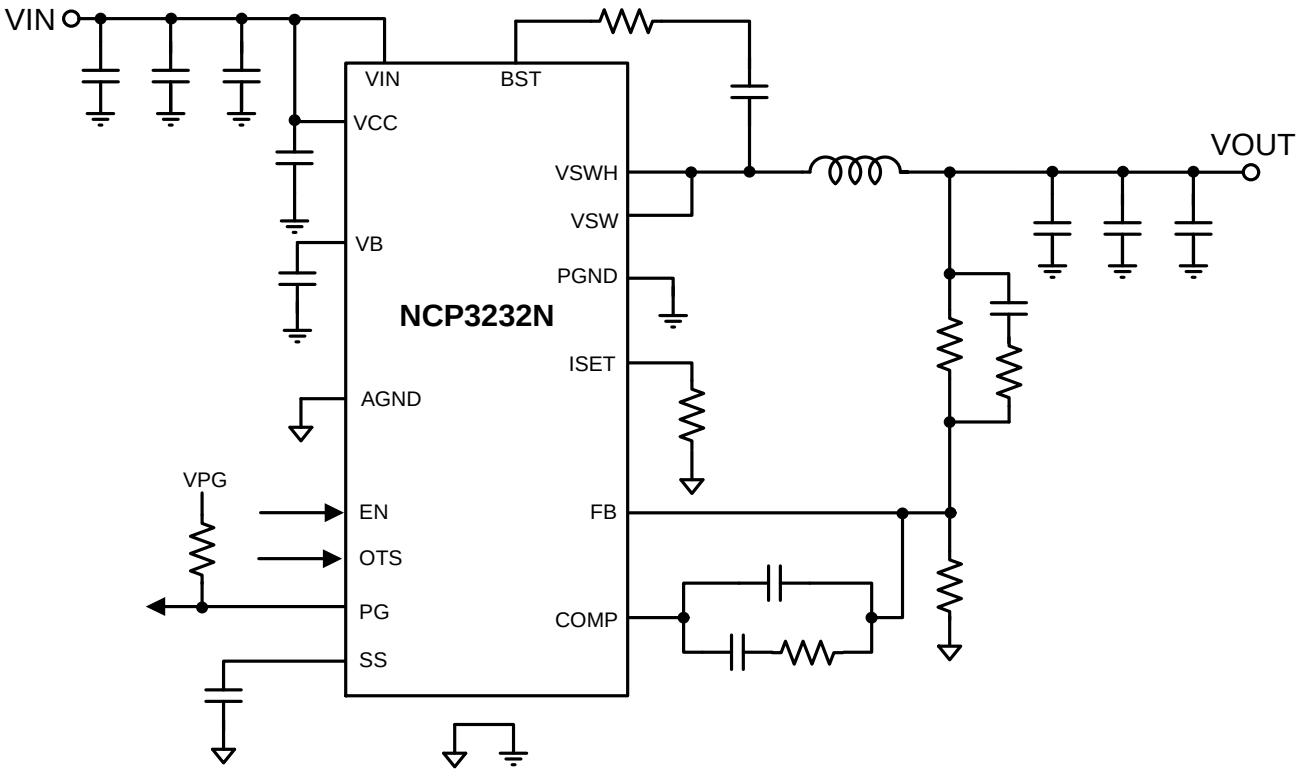


Figure 2. Typical Application Circuit

ABSOLUTE MAXIMUM RATINGS (measured vs. GND pad, unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply to GND	V_{IN}, V_{CC}	23 −0.3	V
VSW to GND	VSWH, VSW	30 −0.6 (DC) 35 (t < 50 ns) −5 (t < 100 ns)	V
BST to GND	BST	35 (DC) −0.6 (DC) 40 (t < 50 ns)	V
All other pins		6.0 −0.3	V
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Operating Junction Temperature Range	T_J	−40 to +125	°C
Maximum Junction Temperature	$T_{J(MAX)}$	+150	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Electrostatic Discharge − Human Body Model	HBM	1.0	kV
Electrostatic Discharge − Charge Device Model	CDM	2.0	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL INFORMATION

HS FET Junction-to-case thermal resistance (Note 1)	$R_{\theta JC-HS}$	1.3	°C/W
LS FET Junction-to-case thermal resistance (Note 1)	$R_{\theta JC-LS}$	0.6	°C/W
Junction-to-ambient thermal resistance	$R_{\theta JA}$	35	°C/W

1. $R_{\theta JC}$ thermal resistance is obtained by simulating a cold plate test on the exposed power pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS (−40°C < T_J < +125°C, V_{CC} = 12 V, for min/max values unless otherwise noted, T_J = +25°C for typical values)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
POWER SUPPLY						
VIN/VCC Operation Voltage	VIN/VCC		4.5		21	V
VB UVLO Threshold (Rising)			4.1	4.2	4.3	V
VB UVLO Threshold (Falling)			3.4	3.6	3.8	V
VB Output Voltage	VB	VCC = 6 V, 0 ≤ IB ≤ 40 mA	4.9	5.15	5.45	V
VB Dropout Voltage		IB = 25 mA, VCC = 4.5 V		36	110	mV
VCC Quiescent Current		EN = H, COMP = H, no switching; PG open; no switching		4.7	6.4	mA
Shutdown Supply Current		EN = 0; V_{CC} = 21 V; PG open		100	140	μA
		EN = 0;V_{CC} = 4.5 V; PG open		55	75	μA
FEEDBACK VOLTAGE						
FB Input Voltage	VFB	T_J = 25°C, 4.5 V ≤ VCC ≤ 21 V	0.597	0.6	0.603	V
		−40°C < TJ < 125°C; 4.5 V ≤ VCC ≤ 21 V	0.594	0.6	0.606	
Feedback Input Bias Current	IFB	VFB = 0.6 V			75	nA
ERROR AMPLIFIER						
Open Loop DC Gain (GBD)			60	85		dB
Open Loop Unity Gain Bandwidth	F0dB,EA			24		MHz
Open Loop Phase Margin				60		°
Slew Rate		COMP pin to GND = 10 pF		2.5		V/μ
COMP Clamp Voltage, High				3.4		V
COMP Clamp Voltage, Low				0.465		V
Output Source Current		VFB = 0 V	15			mA
Output Sink Current		VFB = 1 V	20			mA
CURRENT LIMIT						
Low−side ISET Current Source	LS_ISET	Sourced from ISET pin, before SS, T_J = 25°C	30.5	33	35.5	μA
Low−side ISET Current Source Temperature Coefficient	TC_LS_I−SET			+0.31		%/°C
Low−side OCP Switch−over Threshold		Guaranteed by design		600		mV
Low−side Fixed OCP Threshold	LS_OCPth	Guaranteed by design		300		mV
Low−side Programmable OCP Range		Guaranteed by characterization			< 600	mV
LS OCP Blanking time	LS_Tblnk	Guaranteed by design		150		ns
PWM						
Maximum duty cycle		fsw = 500 kHz, VFB = 0 V 4.5 V < VCC < 21 V		92		%
Minimum duty cycle		VCOMP < PWM Ramp Offset Voltage		0		%
Minimum GH on−time		Guaranteed by characterization		60		ns
PWM Ramp Amplitude		Guaranteed by characterization	VCC/8.6	VCC/6.6	VCC/5.6	V
PWM Ramp Offset				0.64		V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ELECTRICAL CHARACTERISTICS (−40°C < T_J < +125°C, V_{CC} = 12 V, for min/max values unless otherwise noted, T_J = +25°C for typical values)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OSCILLATOR						
Oscillator Frequency Range	fsw	fsw = 500 kHz 4.5 V < VCC < 21 V	450	500	550	kHz
Hiccup Timer	thiccup	tss < 1 ms, fsw = 500 kHz		4		ms
		tss > 1 ms, fsw = 500 kHz		4xtss		ms
ENABLE INPUT (EN)						
EN Input Operating Range					5.5	V
Enable Threshold Voltage		VEN rising	1.11	1.2	1.29	V
Enable Hysteresis		VEN falling		144		mV
Deep Disable Threshold			0.7	0.78	0.9	V
Enable Pull−up Current				2		μA
SOFTSTART INPUT (SS)						
SS Start Delay	tSSD			1.33		ms
SS End Threshold	SSEND			0.6		V
SS Source Current	ISS		2.15	2.5	2.8	μA
VOLTAGE MONITOR						
Power Good Sink Current		PG = 0.15 V	10	20	30	mA
Output Overvoltage Rising			665	675	685	mV
Overvoltage Fault Blanking Time		Guaranteed by design		20		μs
Output Under−Voltage Trip Threshold			500	525	550	mV
Under−voltage Protection Blanking Time				20		μs
UVP Enable Delay				t_{SS}		s
POWER STAGE						
High−side on Resistance	RDSONH	VIN/VCC = 5 V, ID = 2 A		6.5	10	mΩ
Low−side on Resistance	RDSONL	VIN/VCC = 5 V, ID = 2 A		2.9	5.2	mΩ
VFBOOT		IBOOT = 2 mA		0.28		V
THERMAL MONITOR (OTS)						
OTS comparator reference voltage (Rising Threshold)			0.59	0.6	0.61	V
OTS comparator reference voltage (Falling Hysteresis)				50		mV
THERMAL SHUTDOWN						
Thermal Shutdown Threshold		Guaranteed by characterization		150		°C
Thermal Shutdown Hysteresis		Guaranteed by characterization		25		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

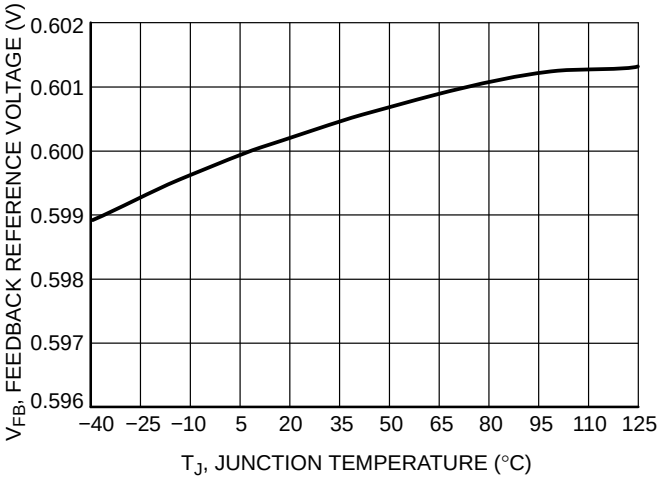


Figure 3. Reference Voltage vs. Temperature

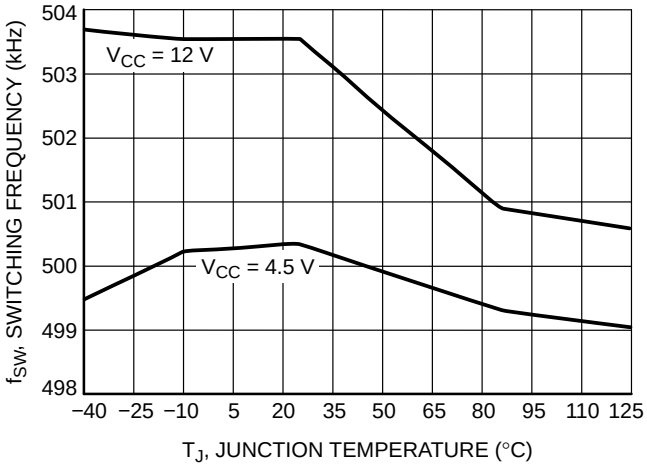


Figure 4. Switching Frequency vs. Temperature

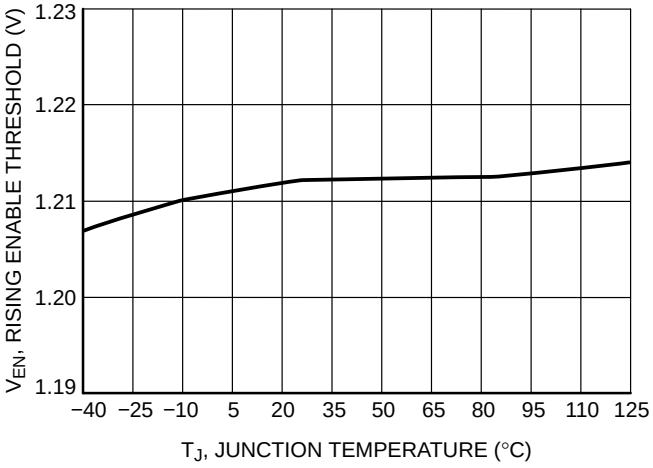


Figure 5. Rising Enable Threshold vs. Temperature

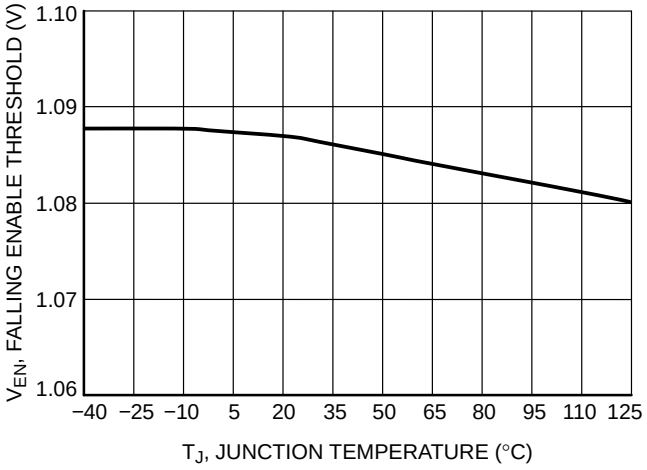


Figure 6. Falling Enable Threshold vs. Temperature

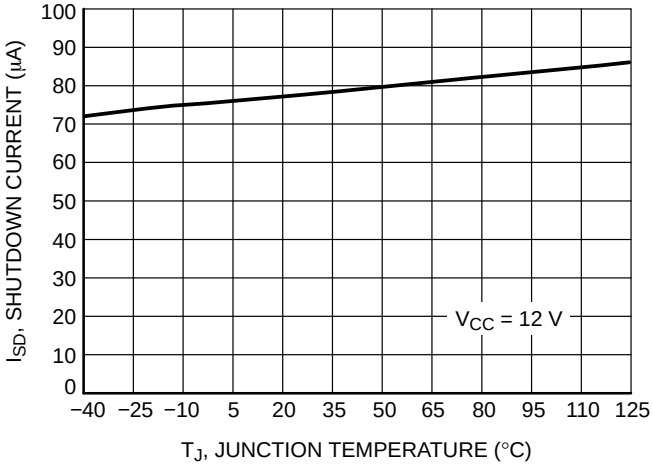


Figure 7. Shutdown Current vs. Temperature

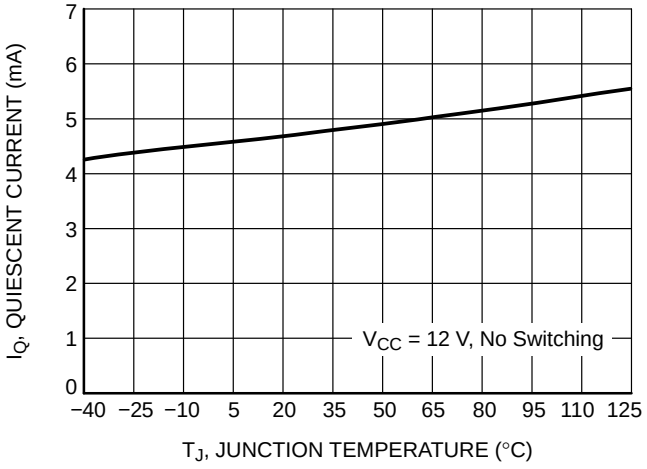


Figure 8. Quiescent Current vs. Temperature

TYPICAL CHARACTERISTICS

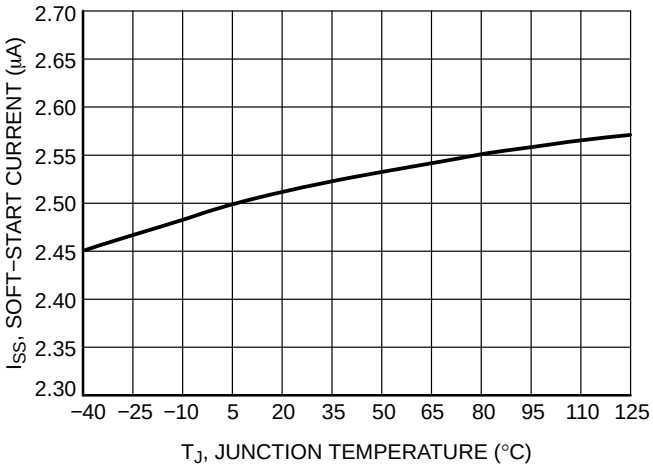


Figure 9. Soft−start Current vs. Temperature

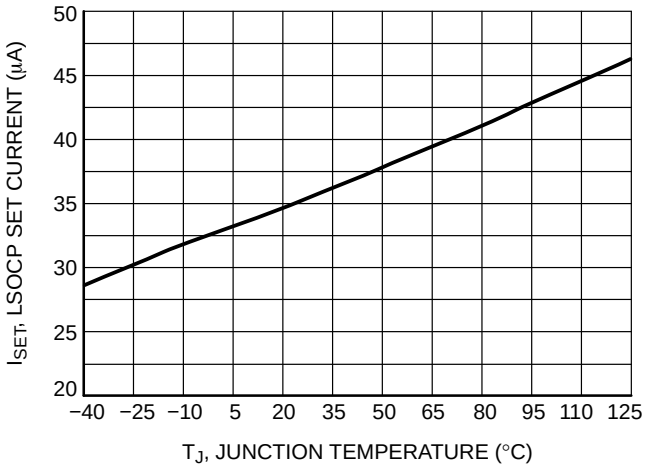


Figure 10. ISET Current vs. Temperature

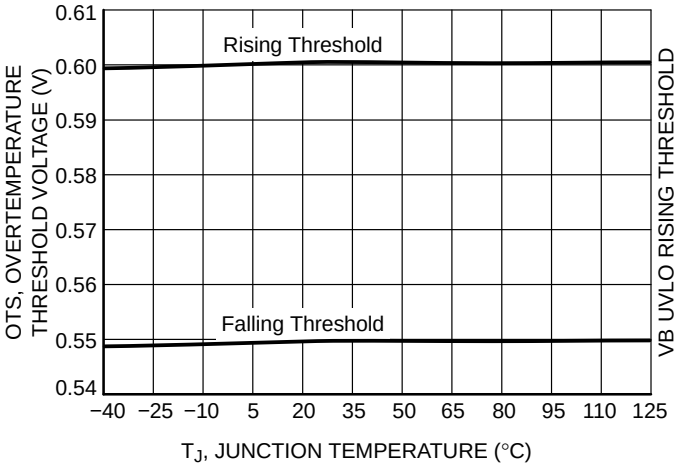


Figure 11. OTS Threshold vs. Temperature

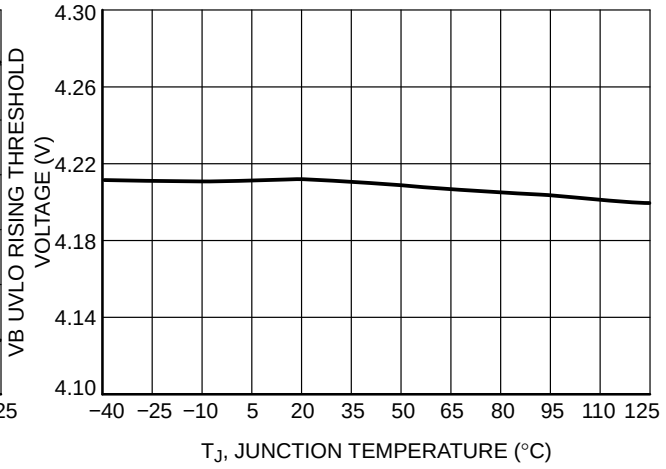


Figure 12. VB UVLO Rising Threshold vs. Junction Temperature

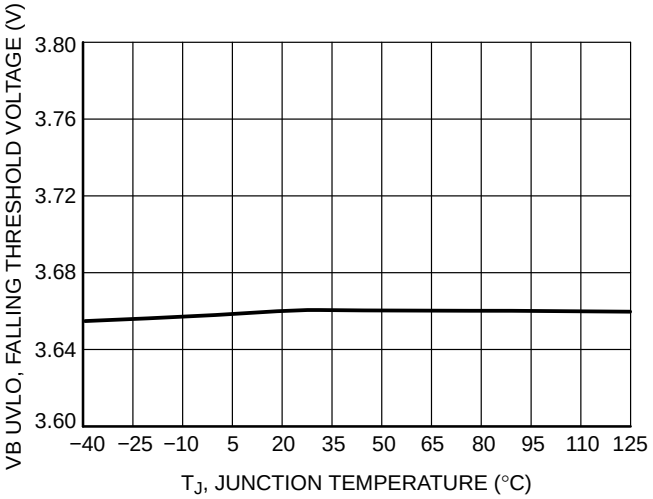


Figure 13. VB UVLO Falling Threshold vs. Junction Temperature

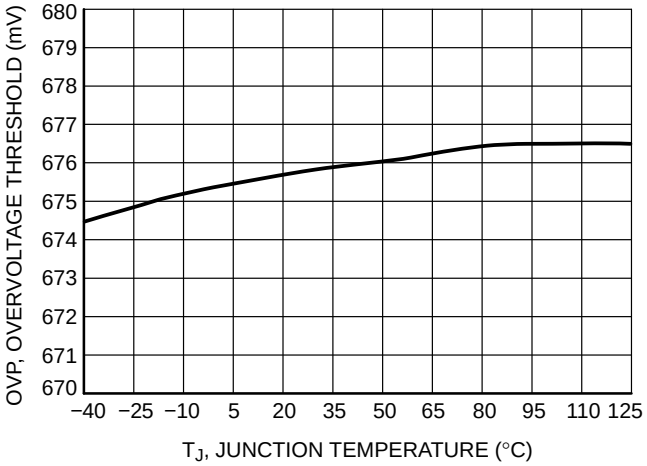


Figure 14. Output OVP vs. Junction Temperature

TYPICAL CHARACTERISTICS

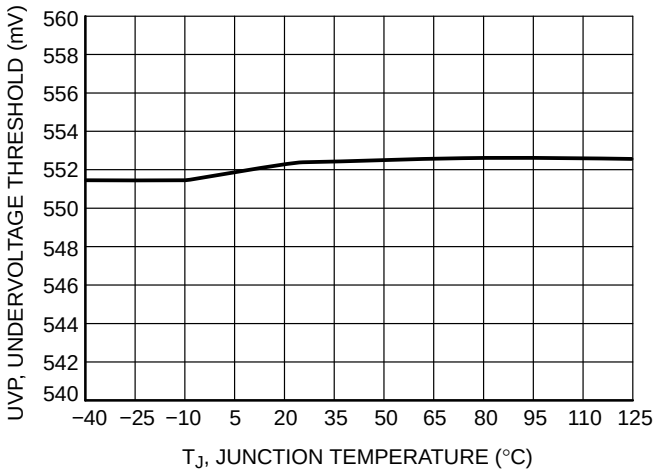


Figure 15. Output UVP vs. Junction Temperature

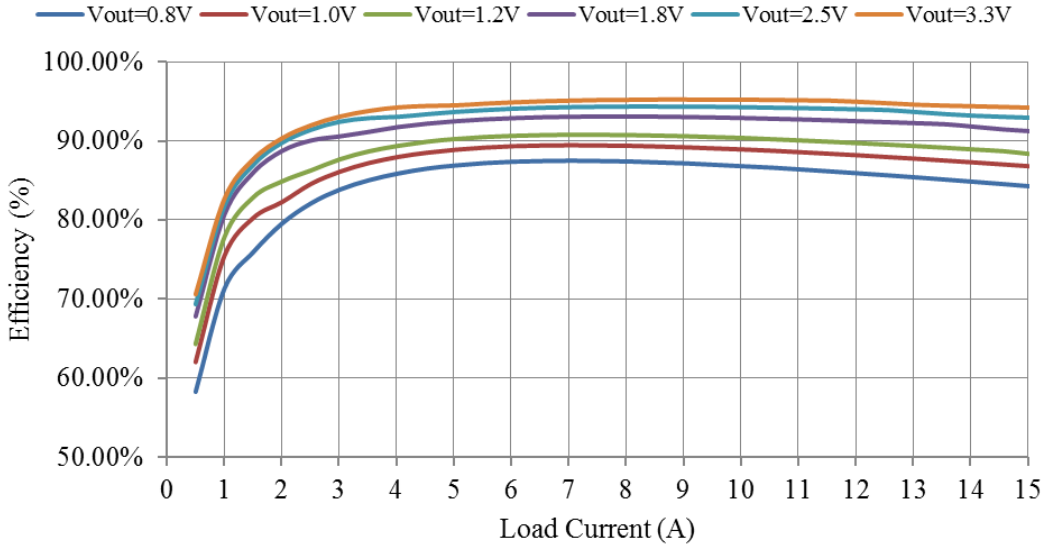


Figure 16. Efficiency vs. Load Current (Vin=12 V)

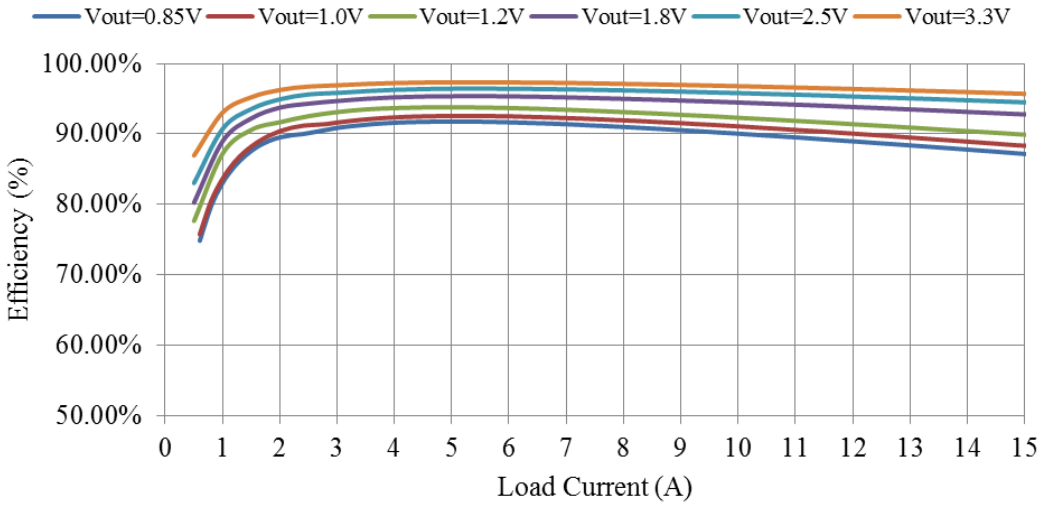
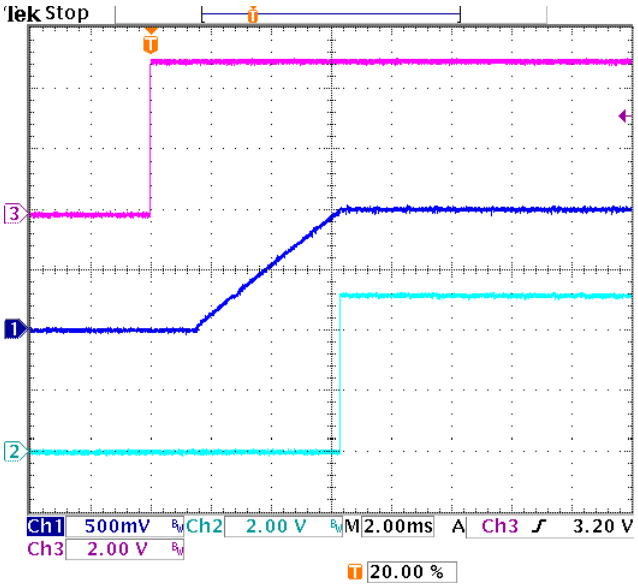


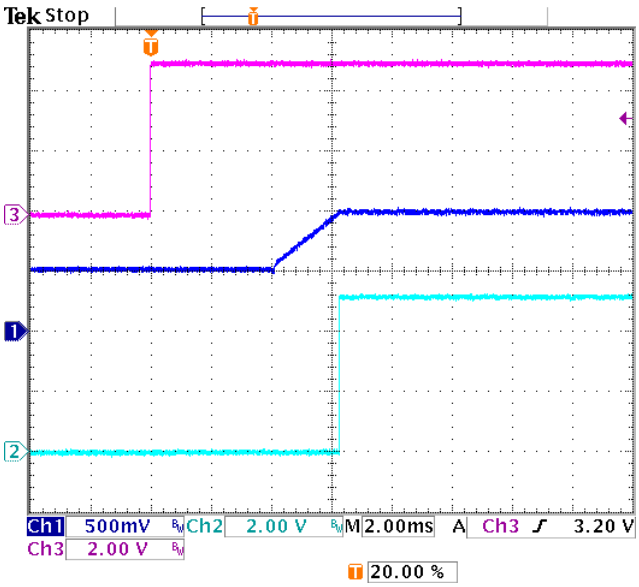
Figure 17. Efficiency vs. Load Current (Vin=5.5 V)

TYPICAL CHARACTERISTICS



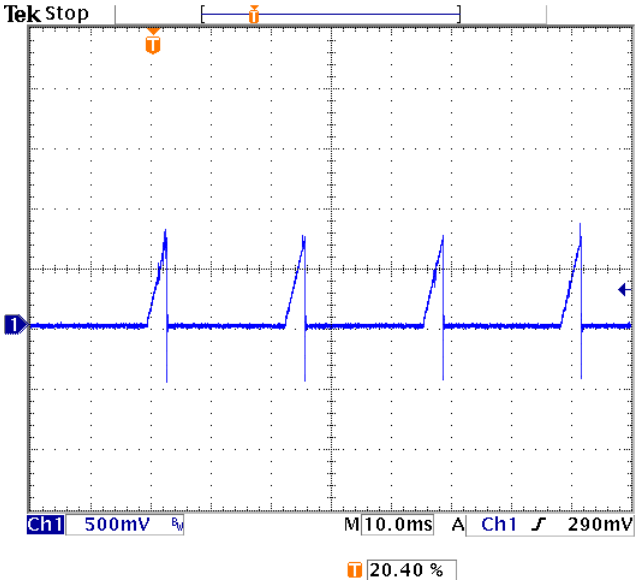
CH1 (Blue): VOUT
CH2 (Aqua): PG
CH3 (Purple): EN

Figure 18. Soft Start Waveform (Vin = 12 V, Vout = 1 V)



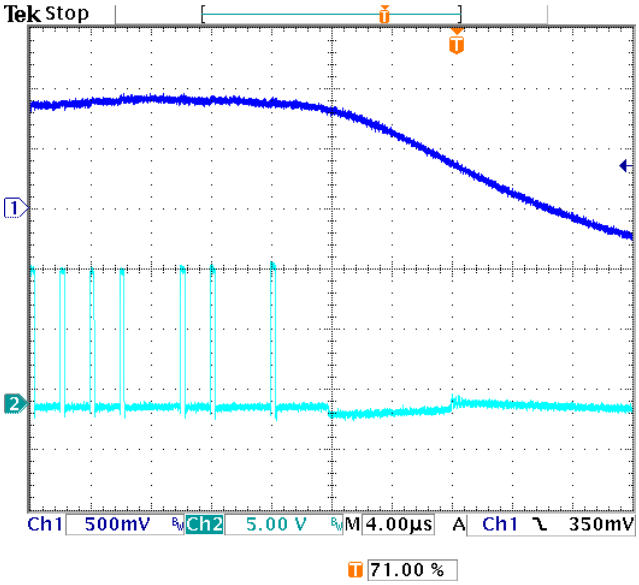
CH1 (Blue): VOUT
CH2 (Aqua): PG
CH3 (Purple): EN

Figure 19. Pre−bias Soft Start Waveform (Vin = 12 V, Vout = 1 V, Pre−bias = 0.5 V)



CH1 (Blue): VOUT

Figure 20. Output Voltage Hiccup Protection Waveform



CH1 (Blue): VOUT
CH2 (Aqua): VSW

Figure 21. Over−current Protection Pulse Skipping Waveform

OVERVIEW

The NCP3232N is a 500 kHz, high efficiency, high current PWM synchronous buck converter. It operates with a single supply voltage from 4.5 to 21 V and provide output current as high as 15 A. NCP3232N utilizes voltage mode with voltage feed-forward control to response instantly to Vin changes and provide for easier compensation over the supply range of the converter. The device also includes pre-bias startup capability to allow monotonic startup in the event of a pre-biased output condition.

Protection features include overcurrent protection (OCP), output over and under voltage protection (OVP, UVP), and power good. The enable function is highly programmable to allow for adjustable startup voltages at higher input voltages. There is also an adjustable soft-start, and over-temperature/over-voltage comparator, and internal thermal shutdown.

Reference Voltage

The NCP3232N incorporates an internal reference that allows output voltages as low as 0.6 V. The tolerance of the internal reference is guaranteed over the entire operating temperature range of the controller. The reference voltage is trimmed using a test configuration that accounts for error amplifier offset and bias currents.

Oscillator Ramp

The ramp waveform is a saw tooth form at the PWM frequency with a peak-to-peak amplitude of VCC/6.6, offset from GND by typically 0.64 V. The PWM duty cycle is limited to a maximum of 92%, allowing the bootstrap capacitors to charge during each cycle.

Error Amplifier

The error amplifier's primary function is to regulate the converter's output voltage using a resistor divider connected from the converter's output to the FB pin of the controller, as shown in the Applications Schematic. A type III compensation network must be connected around the error amplifier to stabilize the converter. It has a bandwidth of greater than 24 MHz, with open loop gain of at least 60 dB.

Programmable Soft-Start

An external capacitor connected from the SS pin to ground sets up the soft start period, which can limit the start-up inrush current. The soft start period can be programmed based on the Equation 1.

$$t_{ss} = \frac{C_{SS} \cdot V_{ref}}{I_{SS}} \qquad \text{(eq. 1)}$$

OCP is the only fault that is active during a soft-start.

Adaptive Non-Overlap Gate Driver

In a synchronous buck converter, a certain dead time is required between the low side drive signal and high side drive signal to avoid shoot through. During the dead time, the body diode of the low side FET freewheels the current. The body diode has much higher voltage drop than that of the MOSFET, which reduces the efficiency significantly. The longer the body diode conducts, the lower the efficiency. NCP3232N implements adaptive dead time control to minimize the dead time, as well as preventing shoot through.

Precision Enable (EN)

The ENABLE block allows the output to be toggled on and off and is a precision analog input.

When the EN voltage exceeds V_EN, the controller will initiate the soft-start sequence as long as the input voltage and sub-regulated voltage have exceeded their UVLO thresholds. V_EN_hyst helps to reject noise and allow the pin to be resistively coupled to the input voltage or sequenced with other rails.

If the EN voltage is held below typically 0.8 V, the NCP3232N enters a deep disable state where the internal bias circuitry is off. As the voltage at EN continues to rise, the Enable comparator and reference are active and provide a more accurate EN threshold. The drivers are held off until the rising voltage at EN crosses V_EN.

An internal 2 μA pullup automatically enables the device when the EN pin is left floating.

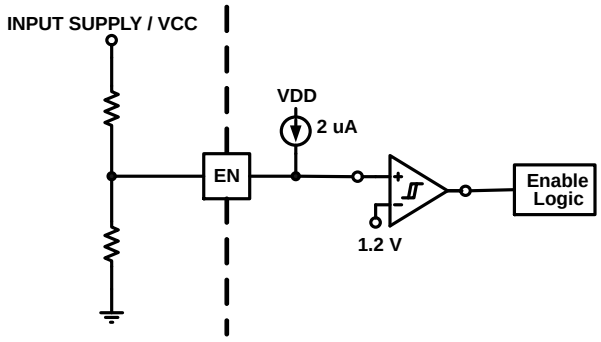


Figure 22. Enable Functional Block Diagram

Pre-bias Startup

In some applications the controller will be required to start switching when its output capacitors are charged anywhere from slightly above 0 V to just below the regulation voltage. This situation occurs for a number of reasons: the converter's output capacitors may have residual charge on them or the converter's output may be held up by a low current standby power supply. NCP3232N supports pre−bias start up by holding off switching until the feedback voltage and thus the output voltage rises above the set regulated voltage. If the pre-bias voltage is higher than the set regulated voltage, switching does not occur until the output voltage drops back to the regulation point.

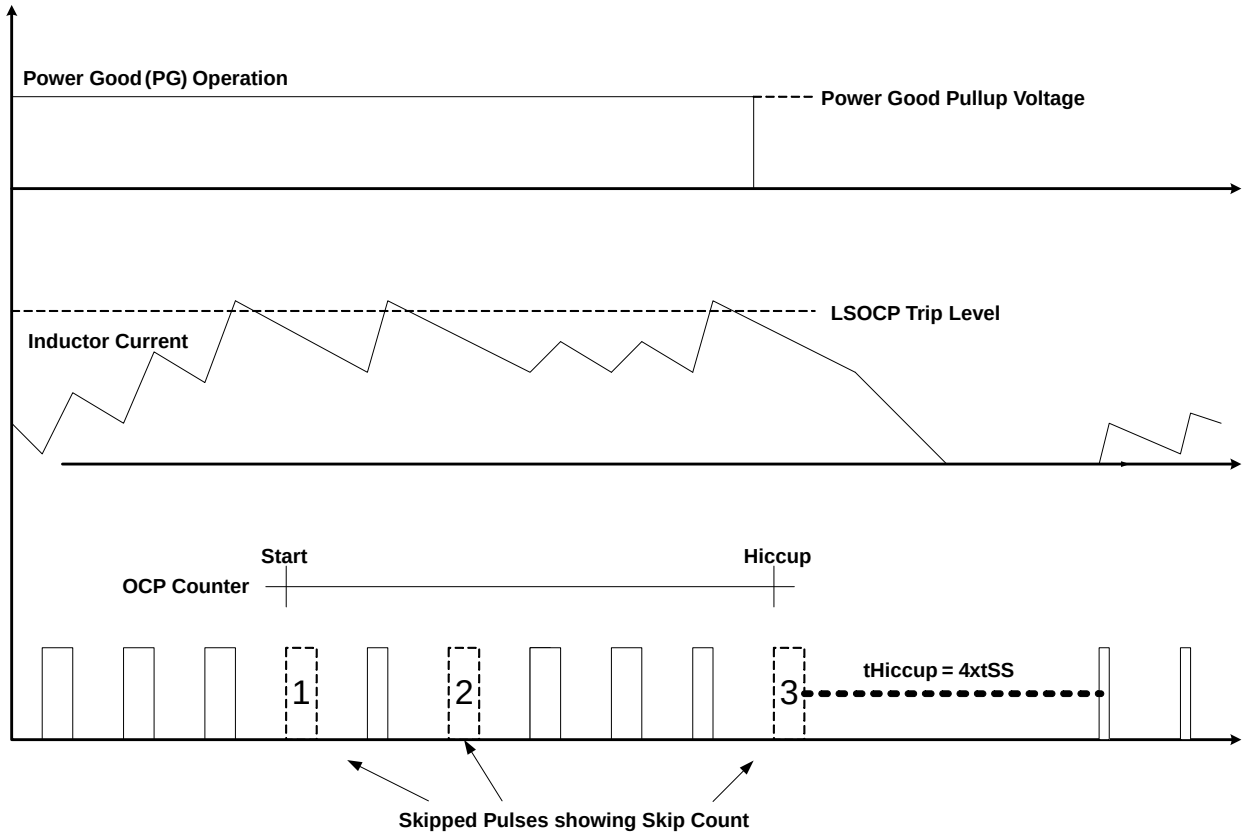


Figure 23. LSOCP Function with Counters and Power Good Shown (exaggerated for informational purposes)

PROTECTION FEATURES

Hiccup Mode

The NCP3232N utilizes hiccup mode for all of its fault conditions. Upon entering hiccup mode after a fault detection, the NCP3232N turns off the high side and low side FETs and PG goes low. It waits for tHICCUP ms before reinitiating a soft-start. tHiccup is defined as four soft start timeouts (tss). The equation for tss is shown in Equation 1. OCP is the only active fault detection during the hiccup mode soft start.

Over Temperature Comparator (OTS)

The NCP3232N provides an over-temperature shutdown (OTS) comparator with 50 mV hysteresis and a 0.6 V reference in order to remotely sense an external temperature detector or thermistor. When the voltage at the OTS pin rises above 0.6 V, the drivers stop switching and both FETs remain off. When this voltage drops below typically 0.55 V, a new soft-start cycle is generated automatically. Tie the OTS pin to ground if this function is not required.

Over Voltage Protection (OVP)

When the voltage at the FB pin (VFB) is above the OVP threshold for greater than 20 μs (typical), an OVP fault is set. The high side FET (HSFET) will turn off and the low side FET (LSFET) will turn on to discharge output voltage. The open-drain PG pull down will turn on at that point as well, thus pulling PG low. Once VFB has fallen below the Undervoltage Protection Threshold (UVP), the device will enter hiccup mode.

Under Voltage Protection (UVP)

A UVP circuit monitors the VFB voltage to detect an under voltage event. If the VFB voltage is below this threshold for more than 20 μs, a UVP fault is set and the device will enter hiccup mode.

Over Current Protection (OCP)

The NCP3232N over current protection scheme senses the peak freewheeling current in the low-side FET (LSOCP) after a blanking time of 150 ns as shown in Figure 23. The low-side FET drain-to-source voltage, VDS, is compared against the voltage of a fixed, internal current source, ISET and a user-selected resistor, RSET. Voltage across the low-side FET is sensed from the VSW pin to GND.

After an OCP detection, the NCP3232N keeps the high-side FET off until the Low-side FET current falls below the trip point again and the next clock cycle occurs. An internal OCP counter will count up to 3 consecutive LSOCP events. After the third consecutive count, the device enters hiccup mode.

To prevent nuisance trips, there is a backup counter that will reset the OCP counter after 7 consecutive cycles without an LSOCP trigger. The backup counter is reset and then started again after each OCP trip until the third OCP count as stated above occurs.

Over Current Protection Threshold (ISET)

The NCP3232N allows the user to adjust the LSOCP threshold with an external resistor, RSET. This resistor, along with an internal temperature compensated current source, ISET, sets the current limit reference voltage for the LSOCP comparator.

Internally, a current sense circuit samples the voltage from VSW to GND. This voltage is then multiplied by a factor of 2X and compared against the ISET*RSET voltage threshold.

The basic design equation for LSOCP trip point selection is:

$$RSET = \frac{2 \times ISET \times RDSON}{33 \times 10^{-6}} \quad \text{(eq. 2)}$$

In case RSET is not connected, the device switches the OCP threshold to a fixed 300 mV value: an internal safety clamp on ISET is triggered as soon as the ISET voltage reaches 600 mV, enabling the 300 mV fixed threshold.

Thermal Shutdown (TSD)

The NCP3232N protects itself from overheating with an internal thermal monitoring circuit. If the junction temperature exceeds the thermal shutdown threshold both the upper and lower MOSFETs will be shut OFF. Once the temperature drops below the falling hysteresis threshold, the voltage at the COMP pin will be pulled below the ramp valley voltage and a soft-start will be initiated.

Power Good Monitor (PG)

NCP3232N monitors the output voltage and signal when the output is out of regulation or during a non-regulated pre-bias condition, or fault condition. When the output voltage is within the OVP and UVP thresholds, the power good pin is a high impedance output. If the NCP3232N detects an OCP, OVP, UVP, OTS, TSD or is in soft start, it pulls PG pin low. The PG pin is an open drain 5-mA pull down output.

Layout Guideline

When laying out a power PCB for the NCP3232N there are several key points consider.

General Layout Guide: these are the common techniques for high frequency high power board layout design.

Base component placement: High current path components should be placed to keep the current path as tight as possible. Placement of components on the bottom of the board such as input or output decoupling can add loop inductance.

Ground Return for Power and Signals: Solid, uninterrupted ground planes must be present and adjacent to the high current path.

Copper Shapes on Component Layers: Large copper planes on one or multiple layers with adequate vias will increase thermal transfer, reduce copper conduction losses, and minimize loop inductance. Greater than 20 A designs require 2~3 layer shapes or more, increasing the number of layers will only improvement performance.

Via Placement for Power and Ground: Place enough vias to adequately connect outer layers to inner layers for thermal transfer and to minimize added inductance in layer transition. Multiple vias should be placed near important components like input ceramics and output ceramic capacitors.

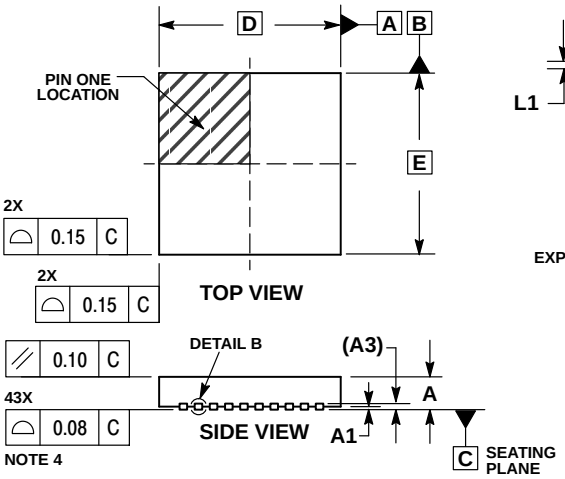
Key Signal Routes: Do not route sensitive signals, such as FB near or under noisy nets such as the switch node VSW and BST node, to reduce noise coupling effects on the sensitive lines.

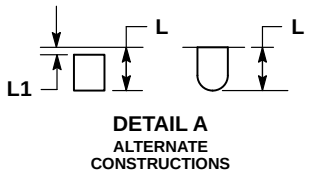
To improve the Low-side OCP accuracy, users should use single ground connection instead of separate analog ground and power ground. Make sure that the inner layers (at least 2nd layer, 3rd layer and 4th layer) are dedicated for ground plane. Do not use other copper planes to break or interrupt the shape of ground plane, which may add more parasitic components to affect the sensing accuracy.

Thermal management consideration: the major heat flow path from package to the ambient is through the copper on the PCB, the area and thickness of copper plane affect the themeral performance; maximize the copper coverage on all the layers to increase the effective thermal conductivity of the board. This is importatnt especially when there is no heat sinks attached to the PCB on the other side of the package; add as many thermal vias as possible directly under the package ground pad to maximize the effective out-of-plane thermal conductivity of the board; all the thermal vias must be either plated (copper) shut or plugged and capped on both sides of the board. This prevents solder seeping in to the thermal vias causing solder voids. Solder voides are higher detrimental to the thermal and electrical performance of the package; to ensure reliability and performance, the solder coverage should be at least 85 percent. This means the total voids on the ground pad should be less than 15 percent with no single void larger than 1 mm. Several smaller voids are always better than a few big voids.

PACKAGE DIMENSIONS

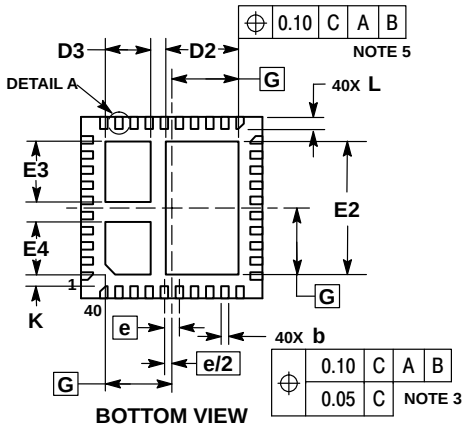
QFN40 6x6, 0.5P
CASE 485CM
ISSUE O

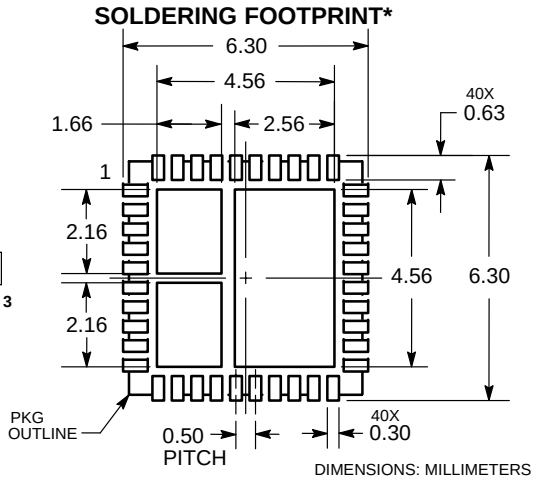




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. POSITIONAL TOLERANCE APPLIES TO ALL THREE EXPOSED PADS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	−−−	0.05
A3	0.20 REF	
b	0.18	0.30
D	6.00 BSC	
D2	2.30	2.50
D3	1.40	1.60
E	6.00 BSC	
E2	4.30	4.50
E3	1.90	2.10
E4	1.64	1.84
e	0.50 BSC	
G	2.20 BSC	
K	0.20	−−−
L	0.30	0.50
L1	−−−	0.15





*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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