TC35667FTG
Bluetooth® LE Single IC
For Bluetooth® Smart

Rev 1.x
Overview Document

Contents

1 General Description

1.1. Product Concept

TC35667FTG is IC based on a 2.4 GHz wireless-communications Bluetooth™ V4.0 Low Energy standard, which includes an RF analog part and a Baseband digital part. TC35667FTG provides Bluetooth™ HCI (Host Control Interface) function and LE (Low Energy) function specified in Bluetooth™ Specifications.

Connected with an external host processor, TC35667FTG easily realizes low energy consumption applications.

1.2. Features

- Compliant with Bluetooth™ Ver4.0 Low Energy
  - Built-in Bluetooth™ Baseband digital core
  - Built-in Bluetooth™ RF analog core
  - Built-in ARM7TDMI-S™ core
  - On-chip ProgramMask-ROM (320 KB)
  - On-chip Work RAM for Bluetooth™ Baseband process (96 KB)
  - On-chip RAM for application program storing (32 KB)
  - Supports patch program loader function
- General Purpose IO (16 pins)
- General Purpose Serial Interfaces
  - SPI interface (1 ch/General Purpose IO)
  - I2Cinterface (1 ch/General Purpose IO)
- Host CPU Interface
  - UART interface (2.4 kbps to 921.6 kbps, 2 channels – RTS/CTS are shared with TX2/RX2 and GPIO)
- Wake-up Interface (1 ch/General Purpose IO)
  - Wake-up input function from sleep and deep sleep
- PWM Interface (3 ch/General Purpose IO)
- Base Clock Input (26 MHz)
  - Built-in oscillator for external resonator connection
- Sleep Clock Input (32.768 kHz)
  - External input supported
  - Built-in oscillator for external resonator connection
  - Internal oscillation SiOSC supported
- Sleep and Deep Sleep Function
- Built-in DCDC converter and LDO
  - Wide range of input power supply voltage supported (1.8 to 3.6 V, single)
- Built-in general purpose ADC
  - 3 ch for external inputs
  - 1 ch for internal VDD detection
- Package:
  - QFN40-P-606-0.50 [40 pin, 6 x 6 mm2, 0.5 mm pitch, 0.9 mm thickness]

2. Pin Function

2.1. Pin Assignment (Top View) ver. QFN40-P-0606-0.50

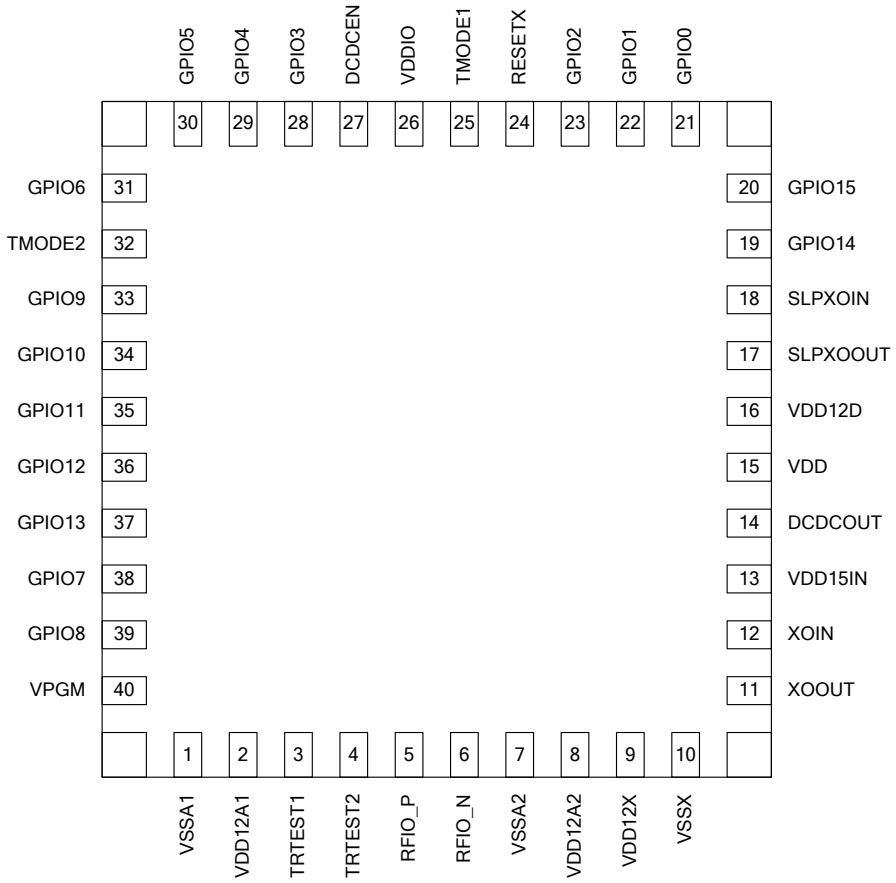


Figure 2-1 Pin Assignment (Top View)

2.2. Pin Function Descriptions

Details available only under NDA

Table 2.1-1 Pin Functions

2.3. GPIO function list

GPIO pins can be assigned to UART I/Fs, serial memory I/Fs or some other functions by TC35667FTG firmware or command from external Hosts. Table 2-2 shows available functions for each GPIO pin, and Table 2-3 examples of GPIO function settings.

Table 2.1-2 Available functions for GPIO

Pin	Analog input	Function 1	Function 2	Function 3	Function 4	Function 5
GPIO0	-	GPIO1 Digital I/O	WakeUp Input	-	-	-
GPIO1	ADC0 Input	GPIO Digital I/O	-	-	-	-
GPIO2	ADC1 Input	GPIO Digital I/O	PWM0 Output	-	-	-
GPIO3_TEST	-	GPIO Digital I/O	UART1-TX Output	-	SPI-DOUT Output	UART2-TX Output
GPIO4	-	GPIO Digital I/O	UART1-RX Input	-	SPI-DIN Input	UART2-RX Input
GPIO5_Bmode	-	GPIO Digital I/O	UART1-RTSX Output	UART2-TX Output	SPI-SCS Output	UART1-TX Output
GPIO6	-	GPIO Digital I/O	UART1-CTSX Input	UART2-RX Input	SPI-SCLK Output	UART1-RX Input
GPIO7	-	GPIO Digital I/O	-	I2C-SCL Output	SPI-DOUT Output	-
GPIO8	-	GPIO Digital I/O	-	I2C-SDA I/O	SPI-DIN Input	-
GPIO9	-	GPIO Digital I/O	PWM1 Output	I2C-SCL Output	-	-
GPIO10	-	GPIO Digital I/O	PWM2 Output	I2C-SDA I/O	-	-
GPIO11～14	-	GPIO Digital I/O	-	-	-	-
GPIO15	ADC2 Input	GPIO Digital I/O	-	-	-	-

Table 2.1-3 GPIO function list (example)

Details available only under NDA

2.4. Power Supply Pins

Details available only under NDA

2.5. Equivalent Circuit

Details available only System Configuration

2.6. Block Diagram

Details available only under NDA

TC35667FTG is powered by single voltage between 1.8 V and 3.6 V. The chip has built-in DCDC and LDO requiring external capacitors. It uses 26 MHz base clock and 32.768 kHz sleep clock. EEPROM Interface is SPI or I2C, and host CPU interface is UART.

Figure 2.1 available under NDA

3. Hardware Interfaces

3.1. Reset Interface (Power supply sequence)

Details only available under NDA

3.2. UART Interface

3.2.1. Features

TC35667FTG UART interface has the following features.

- 1.8 to 3.6 V operation
- Full-duplex start-stop synchronization data transfer (RX data, TX data)
- Either 1 ch of two-wire start-stop synchronization data transfer, 2 ch of two-wire start-stop synchronization data transfer , or four wire start-stop synchronization data transfer (RX, TX, CTS, RTX) are available depending on the settings.
- Programmable baud rate: 2400 bps to 921.6 kbps (UART2 has 9600 bps at the maximum)
- Error detection (character timeout, overrun error, framing error)

TC35667FTG communicates commands, status, and data with a host CPU through UART interfaces. The UART interfaces are shared with GPIO pins, and during boot process after reset is released, TC35667FTG firmware assigns UART interfaces to the GPIOs. The UART interfaces can operate at 3.0 V depending on the power supply voltage. They cannot operate at a different voltage from other hardware interfaces because they share the power supply terminal with other hardware interfaces.

3.2.2. Connection Example

Figure 4-3 shows UART connection example with an external host CPU. TC35667FTG UART can be connected with an UART interface on a host MCU. .Figure 3-4 shows the sequence diagram from reset state to UART active state.

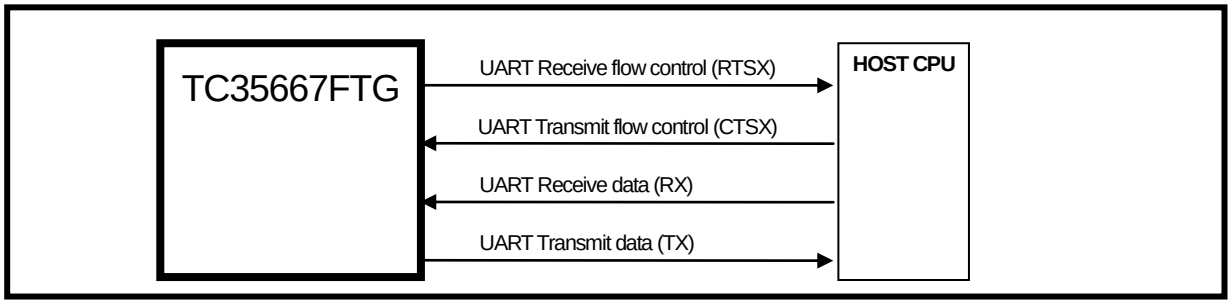
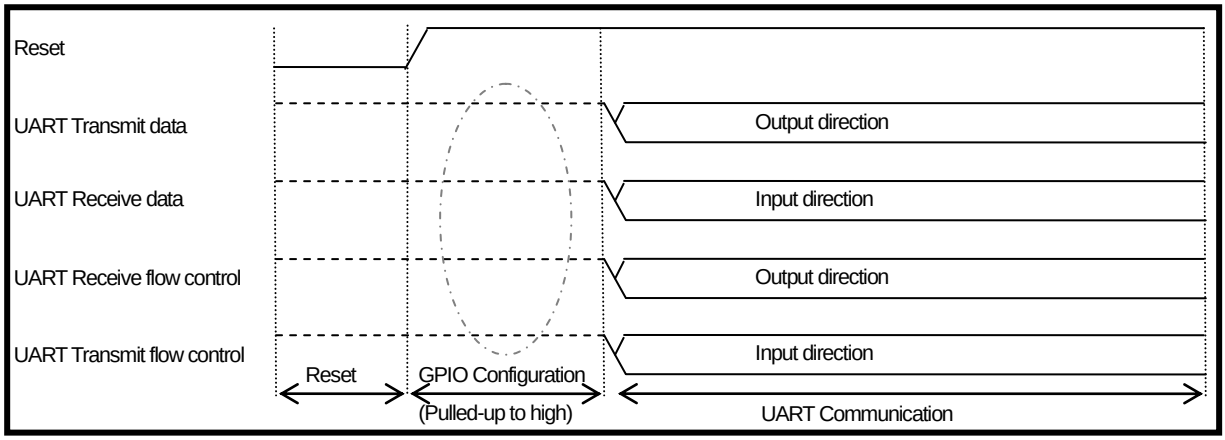


Figure 3-3 UART connection example



The flow control is supported only for UART1.

Figure 3-4 Power-up sequence for UART configuration

3.2.3. Frame Format

TC35667FTG supporting format is as follows.

- Number of data bits: 8 bits (LSB first)
- Parity bit: no parity
- Stop bit: 1 stop bit
- Flow control: RTSX/CTSX

Figure 3-5 shows UART data frame.

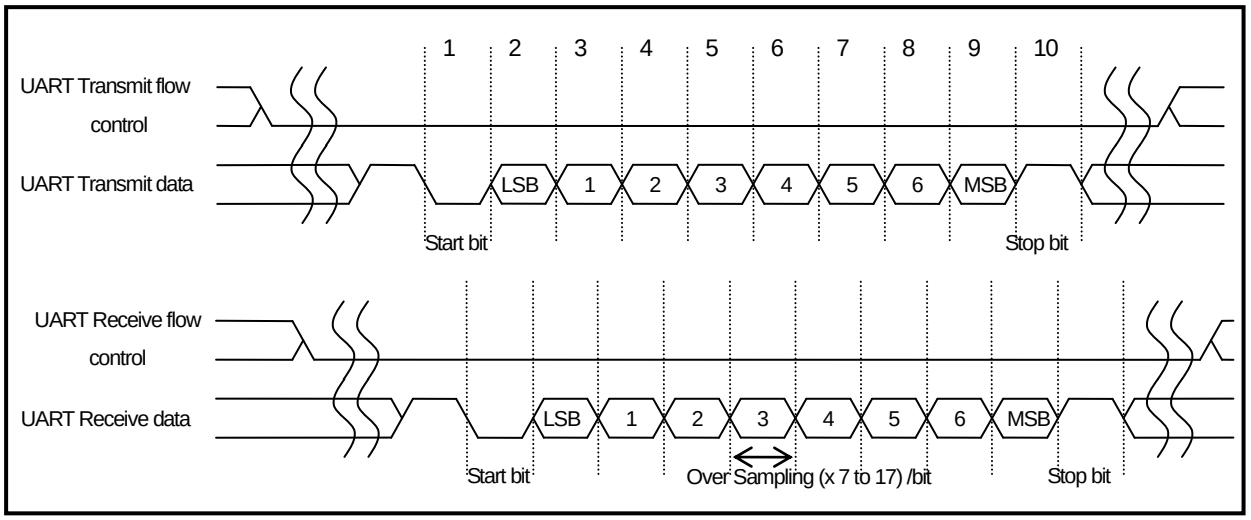


Figure 3-5 UART data frame

3.2.4. Flow Control Function

TC35667FTG UART interface uses flow control function by hardware signal when it is assigned to GPIO3 to GPIO6 as four wired UART1. Transmit flow control (CTSX) and receive flow control (RTSX). Figure 3-3 shows signals input and output direction. Figure 3-5 shows signal polarity.

CTSX (Clear to Send) input signal is used for UART transmitting. Low input indicates close of the preparation of the other party to receive data and TC35667FTG does UART transmitting data if there is data for transmission. In case of input high level, TC35667FTG stops transmitting on the basis of UART unit frame.

RTSX (Request to Send) input signal is used for UART receiving. Low output indicates request data transmission to UART transmit side device of the other party. TC35667FTG outputs Low level from RTSX when being able to receive data and prepares to receive data. When the UART becomes busy and cannot receive data, TC35667FTG makes RTSX high level, and stops UART communication on the basis of UART unit frame.

Response time of UART transmitting and receiving for flow control signal depends on baud rate and internal process status of frame. It is from 1 frame to 4 frames.

3.2.5. UART Baud Rate Setting

Details available only under NDA

3.2.6. Error Detect Function

Details available only under NDA

3.3. SPI Interface

3.3.1. Features

TC35667FTG has the following main features for a serial memory interface

- Operation voltage: 1.8 to 3.6 V
- SPI interface
  - Chip select: 1 channel
  - Chip select polarity: High-active, Low-active
  - Serial clock master operation: Polarity and phase are adjustable (one out of four options can be selectable)
  - Serial clock frequency: 25.5 kHz to 6.5 MHz (CPU normal 13 MHz)
    1.96 kHz to 500.0 kHz (CPU slow 1 MHz)
  - Serial data transfer mode: MSB-first, LSB-first

3.3.2. Connection Example

Serial EEPROMs and serial Flash-ROMs can be connected to TC35667FTG SPI interface.

TC35667FTG has one chip select port. Figure 3-6 shows a connection example, where a serial Flash-ROM is connected to TC35667FTG. .

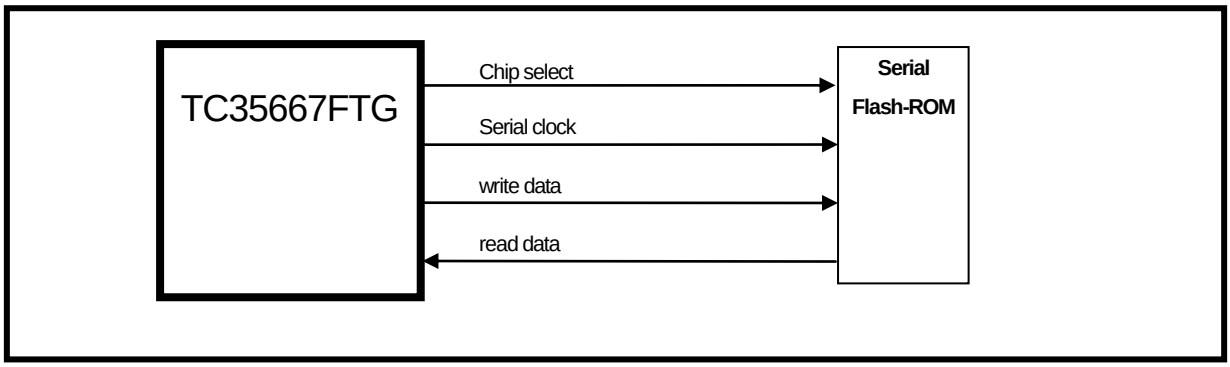


Figure 3-6 Connection example for serial Flash-ROM using SPI interface

3.3.3. Frame Format

When the SPI interface is connected to external ICs, the first 8 bit (X7 to X0) specifies the address and read or write mode. The command recognition code type and the address bit width should be determined by the external IC in use. For more information in detail, please refer to the technical documents for the external IC.

Figure 4-7 shows an example where 8-bit address is written and then 8-bit data is read. Figure 4-8 shows an example where 8-bit address is written and then 8-bit data is written.

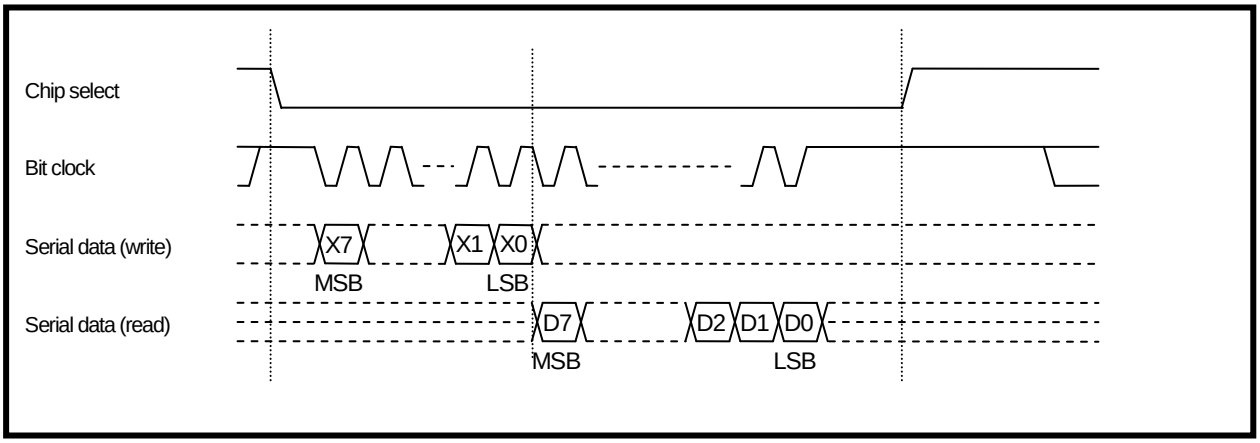


Figure 3-7 SPI format (single byte read)

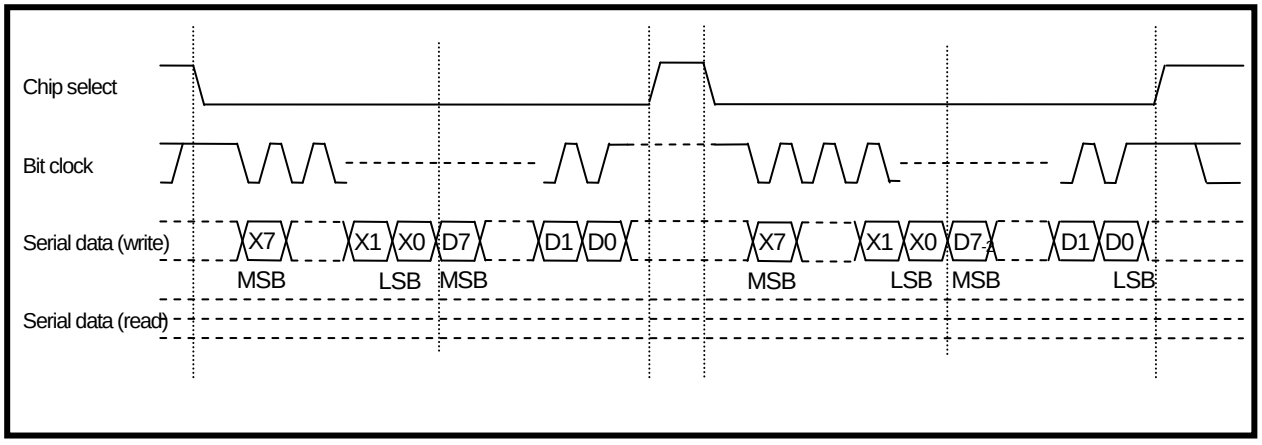


Figure 3-8 SPI format (single byte write)

3.4. I2C Interface

3.4.1. Features

TC35667FTG has the following main features for a serial memory interface.

- Operation voltage: 1.8 to 3.6 V
- I2C bus interface
  - Operation mode: I2C bus master
  - Serial clock frequency: Standard mode (100 kHz or less), Fast mode (400 kHz or less)
    # When the internal CPU slow clock is operating at 1 MHz, the serial clock frequency is limited to less than 27.8 kHz for standard mode.
- Output mode: Open-drain output, CMOS output
- Device address format: 7-bit address (10-bit address is not supported)

3.4.2. Connection Example

Figure 3-9 shows a connection example of a serial EEPROM using I2C bus interface of the open-drain mode. External pull-up resistors (Rext) are necessary for both serial clock line and serial data line.
Figure 3-10 shows another connection example where I2C bus is in the CMOS output mode. Only the serial data line needs Rext because this line can be driven by neither TC35667FTG nor a serial EEPROM.

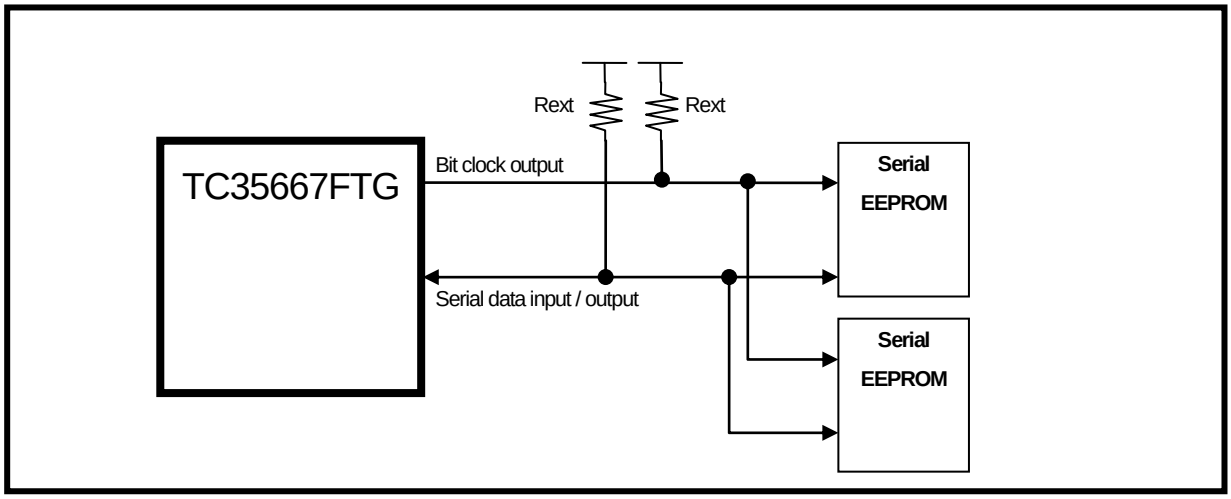


Figure 3-9 Connection example for serial EEPROM with I2C-bus interface (Open-drain output)

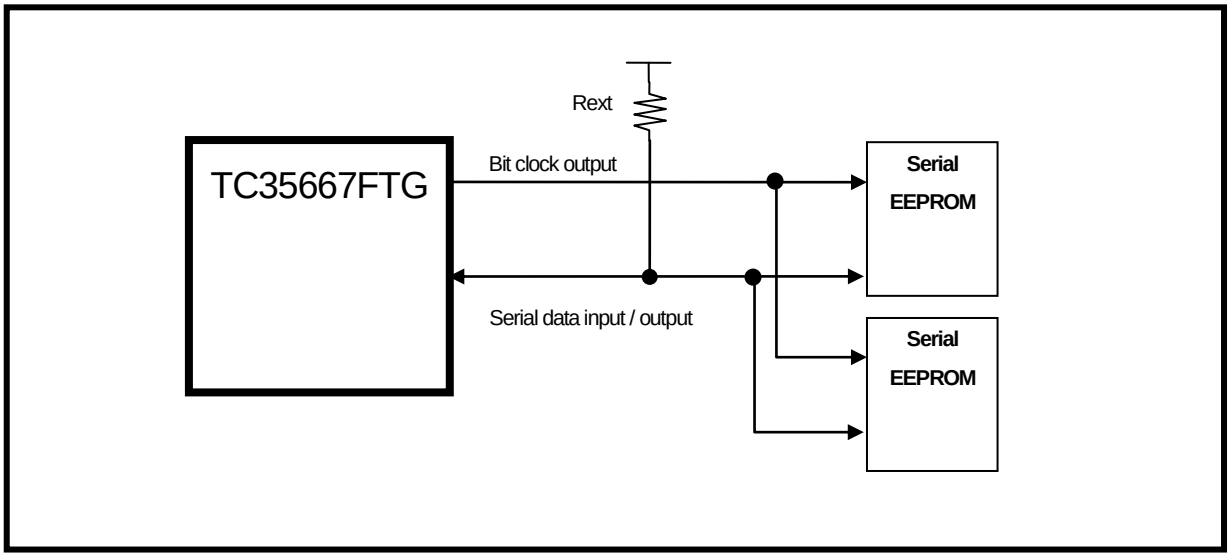


Figure 3-10 Connection example for serial EEPROM with I2C-bus interface (CMOS output)

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3.4.3. Selection of External Pull-up Resistor Value

Details available only under NDA

3.4.4. Frame Format

For I2C format, TC35667FTG first generates start condition. Then, it sends device recognition address (7 bit: [A6:A0]) and the first byte address ([B7:B0]) for the access target. Next, it goes for read or write sequence. For I2C, every data is sent as MSB first. The value of device recognition address and the way byte address is specified should be set as they are specified depending on connected devices. For read operation, TC35667FTG returns to the serial memory either receive acknowledge bit (ACK) or receive not acknowledge bit (NACK) every time it receives one byte. For write operation, TC35667FTG receives either ACK or NACK from the serial memory every time it sends one byte. It can handle not only one byte but also several bytes in a row. TC35667FTG generates stop condition when it has finished all the read or write of data.

Figure 4-11 shows an example where TC35667FTG reads two-byte data. Figure 4-12 shows an example where TC35667FTG writes two-byte data. In these examples, gray texts and lines indicate signals that are given by the serial memory. For read operation, after having read the final byte data, TC35667FTG returns NACK with which the serial memory gets to know the completion of the read operation.

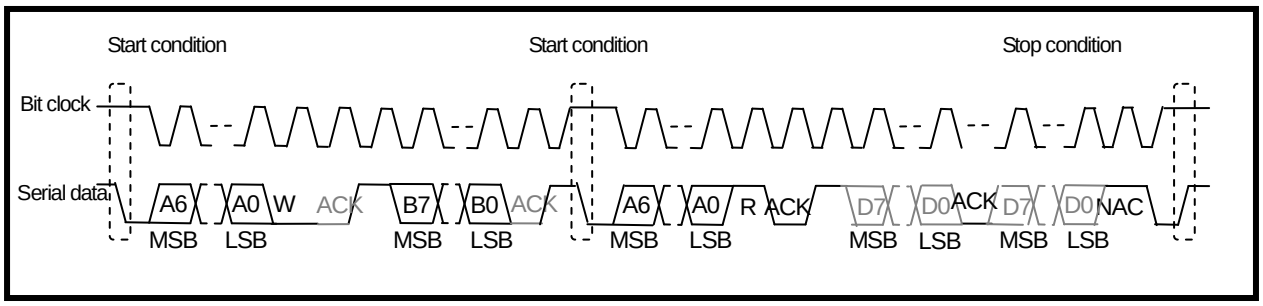

Figure 3-11 I2C format (Serial memory, read)

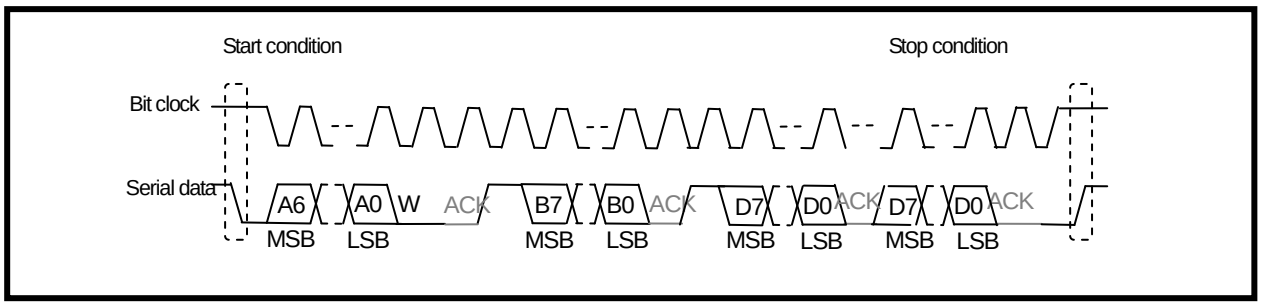

Figure 3-12 I2C format (Serial memory, write)

3.5. PWM Interface

Details only available under NDA

3.5.1. Pulse Generation Function

Details only available under NDA

3.5.2. Rhythm Function (Output Masking)

Details only available under NDA

3.6. ADC

3.6.1. Features

TC35667FTG has 4 channels of 10-bit ADCs for battery monitoring, analog inputs from external sensors, for example. The ADC has the following features.

- 3 channels of analog inputs (shared with GPIO terminals)
- 1 channel of VDD voltage monitor (reference voltage is 1.2 V LDO output.)
- Maximum conversion rate: 1 MS/s

The ADC converts inputs from channels selected by register settings. When a conversion has finished, the CPU detects it by the interrupt or register polling, and then returns the results. The maximum sampling rate depends on software load on the CPU.

Details only available under NDA

3.7. IC Reference Clock Interface

3.7.1. Features

TC35667FTG has the following features for IC reference clock interface which receives an external clock.

- Clock frequency: 26 MHz (The deviation should be adjusted within 50 ppm at the temperature in use)

TC35667FTG has an internal feed-back resistor between XOIN and XOOUT and doesn't require external feedback resistors. Please adjust external capacitors (C_{IN} and C_{OUT}) based on PCB layout and assembly if necessary within the range of the X'tal's specification.

3.7.2. Connection Example

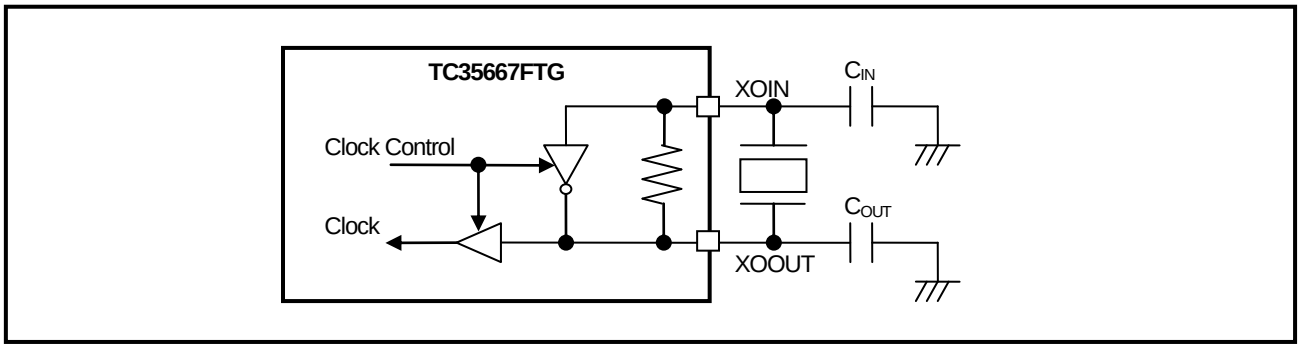

Figure 3-16 OSC connection example

3.7.3. Oscillation Frequency Adjust Function

Details available only under NDA

3.8. Sleep Clock Interface

TC35667FTG has the following features for sleep clock interface which receives an external clock.

- Type: Crystal oscillator (OSC)
- Clock frequency: 32.768 kHz (please adjust the frequency accuracy within plus or minus 500 ppm at the temperature in use)

Details available only under NDA

3.8.1. Connection Example

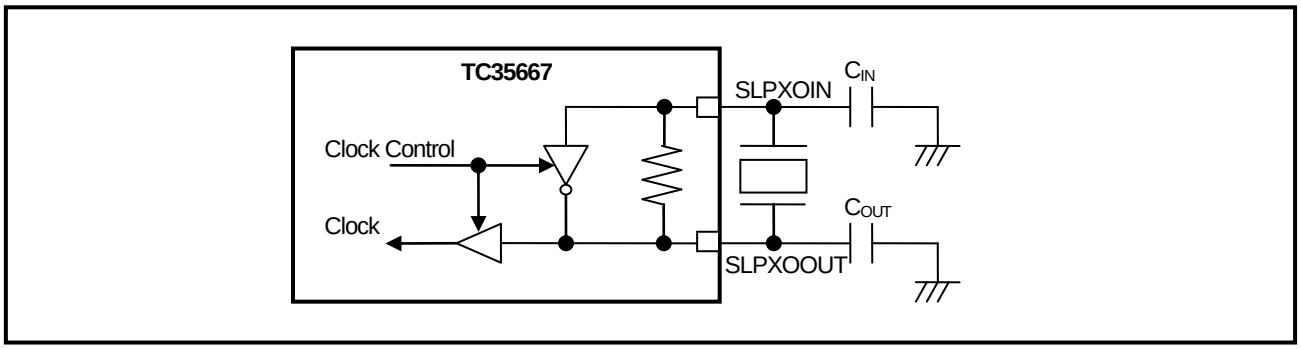

Figure 3-1 Sleep clock connection example

4. Electric Characteristics

4.1. Absolute Maximum Ratings

Maximum ratings must not be exceeded even for a moment. Voltages, currents, and temperatures that exceed the maximum ratings can cause break-downs, degradations, and damages not only for ICs but also for other components and boards. Please make sure application designs not to exceed the maximum ratings in any situation.

Table 5-1 Maximum ratings (VSSA1 = VSSA2 = VSSD = VSSX = 0 V)

Items	Symbols	Ratings		Units
		Minimum	Maximum	
Power supply	VDD VDDIO*	-0.3	+3.9	V
Input voltage	VIN	-0.3	VDDIO + 0.3	V
Output voltage	VOUT	-0.3	VDDIO + 0.3	V
Input current	IIN	-10	+10	mA
Input voltage	RFIO	—	+6	dBm
Storage temperature	—	-40	+125	degC

*

Note: It is not supposed that VDD is grounded while VDDIO is supplied. It can trigger current path from VDDIO to VDD through internal circuitry, and may cause degradations and break-downs.

4.2. Recommended Operating Conditions

TC35667FTG can operate normally with proven quality under the recommended operating conditions. Any diversion from the recommended operating conditions may cause false operation. Thus, please make sure application design to comply these recommended operating conditions.

Table 4-1 Recommended operating conditions (VSSA1 = VSSA2 = VSSD = VSSX = 0 V)

Items	Symbols	Ratings			Units
		Minimum	Typical	Maximum	
Power supplies	Operating VDD	1.8	3.0	3.6	V
	Power up VDD	TBD	1.87	TBD	V
	VDD detection	TBD	1.80	TBD	V
	VDDIO	1.8	3.0	3.6	V
	VDD15IN	1.45	1.5	3.6	V
	VDD12A1 / VDD12A2 / VDD12D / VDD12X.	—	1.2	—	V
RF frequency	Fc	2400	—	2483.5	MHz
Clock frequencies	Fck	25.99948	26.00000	26.00052	MHz
	fslclk	32.759808	32.768000	32.776192	kHz
Ambient temp.	Ta	TBD	+25	TBD	degC

Note; Please refer to other documents for our recommended connection examples.
Please do not input power supply and do connect external capacitors to VDD12A1, VDD12A2, VDD12D, and VDD12X because they are supplied by the internal LDO.

4.3. DC electric characteristics

Details only available under NDA

4.4. Built-in Regulator Characteristics

Table 4-2 Built-in regulator characteristics (VDD = 1.8 to 3.6 V, VSSA1 = VSSA2 = VSSD = VSSX = 0 V)

Item	Symbol	Pin names and conditions	Ratings			Units
			Minimum	Typical	Maximum	
Input voltages	Vin1	Power up VDD1	TBD	1.80	TBD	V
	Vin2	Power up VDD 2	TBD	1.87	TBD	V
Output voltages	Vout1	DCDCOUT	1.45	1.5	1.6	V
	Vout2	VDD12A1 / VDD12A2 /VDD12D /VDD12X	1.1	1.2	1.3	V
	Vout3	VDD12D	0.7	1.2	1.3	V

Note: DCDC has low VDD detector and stops its operation for VDD less than 1.0 V. The detection voltage has hysteresis so that it doesn't repeat powering on over again due to the load variation after it has stopped the operation. When VDD rises up, DCDC starts at more than 2 V VDD. When VDD is supplied externally, DCDC also requires more than 2 V VDD to start up.

4.5. ADC Characteristics

Table 4-3 ADC characteristics (VDD = 1.8 to 3.6 V, VSSA1 = VSSA2 = VSSD = VSSX = 0 V)

Item	Symbol	Condition	Ratings			Unit
			Minimum	Typical	Maximum	
Analog reference voltage	VREFH		1.8	-	3.6	V
Analog input voltage	VAIN	—	VSSD	-	VREFH	V

4.6. RF Characteristics

Details only available under NDA

4.7. AC Interface Characteristics

4.7.1. UART Interface

Table 4-8 UART Interface AC characteristics

Symbols	Items	Min	Typ.	Max	Unit
tCLDTDLY	Transmit Data ON from CTSX Low level	96	-	-	ns
tCHDTDLY	Transmit Data OFF from CTSX High level	-	-	2	byte
tTXDIV	Transmit Data Tolerance (per 1 Symbol) (*1)	-0.756	-	+0.756	%
tRLDTDLY	Received Data ON from RTSX Low level	0	-	-	ns
tRHDTDLY	Received Data OFF from RTSX High level	-	-	8	byte
tRXDIV	Received Data Acceptable Tolerance (per 1 Symbol) (*1)	-0.756	-	+0.756	%

(*1) Difference between ideal and real value

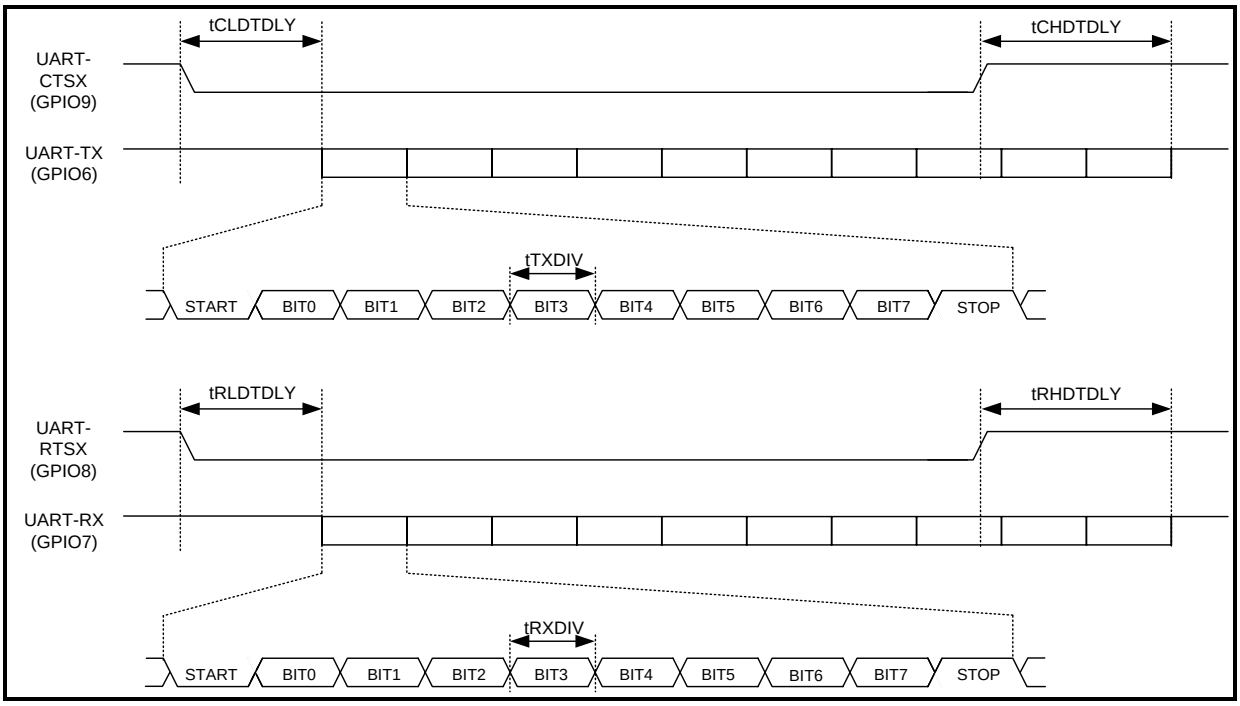

Figure 4-1 UART Interface Timing Diagram

4.7.2. I2C Interface

4.7.2.1. Normal Mode

Table 4-9 I2C Interface Normal mode AC Characteristics

Symbols	Items	Min	Typ.	Max	Unit
tDATS	Data set-up time	250	-	-	ns
tDATH	Data hold time	300	-	-	ns
tDATVD	Datavalidity period	-	-	3450	ns
tACKVD	ACKvalidity period	-	-	3450	ns
tSTAS	Restart condition set-up time	4700	-	-	ns
tSTAH	Restart condition hold time	4000	-	-	ns
tSTOS	Stop condition set-up time	4000	-	-	ns
tBUF	Bus open period from stop condition to start condition	4700	-	-	ns
tr	Rise up time	-	-	1000	ns
tf	Fall down time	-	-	300	ns
tHIGH	Serial clock period of High	4000	-	-	ns
tLOW	Serial clock period of Low	4700	-	-	ns
Cb	Bus load capacitance	-	-	400	pF

When CPU is operating at 13 MHz

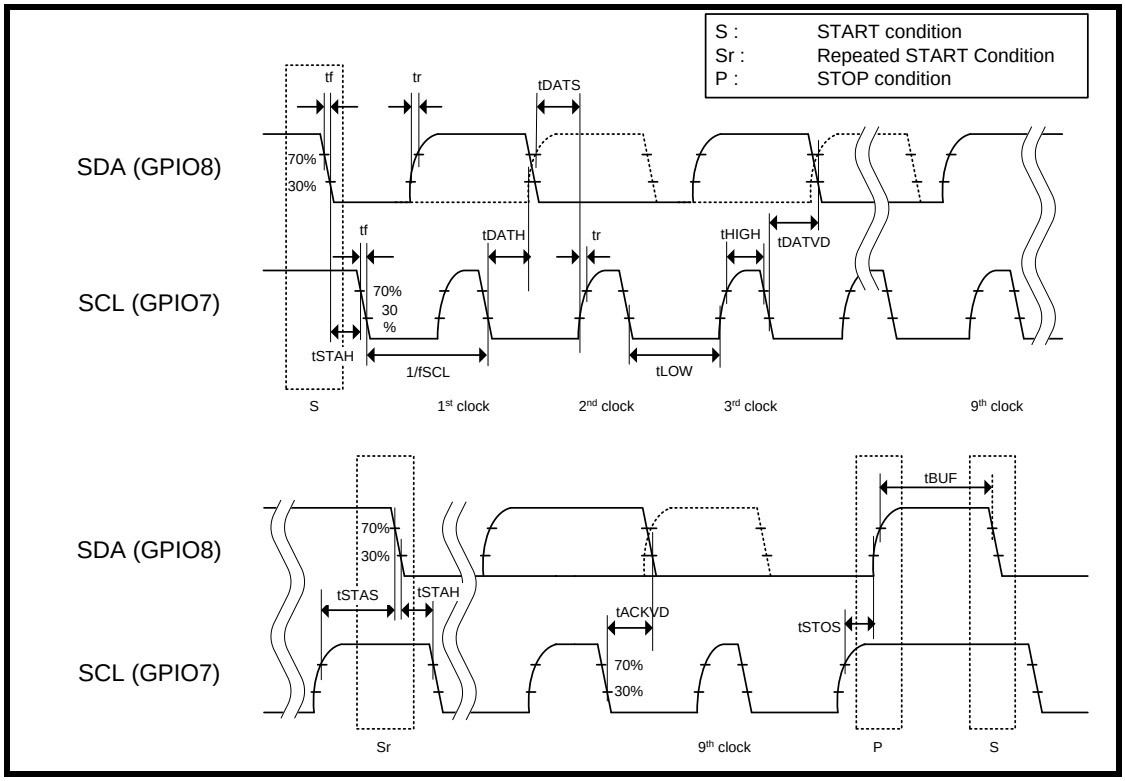

Figure 4-2 I2C Interface Normal mode Timing diagram

4.7.2.2. Fast mode

Table 4-10 I2C Interface Fast mode AC Characteristics

Symbols	Items	Min	Typ.	Max	Unit
tDATS	Data set-up time	100	-	-	ns
tDATH	Data hold time	300	-	-	ns
tDATVD	Datavalidity period	-	-	900	ns
tACKVD	ACKvalidity period	-	-	900	ns
tSTAS	Restart condition set-up time	600	-	-	ns
tSTAH	Restart condition hold time	600	-	-	ns
tSTOS	Stop condition set-up time	600	-	-	ns
tBUF	Bus open period from stop condition to start condition	1300	-	-	ns
tr	Rise up time	20 + 0.1Cb	-	300	ns
tf	Fall down time	20 + 0.1Cb	-	300	ns
tSP	Spike pulse width that can be removed	0	-	50	ns
tHIGH	Serial clock period of High	600	-	-	ns
tLOW	Serial clock period of Low	1300	-	-	ns
Cb	Bus load capacitance	-	-	400	pF

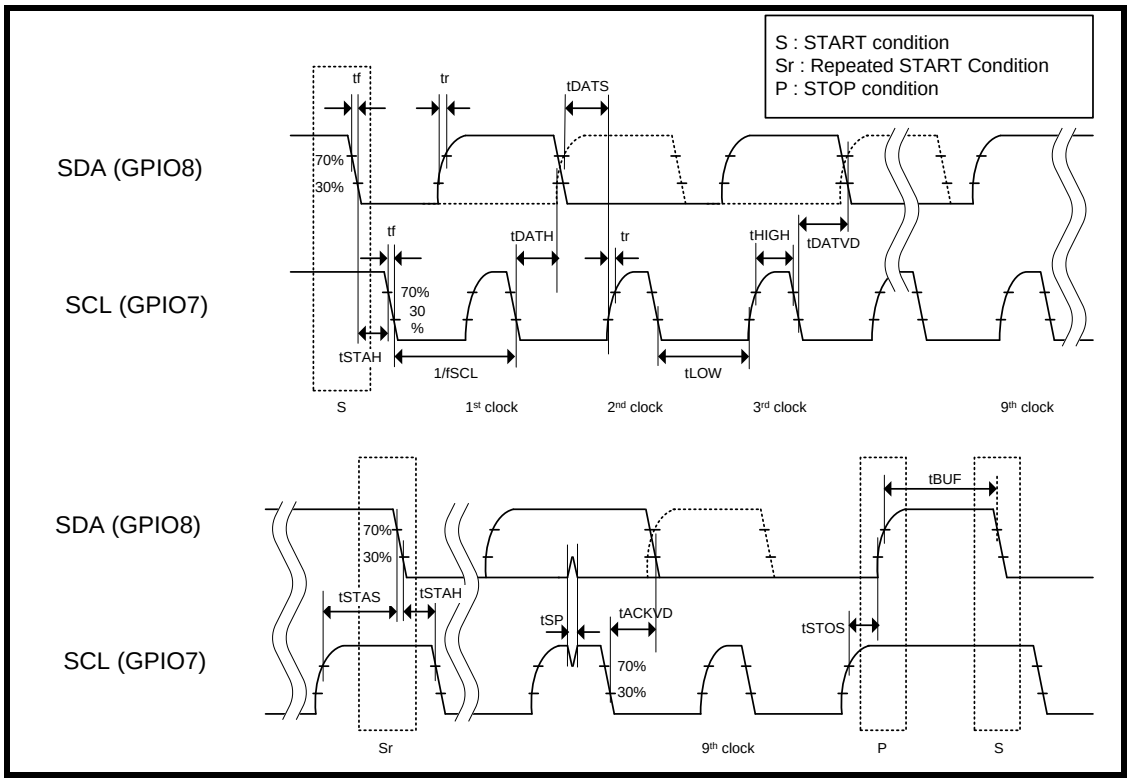

Figure 4-3 I2C Interface Normal mode Timing diagram

4.7.3. SPI Interface

Table 4-4 SPI Interface

Symbols	Items	Min.	Typ.	Max.	Unit
tSPICLKCYC	SPI clock frequency	154	-	-	ns
tSPICLKHPW	SPI clock high pulse width	77	-	-	ns
tSPICLKLPW	SPI clock low pulse width	77	-	-	ns
tSPICSS	SPI chip select setup time	38	-	-	ns
tSPICSH	SPI chip select hold time	77	-	-	ns
tSPIIW	SPI transfer idle pulse width	54	-	-	ns
tSPIAS	SPI address setup time	38	-	-	ns
tSPIAH	SPI address hold time	77	-	-	ns
tSPIDS	SPI data setup time	38	-	-	ns
tSPIDH	SPI data hold time	77	-	-	ns
tSPIDLY	SPI output delay	-	-	TBD	ns

#Serial memory interface operates on the basis of 1/n frequency of half the frequency of ARM7 core clock (6.5 MHz for 13 MHz core clock)

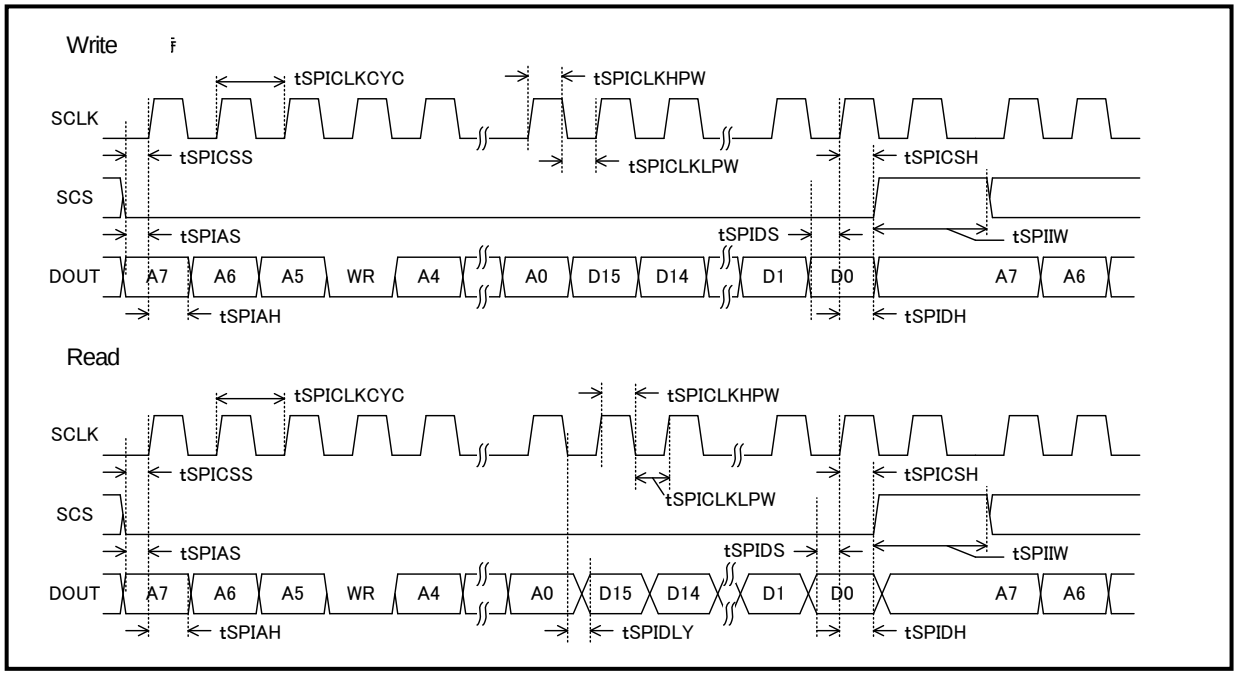

Figure 4-4 SPI Interface timing diagram

5. System Configuration Example

This figure shows an example of system configuration.

5.1. In case of Host CPU connection

Host interface=UART, 26MHz Reference Clock= XOSC Connection,

32.768 kHz XOSC (enclosed by a dotted line) not need to select the built-in SiOSC or external input (sharing with HOST).

Details available only under NDA

Figure 6-1 Example of TC35667FTG system configuration (HOST CPU connection)

5.2. In case of Standalone

32.768 kHz XOSC (enclosed by a dotted line) is not need to select the built-in SiOSC or external input (sharing with HOST).

Details available only under NDA

Figure 4-2 Example of TC35667FTG system configuration (Stand-alone)

6. Package outline

6.1. Outline dimensional drawing

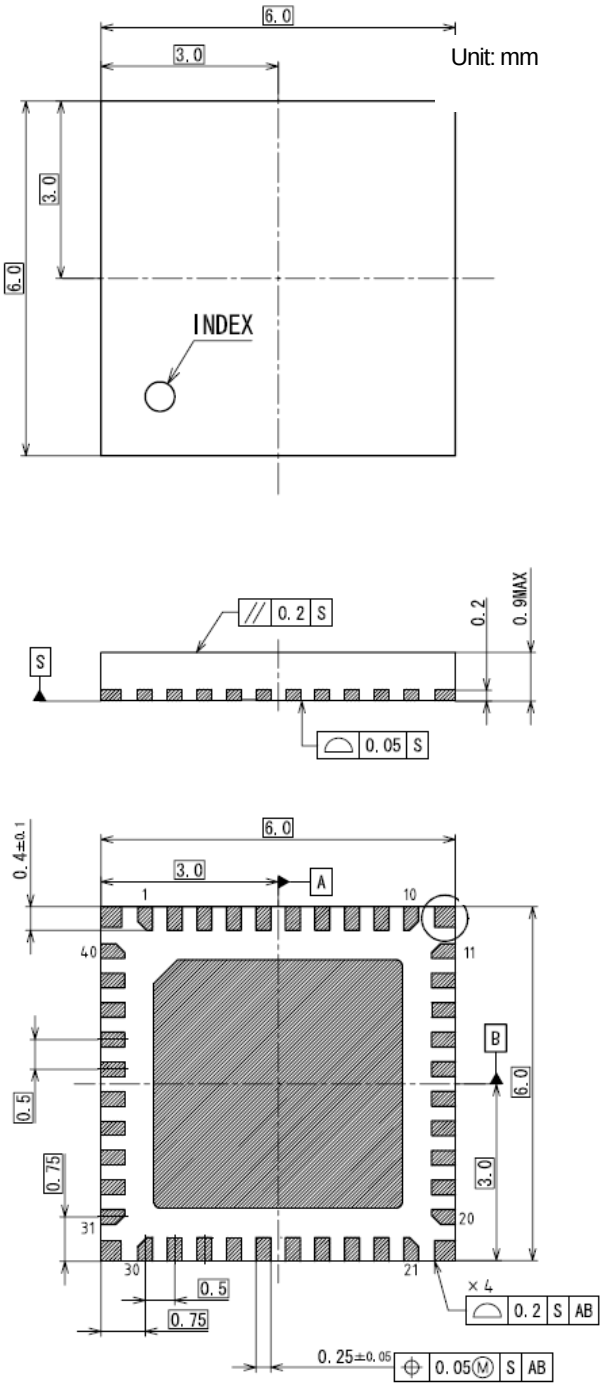

Figure 6.1-1 Package outline (QFN40-P-0606-0.5)

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