MXO45LV & MXO45HSLV

HCMOS/TTL Clock Oscillators

Part Dimensions:
20.8 × 13.2 × 5.1mm • 3.774537g
13.2 × 13.2 × 5.1mm • 2.206637g

Features

- Standard 14-Pin or 8-Pin Metal DIP Packages
- Fundamental and 3rd Overtone Crystal Designs
- Low Phase Jitter Performance
- Frequency Range 1 – 200MHz
- +3.3V Operation
- Output Enable Option Available
- Three Approved Packing Methods.

Applications

- Computers & Peripherals
- Storage Area Networking
- Broadband Access
- Microcontrollers/FPGAs
- Networking Equipment
- Ethernet/Gigabit Ethernet
- Fiber Channel
- Test and Measurement

Description

CTS MXO45LV and MXO45HSLV are legacy thru-hole clock oscillators that offer a low cost design supporting older HCMOS/TTL applications. MXO45LV/MXO45HSLV is not recommended for new design activity, but is available to support existing applications developed for the full and half-size metal DIP packages.

Ordering Information

Model	Package Type/ Output Enable		Frequency Stability	Temperature Range		Frequency Code [MHz]
MXO	45LV	-	3	C	-	XXXMXXXXXX

Code	Package/Enable
45LV	14-Pin DIP/STD Output [no enable]
45TLV	14-Pin DIP/Output Enable
45HSLV	8-Pin DIP/STD Output [no enable]
45HSTLV	8-Pin DIP/Output Enable

Code	Temp. Range
C	-20°C to +70°C
I	-40°C to +85°C

Code	Stability
6	±20ppm [1]
5	±25ppm
3	±50ppm
2	±100ppm

Code	Frequency
	Product Frequency Code [2]

Notes:

1] Consult factory for availability of 6C Stability/Temperature combination. The 6I combination is not available.

2] Frequency is recorded with only 1, 2 or 3 leading significant digits before and 4 - 6 significant digits [including zeroes] after the "M". [Ex. 3M579545 (3.579545MHz), 14M31818 (14.31818MHz), 125M0000 (125MHz)]

Not all performance combinations and frequencies may be available.
Contact your local CTS Representative or CTS Customer Service for availability.

Electrical Specifications

Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Supply Voltage	V_{CC}	-	-0.5	-	7.0	V
Supply Voltage	V_{CC}	±10%	2.97	3.3	3.63	V
Supply Current		Freq Range [tested load noted for TYP values.]				
	I_{CC}	1.0MHz to 20MHz [C_L = 15pF]	-	7	17	mA
		20.001MHz to 40MHz [C_L = 15pF]	-	15	25	
		40.001MHz to 80MHz [CL = 15pF]	-	20	35	
		80.001MHz to 125MHz [C_L = 15pF]	-	30	45	
		125.001MHz to 200MHz [C_L = 15pF]	-	45	65	
Operating Temperature	T_A	-	-20 -40	+25	+70 +85	°C
Storage Temperature	T_{STG}	-	-40	-	+100	°C

Frequency Stability

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency Range	f_O	-		1 - 200		MHz
Frequency Stability [Note 1]	$\Delta f/f_O$	-		20, 25, 50 or 100		±ppm
Aging	$\Delta f/f_{25}$	First Year @ +25°C, nominal V_{CC}	-5	±3	5	ppm

1.] Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 1st year aging.

Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output Type	-	-		HCMOS		-
Output Load	C_L	1.0MHz to 50MHz [CMOS Load]	-	15	30	pF
		50.001MHz to 80MHz [CMOS Load]	-	15	15	
		80.001MHz to 200MHz [CMOS Load]	-	15	15	
		1.0MHz to 200MHz [TTL Load]	-	-	10	TTL
Output Voltage Levels	V_{OH}	CMOS Load	$0.9V_{CC}$	-	-	V
		10TTL Load	2.4	-	-	
	V_{OL}	CMOS Load	-	-	$0.1V_{CC}$	
		10TTL Load	-	-	0.4	
Output Current Levels	I_{OH}	V_{OH} = 2.2V, V_{CC} = 3.3V	-	-	-8	mA
	I_{OL}	V_{OL} = 0.4V, V_{CC} = 3.3V	-	-	8	
Output Duty Cycle	SYM	@ 50% Level	45	-	55	%
Rise and Fall Time		@ 10%/90% Levels [tested load noted for TYP values.]				
	T_R, T_F	1.0MHz to 20MHz [C_L = 30pF]	-	8	10	ns
		20.001MHz to 80MHz [C_L = 15pF]	-	5	8	
		80.001MHz to 125MHz [CL = 15pF]	-	2.5	5	
		125.001MHz to 200MHz [C_L = 15pF]	-	-	2	
Start Up Time	T_S	Application of V_{CC}, C_L = 15pF	-	5	10	ms

Electrical Specifications

Output Parameters

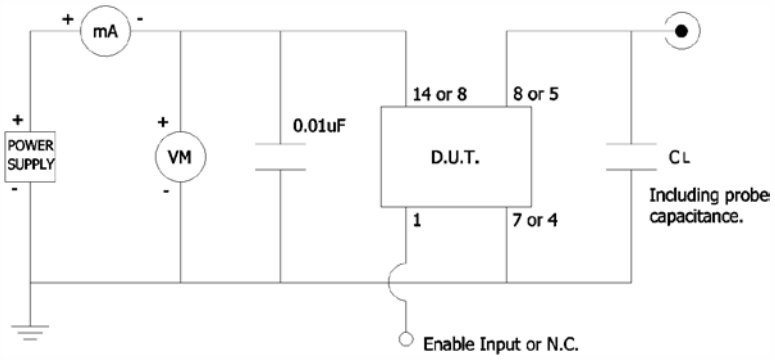
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Enable Function						
Enable Input Voltage	V_{IH}	Pin 1 Logic '1', Output Enabled	2.0	-	-	V
Disable Input Voltage	V_{IL}	Pin 1 Logic '0', Output Disabled	-	-	0.8	V
Disable Current	I_{IL}	Pin 1 Logic '0', Output Disabled	-	-	10	uA
Enable Time	T_{PLZ}	Pin 1 Logic '1', Output Enabled	-	-	100	ns
Phase Jitter, RMS	tjrms	Bandwidth 12 kHz - 20 MHz	-	0.7	1	ps
Period Jitter, RMS	pjrms	-	-	-	5	ps
Period Jitter, pk-pk	pjpk-pk	-	-	-	50	ps

Enable Truth Table

Pin 1	Pin 8 or Pin 5
Logic '1'	Output
Open	Output
Logic '0'	High Imp.

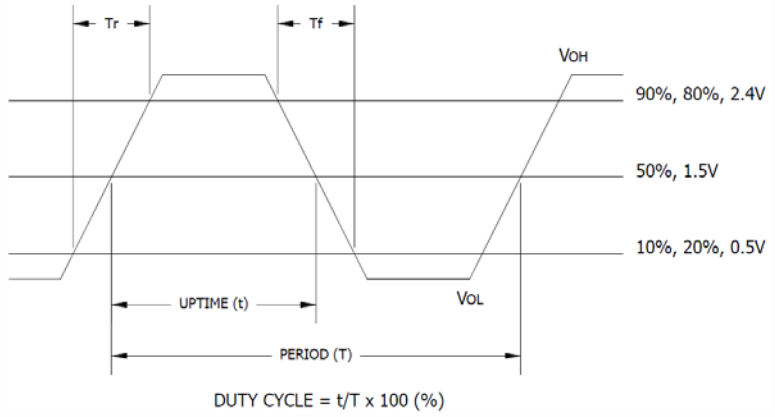
Test Circuit

HCMOS



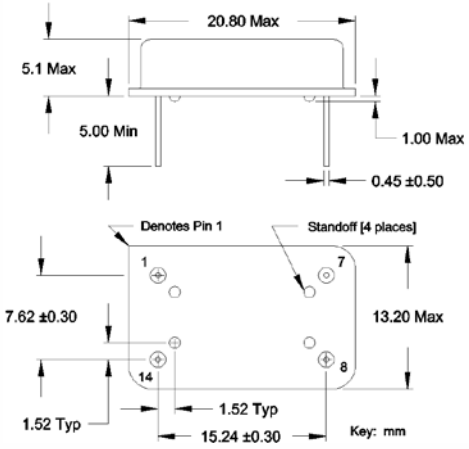
Output Waveform

HCMOS



Mechanical Specifications

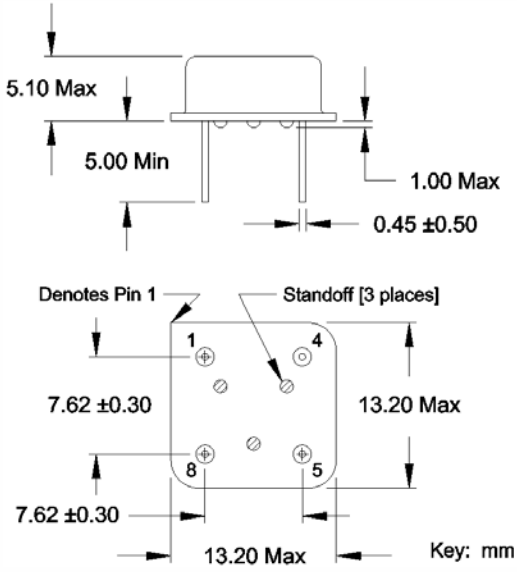
Package Drawing – DIP-14



Marking Information

1. Model Name:
   DIP-14 – MXO45LV or MXO45TLV
   DIP-8 – MXO45HSLV or MXO45HSTLV
2. XXXMXXXXXX – Frequency is recorded with only 1, 2 or 3 leading significant digits before and 4 - 6 significant digits [including zeroes] after the "M". [Ex. 3M579545 (3.579545MHz), 14M31818 (14.31818MHz), 125M0000 (125MHz)]
3. ST – Frequency Stability/Temperature Code. [Refer to Ordering Information]
4. YYWW – Date Code; YY – year, WW – week.
5. ** - Manufacturing Site Code.

Package Drawing - DIP-8



Notes

1. JEDEC termination code (e1). Lead finish is tin-silver-copper [SnAgCu].
2. Reflow conditions per JEDEC J-STD-020; +260°C maximum, 20 seconds.
3. Hand soldering conditions; solder iron temperature +350°C maximum, 10 seconds.
4. MSL = 1.

Pin Assignments

Pin	Symbol	Function
1	EOH	Enable
7 or 4	GND	Circuit & Package Ground
8 or 5	Output	RF Output
14 or 8	V_{CC}	Supply Voltage

Packaging - CTS Approved Methods

Anti-Static Plastic Trays

Typical packing format:

1. 50pcs. per plastic tray.
   Tray size is approximately 180mm x 136mm x 18mm [LxWxH].
2. 2 trays per anti-static bag [100pcs.] or 10 trays per anti-static bag [500pcs.]
   Bag height for 10 trays is approximately 175mm.
3. One anti-static bag per inner cardboard carton.
4. Master-pack multiple inner cartons in a larger outer cardboard carton.
   8 inner cartons [10 trays per carton] per outer carton, is approximately 460mm x 380mm x 400mm [LxWxH].

Anti-Static Foam in Cardboard Carton

Typical packing format:

1. 50pcs. per anti-static foam layer.
2. 2 layers of anti-static foam [100pcs.] per inner cardboard carton.
   Carton size is approximately 170mm x 120mm x 45mm [LxWxH].
3. A foam sheet layer is placed as a buffer on top of each layer containing oscillators.
4. Master-pack multiple inner cartons in a larger outer cardboard carton.
   20 inner cartons [100pcs. per carton] per outer carton, is approximately 550mm x 350mm x 180mm [LxWxH].

Anti-Static Plastic Tubes

Typical packing format:

1. 10pcs. per plastic tube – Full-Size package.
   15pcs. per plastic tube – Half-Size package.
2. Plastic tubes are master packed in cardboard carton.
   Carton is approximately 35mm x 35mm x 20mm [LxWxH].