

## General Description

The MAX14745 is a battery-charge-management solution ideal for low-power wearable applications. The device includes a linear battery charger with a smart power selector and several power-optimized peripherals. The MAX14745 features two ultra-low quiescent current buck regulators and three ultra-low quiescent current low-dropout (LDO) linear regulators, providing up to five regulated voltages, each with an ultra-low quiescent current, allows designers to minimize power consumption and extend battery life in 24/7 operation devices, such as those in the wearable market.

The battery charger features a smart power selector that allows operation on a dead battery when connected to a power source. To avoid overloading a power adapter, the input current to the smart power selector is limited based on an I<sup>2</sup>C register setting. If the charger power source is unable to supply the entire system load, the smart power control circuit supplements the system load with current from the battery. The charger also supports temperature dependent charge currents.

The two synchronous, high-efficiency step-down buck regulators feature a variable frequency mode for increased efficiency during light-load operation. The output voltage of these regulators can be programmed through I<sup>2</sup>C with the default preconfigured. The buck regulators can support dynamic voltage scaling to further improve system power consumption.

The three configurable LDOs each have a dedicated input pin. Each LDO regulator output voltage can be programmed through I<sup>2</sup>C with the default preconfigured. The linear regulators can also be configured to operate as power switches that may be used to disconnect the quiescent load of the system peripherals.

The MAX14745 features a programmable power controller that allows the device to be configured for applications that require the device be in a true-off, or always-on, state. The controller also provides a delayed reset signal and voltage sequencing.

The MAX14745 is available in a 36-bump, 0.4mm pitch, 2.72mm x 2.47mm wafer-level package (WLP).

## Benefits and Features

- Extend System Use Time Between Battery Charging
  - Dual Ultra-Low-I<sub>Q</sub> 200mA Buck Regulators
    - Output Programmable from 0.8V to 2.375V and 0.8V to 3.95V
    - 0.9μA (typ) Quiescent Current (Buck 1)
    - Optional Fixed Peak-Current Mode to Optimize Ripple Frequency in Noise-Sensitive Applications
  - Three Ultra-Low-I<sub>Q</sub> 100mA LDOs
  - LDO1
    - Output Programmable from 0.8V to 3.6V
    - 0.6μA (typ) Quiescent Current
    - 2.7V to 5.5V Input with Dedicated Pin
  - LDO2/3
    - Output Programmable from 0.9V to 4V
    - 1μA (typ) Quiescent Current
    - 1.71V to 5.5V Input with Dedicated Pin
- Easy-to-Implement Li+ Battery Charging
  - Smart Power Selector
  - 28V/-5.5V Tolerant Input
  - Thermistor Monitor
- Minimize Solution Footprint Through High Integration
  - Provides Five Regulated Voltage Rails
  - Switch Mode Option on Each LDO
- Optimize System Control
  - Monitors Pushbutton for Ultra-Low Power Mode
  - Power-On Reset Delay and Voltage Sequencing
  - On-Chip Voltage Monitor Multiplexer

## Applications

- Wearable Electronics
- Fitness Monitors
- Rechargeable IoT devices

[Ordering Information](#) appears at end of data sheet.

---

**TABLE OF CONTENTS**


---

General Description . . . . .	1
Benefits and Features . . . . .	1
Applications . . . . .	1
Typical Application Circuit . . . . .	5
Absolute Maximum Ratings . . . . .	6
Package Information . . . . .	6
Electrical Characteristics . . . . .	7
Typical Operating Characteristics . . . . .	22
Bump Configuration . . . . .	25
Bump Description . . . . .	25
Block Diagram . . . . .	27
Detailed Description . . . . .	27
Power Regulation . . . . .	27
Power On/Off and Reset Control . . . . .	27
Power Sequencing . . . . .	30
Smart Power Selector . . . . .	31
Thermal Current Regulation . . . . .	31
System Load Switch . . . . .	32
Input Limiter . . . . .	32
Fast-Charge Current Setting . . . . .	33
Thermistor Monitoring with Charger Shutdown . . . . .	33
I <sup>2</sup> C Interface . . . . .	35
I <sup>2</sup> C Addresses . . . . .	35
Thermistor Monitoring with Charger Shutdown . . . . .	36
I <sup>2</sup> C Interface . . . . .	38
Start, Stop, And Repeated Start Conditions . . . . .	38
Slave Address . . . . .	38
Bit Transfer . . . . .	38
Single-Byte Write . . . . .	38
Burst Write . . . . .	39
Single Byte Read . . . . .	39
Burst Read . . . . .	40
Acknowledge Bits . . . . .	40
I <sup>2</sup> C Register Map . . . . .	41
I <sup>2</sup> C Register Descriptions . . . . .	43
Applications Information . . . . .	62

---

## TABLE OF CONTENTS (continued)

---

Inductor Selection . . . . .	62
Output Capacitor Selection . . . . .	62
Input Capacitor Selection . . . . .	62
PCB Layout and Routing . . . . .	62
Ordering Information . . . . .	66
Chip Information . . . . .	66
Revision History . . . . .	67

---

## LIST OF FIGURES

---

Figure 1. Power Function Input Control Modes Flow Diagrams . . . . .	29
Figure 2a. Power-On Sequencing . . . . .	30
Figure 2b. Power-On Sequencing Without Battery . . . . .	31
Figure 3. Smart Power Selector Current/Voltage Behavior . . . . .	32
Figure 4a. Charging Behavior Using Thermistor Monitoring Mode . . . . .	34
Figure 4b. Charging Behavior Using JEITA Monitoring 1 and 2 Modes . . . . .	34
Figure 5a. Charger State Diagram (Thermistor Monitoring with Charger Shutdown) . . . . .	36
Figure 5b. Battery Charger State Diagram (JEITA Monitoring with Charger Shutdown) . . . . .	37
Figure 6. I <sup>2</sup> C START, STOP and REPEATED START Conditions . . . . .	38
Figure 7. Write Byte Sequence . . . . .	38
Figure 8. Burst Write Sequence . . . . .	39
Figure 9. Read Byte Sequence . . . . .	39
Figure 10. Burst Read Sequence . . . . .	40
Figure 11. Acknowledge . . . . .	40

---

## LIST OF TABLES

---

Table 1. Power Function Input Control Modes . . . . .	28
Table 2. Thermistor Monitoring/JEITA Monitoring Enable Control . . . . .	35
Table 3. I <sup>2</sup> C Slave Addresses . . . . .	38
Table 4. ChipId Register (0x00) . . . . .	43
Table 5. ChipRev Register (0x01) . . . . .	43
Table 6. StatusA Register (0x02) . . . . .	43
Table 7. StatusB Register (0x03) . . . . .	44

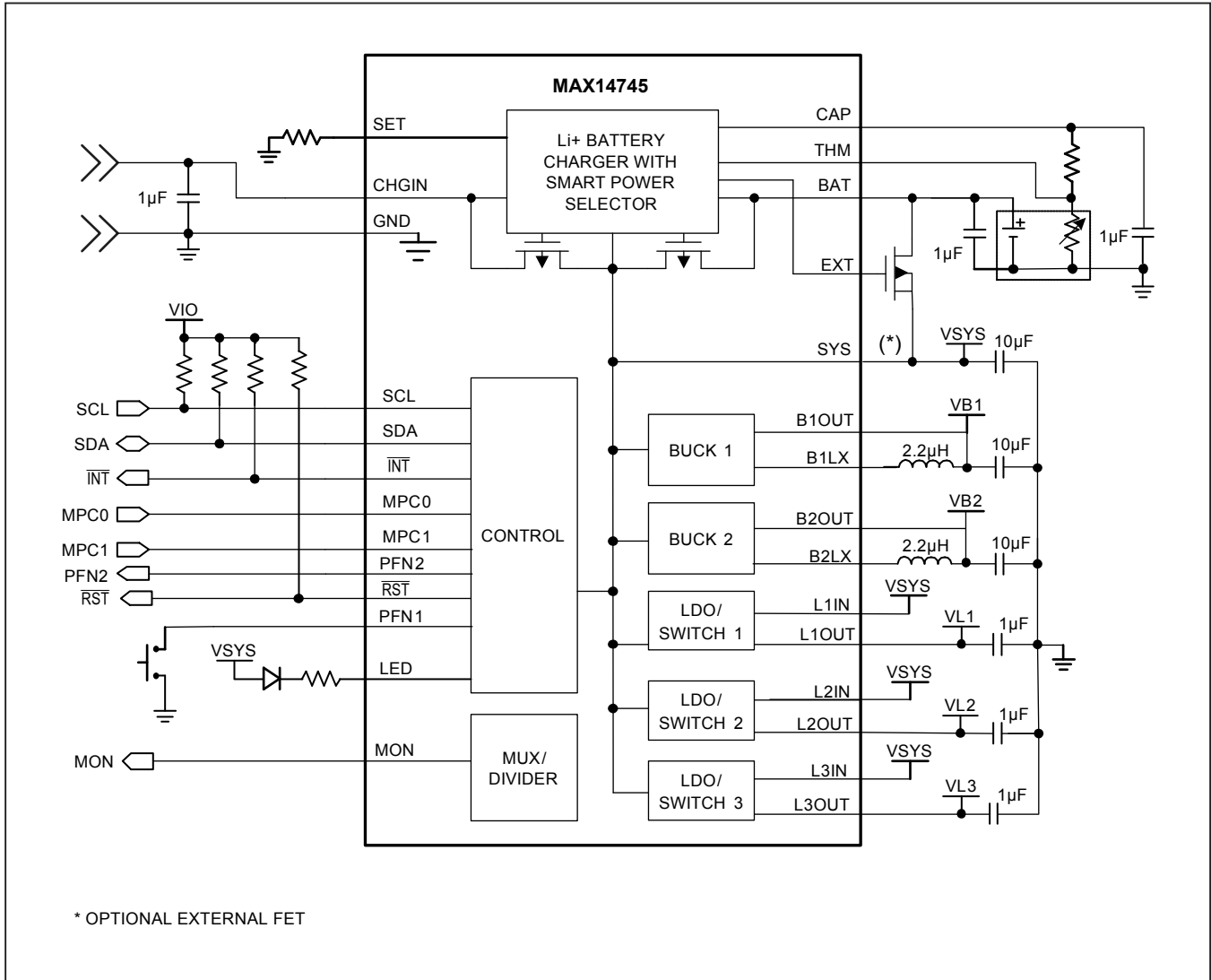
---

**LIST OF TABLES (continued)**


---

Table 8. StatusC Register (0x04) . . . . .	45
Table 9. IntA Register (0x05) . . . . .	46
Table 10. IntB Register (0x06) . . . . .	46
Table 11. IntMaskA Register (0x07) . . . . .	47
Table 12. IntMaskB Register (0x08) . . . . .	48
Table 13. ILimCntl Register (0x09) . . . . .	48
Table 14. ChgCntlA Register (0x0A) . . . . .	49
Table 15. ChgCntlB Register (0x0B) . . . . .	50
Table 16. ChTmr Register (0x0C) . . . . .	51
Table 17. Buck1Cfg Register (0x0D) . . . . .	51
Table 18. Buck1VSet Register (0x0E) . . . . .	52
Table 19. Buck2Cfg Register (0x0F) . . . . .	52
Table 20. Buck2VSet Register (0x10) . . . . .	53
Table 21. Buck1/2ISet Register (0x11) . . . . .	53
Table 22. LDO1Cfg Register (0x12) . . . . .	54
Table 23. LDO1VSet Register (0x13) . . . . .	54
Table 24. LDO2Cfg Register (0x14) . . . . .	55
Table 25. LDO2VSet Register (0x15) . . . . .	55
Table 26. LDO3Cfg Register (0x16) . . . . .	56
Table 27. LDO3VSet Register (0x17) . . . . .	56
Table 28. ThrmCfg Register (0x18) . . . . .	57
Table 29. ThrmCfg Register (0x19) . . . . .	58
Table 30. MONCfg Register (0x1A) . . . . .	58
Table 31. BootCfg Register (0x1B) . . . . .	59
Table 32. PinStat Register (0x1C) . . . . .	59
Table 33. Buck1/2Extra Control Register (0x1D) . . . . .	60
Table 34. PwrCfg Register (0x1E) . . . . .	61
Table 35. PwrCmd Register (0x1F) . . . . .	61
Table 36. Suggested Inductors . . . . .	62
Table 37. Output Capacitor Values* . . . . .	62
Table 38. Register Bit Default Values . . . . .	63
Table 39. Register Default Values . . . . .	65

Typical Application Circuit



### Absolute Maximum Ratings

(Voltages referenced to GND.)

SDA, SCL, THM, RST, SYS, PFN1, PFN2, MPC0, MPC1, INT, MON, BAT, LED, L1IN, L2IN, L3IN.....	-0.3V to +6.0V
B1LX, B2LX, B1OUT, B2OUT, EXT .....	-0.3V to (V <sub>SYS</sub> + 0.3V)
L1OUT .....	-0.3V to (V <sub>L1IN</sub> + 0.3V)
L2OUT .....	-0.3V to (V <sub>L2IN</sub> + 0.3V)
L3OUT .....	-0.3V to (V <sub>L3IN</sub> + 0.3V)
CHGIN .....	-6V to +30V
CAP .....	-0.3V to min ( V <sub>CHGIN</sub>   + 0.3V, +6V)
SET .....	-0.3V to V <sub>BAT</sub> + 0.3V

Continuous Current into CHGIN, BAT, SYS .....	±1000mA
Continuous Current into any other terminal .....	±100mA
Continuous Power Dissipation (multilayer board at +70°C):	
6 x 6 Array 36-Bump 2.72mm x 2.47mm	
0.4mm Pitch WLP (derate 21.70mW/°C).....	1.74W
Operating Temperature Range.....	-40°C to +85°C
Junction Temperature.....	+150°C
Storage Temperature Range .....	-65°C to +150°C
Soldering Temperature (reflow).....	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### Package Information

<b>PACKAGE TYPE: 36 WLP</b>	
Package Code	W362D2+1
Outline Number	<a href="#">21-0897</a>
Land Pattern Number	Refer to <a href="#">Application Note 1891</a>
<b>THERMAL RESISTANCE, FOUR-LAYER BOARD</b>	
Junction to Ambient (θ <sub>JA</sub> )	46°C/W

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

## Electrical Characteristics

( $V_{CHGIN} = 5.0V$ ,  $V_{BAT} = 3.7V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , all registers in their default state, unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>GLOBAL SUPPLY CURRENT (L_IN Connected to SYS)</b>						
Charger Input Current	$I_{CHG}$	All functions disabled		0.26		mA
		Power on, $V_{CHGIN} = 5V$ SYS switch closed, buck regulators enabled, LDO1 enabled, $I_{SYS} = 0A$ , $I_{B\_OUT} = 0A$ , $I_{L\_OUT} = 0A$			1.5	
BAT Input Current	$I_{BAT}$	Power off, $V_{CHGIN} = 0V$ , SYS switch open		0.96	1.7	$\mu A$
		Power on, $V_{CHGIN} = 0V$ SYS switch closed, 2x buck regulators enabled, LDOs disabled. $I_{SYS} = 0A$ , $I_{B\_OUT} = 0A$		2.8	4.3	
		Power on, $V_{CHGIN} = 0V$ SYS switch closed, 2x buck regulators enabled, LDO1 enabled, $I_{SYS} = 0A$ , $I_{B\_OUT} = 0A$ , $I_{L\_OUT} = 0A$		3.5	7	
		Power on, $V_{CHGIN} = 0V$ SYS switch closed, 2x buck regulators enabled, 3x LDOs enabled, $I_{SYS} = 0A$ , $I_{B\_OUT} = 0A$ , $I_{L\_OUT} = 0A$		5.2		
<b>BUCK REGULATOR 1</b> ( $V_{SYS} = +3.7V$ , $L = 2.2\mu H$ , $C = 2.2\mu F$ , $V_{B1OUT} = 1.2V$ )						
Input Voltage	$V_{IN\_BUCK1}$	Input voltage = $V_{SYS}$	2.7		5.5	V
Output Voltage	$V_{OUT\_BUCK1}$	25mV step resolution	0.8		2.375	V
Output UVLO Voltage	$V_{UVLO\_BUCK1}$	<b>Note:</b> For $V_{OUT} < UVLO$ ZC is imposed		0.44	0.7	V
Quiescent Supply Current	$I_{Q\_BUCK1}$	Buck enabled, $I_{B1OUT} = 0mA$ , $V_{SYS} = 3.7V$ , $V_{B1OUT} = 1.2V$ (Note 2)		0.9	1.3	$\mu A$
Dropout Quiescent Supply Current	$I_{QDO\_BUCK1}$	$I_{B1OUT} = 0mA$ , ( $V_{SYS} - V_{OUT}$ ) $\leq 0.1V$		1.1		mA
Shutdown Supply Current with Active Discharge Enabled	$I_{SD\_BUCK1}$	Buck1 disabled, Buck1ActDSC=1.		60		$\mu A$
Output Accuracy	$ACC_{BUCK1}$	$I_{B1OUT} = 1mA$	-3		+3.1	%
Peak-to-Peak Ripple	$V_{PPRIPPLE1}$	Buck1ISet = 100mA, $C_{OUT} = 2.2\mu F$ , $I_{B1OUT} = 1mA$		10		mV
$I_{PEAK}$ Set Range	$I_{PEAK\_BUCK1}$	25mA step resolution set by Buck1ISet[3:0].	50		375	mA

### Electrical Characteristics (continued)

( $V_{CHGIN} = 5.0V$ ,  $V_{BAT} = 3.7V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , all registers in their default state, unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Load Regulation Error	$V_{LOADR\_BUCK1}$	Buck1ISet = 150mA, Buck1IAdptEnb = 0, $I_{B1OUT} = 300mA$		-3		%
Line Regulation Error	$V_{LINER\_BUCK1}$	$V_{B1OUT} = 1.2V$ ; $V_{SYS}$ from 2.7V to 5.5V		3		mV
Maximum Operating Output Current	$I_{OUT\_BUCK1}$	$V_{SYS} = 3.7V$ , Buck1VSet = 1.2V, Buck1ISet = 200mA, Buck1IAdptEnb = 0, load regulation error = -5%	200	500		mA
B1OUT Pulldown Current	$I_{LEAK\_B1OUT}$	Buck1 enabled		110		nA
B1OUT Pulldown Resistance	$R_{PD\_B1OUT}$	Buck1 disabled, $V_{B1OUT} = 1.2V$		12		M $\Omega$
pMOS On-Resistance	$R_{ONP\_BUCK1}$	Buck1FFET = 0		0.27	0.5	$\Omega$
		Buck1FFET = 1		0.55	1	$\Omega$
nMOS On-Resistance	$R_{ONN\_BUCK1}$	Buck1FFET = 0		0.24	0.45	$\Omega$
		Buck1FFET = 1		0.43	0.9	$\Omega$
Freewheeling On-Resistance	$R_{ONFW\_BUCK1}$	$V_{SYS} = 3.7V$ , $V_{B1OUT} = 1.2V$		7.3	13	$\Omega$
Minimum $T_{ON}$	$T_{ON\_MIN}$			40	80	ns
Maximum Duty Cycle	$D_{MAX\_BUCK1}$	Buck1IAdptEnb = 0		98		%
Switching Frequency	$f_{SW\_BUCK1}$	Load regulation error = -3%		3		MHz
Average Current During Short-Circuit to GND	$I_{SHRT\_BUCK1}$	Buck1ISet = 150mA, Buck1IAdptEnb = 0, $V_{B1OUT} = 0V$		100		mA
BLX Leakage Current	$I_{BLX\_BUCK1}$			0.005	1	$\mu A$
Active Discharge Current	$I_{PD\_BUCK1}$	$V_{B1OUT} = 1.2V$		17		mA
Passive Discharge Resistance	$R_{PD\_BUCK1}$	$V_{B1OUT} = 1.2V$		9		k $\Omega$
Full Turn-On Time	$t_{ON\_BUCK1}$	Time from enable to full current capability, Buck1Fst = 0		58		ms
Efficiency	$Eff_{BUCK1}$	$I_{LOAD} = 10mA$ , Buck1ISet = 150mA, Inductor = BOURNS SRP2010-2R2M, $V_{B1OUT} = 1.2V$		87		%
BLX Rising/Falling Slew Rate	$SR_{BLX\_BUCK1}$	Buck1LowEMI = 0		2		V/ns
		Buck1LowEMI = 1		0.5		
Thermal-Shutdown Temperature	$T_{SHDN\_BUCK1}$			140		$^{\circ}C$
Thermal-Shutdown Temperature Hysteresis	$T_{SHDN\_HYST\_BUCK1}$			10		$^{\circ}C$



## Electrical Characteristics (continued)

( $V_{CHGIN} = 5.0V$ ,  $V_{BAT} = 3.7V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , all registers in their default state, unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>BUCK REGULATOR 2</b>						
(V <sub>SYS</sub> = +3.7V, L = 2.2μH, C = 2.2μF, V <sub>B2OUT</sub> = 1.2V)						
Input Voltage	V <sub>IN_BUCK2</sub>	Input voltage = V <sub>SYS</sub>	2.7		5.5	V
Output Voltage	V <sub>OUT_BUCK2</sub>	50mV step resolution	0.8		3.95	V
Output UVLO Voltage	V <sub>UVLO_BUCK2</sub>	<b>Note:</b> For V <sub>OUT</sub> < UVLO ZC is imposed		0.44	0.7	V
Quiescent Supply Current	I <sub>Q_BUCK2</sub>	Buck enabled, I <sub>B2OUT</sub> = 0mA, V <sub>SYS</sub> = 3.7V, V <sub>B2OUT</sub> = 1.2V (Note 2)		1	1.3	μA
Dropout Quiescent Supply Current	I <sub>QDO_BUCK2</sub>	I <sub>B2OUT</sub> = 0mA, V <sub>SYS</sub> – V <sub>B2OUT</sub> ≤ 0.1V		1.1		mA
Shutdown Supply Current with Active Discharge Enabled	I <sub>SD_BUCK2</sub>	Buck1 disabled, Buck2ActDSC = 1.		60		μA
Output Accuracy	ACC <sub>BUCK2</sub>	I <sub>B2OUT</sub> = 1mA, V <sub>B2OUT</sub> < 3.4V	-3		+3.1	%
Peak-to-Peak Ripple	V <sub>PPRIPPLE2</sub>	Buck2ISet = 100mA, C <sub>OUT</sub> = 2.2μF, I <sub>B2OUT</sub> = 1mA		10		mV
I <sub>PEAK</sub> Set Range	I <sub>PEAK_BUCK2</sub>	25mA step resolution set by Buck2ISet[3:0].	50		375	mA
Load Regulation Error	V <sub>LOADR_BUCK2</sub>	Buck2ISet = 150mA, Buck2IAdptEnb = 0, I <sub>B2OUT</sub> = 300mA		-3		%
Line Regulation Error	V <sub>LINER_BUCK2</sub>	V <sub>B2OUT</sub> = 1.2V; V <sub>SYS</sub> from 2.7V to 5.5V		3		mV
Maximum Operating Output Current	I <sub>OUT_BUCK2</sub>	V <sub>SYS</sub> = 3.7V, Buck2VSet = 1.2V, Buck2ISet = 200mA, Buck2IAdptEnb = 0, load regulation = -5%	200	500		mA
B2OUT Pulldown Current	I <sub>LEAK_B2OUT</sub>	Buck2 enabled		220		nA
B2OUT Pulldown Resistance	R <sub>PD_B2OUT</sub>	Buck2 disabled, V <sub>B2OUT</sub> = 1.2V		6		MΩ
pMOS On-Resistance	R <sub>ONP_BUCK2</sub>	Buck2FFET = 0		0.27	0.5	Ω
		Buck2FFET = 1		0.55	1	Ω
nMOS On-Resistance	R <sub>ONN_BUCK2</sub>	Buck2FFET = 0		0.24	0.45	Ω
		Buck2FFET = 1		0.43	0.9	Ω
Freewheeling On-Resistance	R <sub>ONFW_BUCK2</sub>	V <sub>SYS</sub> = 3.7V, V <sub>B2OUT</sub> = 1.2V		7.3	13	Ω

### Electrical Characteristics (continued)

( $V_{CHGIN} = 5.0V$ ,  $V_{BAT} = 3.7V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , all registers in their default state, unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum $T_{ON}$	$T_{ON\_MIN}$			40	80	ns
Maximum Duty Cycle	$D_{MAX\_BUCK2}$	Buck2IAdptEnb = 0		98		%
Switching Frequency	$f_{SW\_BUCK2}$	Load regulation error = -3%		3		MHz
Average Current During Short-Circuit to GND	$I_{SHRT\_BUCK2}$	Buck2ISet = 150mA, Buck2IAdptEnb = 0, $V_{B2OUT} = 0V$		100		mA
BLX Leakage Current	$I_{BLX\_BUCK2}$			0.005	1	$\mu A$
Active Discharge Current	$I_{PD\_BUCK2}$	$V_{B2OUT} = 1.2V$		17		mA
Passive Discharge Resistance	$R_{PD\_BUCK2}$	$V_{B2OUT} = 1.2V$		9		k $\Omega$
Full Turn-On Time	$T_{ON\_BUCK2}$	Time from enable to full current capability, Buck2Fst = 0		58		ms
Efficiency	$Eff_{BUCK2}$	$I_{LOAD} = 10mA$ , Buck2ISet = 150mA, Inductor = BOURNS SRP2010-2R2M, $V_{B2OUT} = 1.2V$		87		%
BLX Rising/Falling Slew Rate	$SR_{BLX\_BUCK2}$	Buck2LowEMI = 0		2		V/ns
		Buck2LowEMI = 1		0.5		
Thermal-Shutdown Temperature	$T_{SHDN\_BUCK2}$			140		$^{\circ}C$
Thermal-Shutdown Temperature Hysteresis	$T_{SHDN\_HYST\_BUCK2}$			10		$^{\circ}C$
<b>LDO1</b> ( $C = 1\mu F$ , unless otherwise noted. Typical values are at $V_{L1IN} = 3.7V$ , with $I_{L1OUT} = 10mA$ , $V_{L1OUT} = 3V$ .)						
Input Voltage	$V_{INLDO1}$	LDO mode		2.7	5.5	V
		Switch mode		1.2	5.5	V
Quiescent Supply Current	$I_{Q\_LDO1}$	LDO enabled, $I_{L1OUT} = 0\mu A$		0.55	4	$\mu A$
		LDO enabled, $I_{L1OUT} = 0\mu A$ , Switch mode		0.45		
Shutdown Supply Current with Active Discharge Enabled	$I_{SD\_LDO1}$	LDO1 disabled. LDO1ActDSC=1.		55		$\mu A$
Maximum Output Current	$I_{L1OUT\_MAX}$			100		mA
Output Voltage	$V_{L1OUT}$			0.8	3.6	V
Output Accuracy	$ACC_{LDO1}$	$V_{L1IN} = (V_{L1OUT} + 0.5V)$ or higher, $I_{L1OUT} = 100\mu A$		-2.7	+2.7	%

### Electrical Characteristics (continued)

( $V_{CHGIN} = 5.0V$ ,  $V_{BAT} = 3.7V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , all registers in their default state, unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Dropout Voltage	$V_{DROP\_LDO1}$	$V_{L1IN} = 3V$ , $I_{L1OUT} = 100mA$ , $LDO1VSet = 3V$			102	mV
Line Regulation Error	$V_{LINEREG\_LDO1}$	$V_{L1IN} = (V_{L1OUT} + 0.5V)$ to 5.5V	-0.12	0.022	+0.12	%/V
Load Regulation Error	$V_{LOADREG\_LDO1}$	$I_{L1OUT} = 100\mu A$ to 100mA		0.002	0.005	%/mA
Line Transient	$V_{LINETRAN\_LDO1}$	$V_{L1IN} = 4V$ to 5V, 200ns rise time		$\pm 36$		mV
		$V_{L1IN} = 4V$ to 5V, 1 $\mu s$ rise time		$\pm 28$		mV
Load Transient	$V_{LOADTRAN\_LDO1}$	$I_{L1OUT} = 0mA$ to 10mA, 200ns rise time		145		mV
		$I_{L1OUT} = 0mA$ to 100mA, 200ns rise time		290		mV
Passive Discharge Resistance	$R_{PD\_LDO1}$		5	10	16	K $\Omega$
Active Discharge Current	$I_{ADL\_LDO1}$	$V_{L1IN} = 3.7V$	7	20	37	mA
Switch Mode Resistance	$R_{ON\_LDO1}$	$V_{L1IN} = 2.7V$ , $I_{L1OUT} = 100mA$		0.5	0.85	$\Omega$
		$V_{L1IN} = 1.8V$ , $I_{L1OUT} = 100mA$		0.76	1.3	
		$V_{L1IN} = 1.2V$ , $I_{L1OUT} = 5mA$		1.7	2.8	
Turn-On Time	$t_{ON\_LDO1}$	$I_{L1OUT} = 0mA$ , time from 10% to 90% of final value		1.6	3.7	ms
		$I_{L1OUT} = 0mA$ , time from 10% to 90% of final value, Switch mode		0.25	0.65	
Short-Circuit Current Limit	$I_{SHRT\_LDO1}$	$V_{L1IN} = 2.7V$ , $V_{L1OUT} = GND$	150	345	550	mA
		$V_{L1IN} = 2.7V$ , $V_{L1OUT} = GND$ , Switch mode	150	335	550	mA
Thermal-Shutdown Temperature	$T_{SHDN\_LDO1}$			150		$^{\circ}C$
Thermal-Shutdown Temperature Hysteresis	$T_{SHDN\_HYST\_LDO1}$			16		$^{\circ}C$
Output Noise	$OUT_{NOISE}$	10Hz to 100kHz, $V_{L1IN} = 5V$ , $V_{L1OUT} = 3.3V$		110		$\mu V_{rms}$
		10Hz to 100kHz, $V_{L1IN} = 5V$ , $V_{L1OUT} = 2.5V$		95		
		10Hz to 100kHz, $V_{L1IN} = 5V$ , $V_{L1OUT} = 1.2V$		60		
		10Hz to 100kHz, $V_{L1IN} = 5V$ , $V_{L1OUT} = 0.8V$		60		

## Electrical Characteristics (continued)

( $V_{CHGIN} = 5.0V$ ,  $V_{BAT} = 3.7V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , all registers in their default state, unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>LDO2</b>						
(C = 1 $\mu$ F, unless otherwise noted. Typical values are at $V_{L2IN} = 3.7V$ , with $I_{L2OUT} = 10mA$ , $V_{L2OUT} = 3V$ .)						
Input Voltage	$V_{INLDO2}$	LDO mode	1.71		5.5	V
		Switch mode	1.2		5.5	V
Quiescent Supply Current	$I_{Q\_LDO2}$	$I_{L2OUT} = 0\mu A$		1	5.1	$\mu A$
		$I_{L2OUT} = 0\mu A$ , Switch mode		0.5		
Quiescent Supply Current in Dropout	$I_{QDO\_LDO2}$	$I_{L2OUT} = 0\mu A$ , $V_{L2IN} = 2.9V$ , $LDO2VSet = 3V$ .		1.8		$\mu A$
Shutdown Supply Current with Active Discharge Enabled	$I_{SD\_LDO2}$	LDO2 disabled. $LDO2ActDSC=1$ .		54		$\mu A$
Maximum Output Current	$I_{L2OUT\_MAX}$	$V_{L2IN} \geq 2.7V$	100			mA
		$V_{L2IN} = 1.8V$ or lower	50			mA
Output Voltage	$V_{L2OUT}$		0.9		4	V
Output Accuracy	$ACC_{LDO2}$	$V_{L2IN} = (V_{L2OUT} + 0.5V)$ or higher, $I_{L2OUT} = 100\mu A$	-2.7		+2.7	%
Dropout Voltage	$V_{DROP\_LDO2}$	$V_{L2IN} = 3V$ , $I_{L2OUT} = 100mA$ , $LDO2VSet = 3V$			100	mV
Line Regulation Error	$V_{LINEREG\_LDO2}$	$V_{L2IN} = (V_{L2OUT} + 0.5V)$ to 5.5V	-0.4	+0.05	+0.4	%/V
Load Regulation Error	$V_{LOADREG\_LDO2}$	$I_{L2OUT} = 100\mu A$ to 100mA		0.001	0.005	%/mA
Line Transient	$V_{LINETRAN\_LDO2}$	$V_{L2IN} = 4V$ to 5V, 200ns rise time		$\pm 35$		mV
		$V_{L2IN} = 4V$ to 5V, 1 $\mu s$ rise time		$\pm 25$		mV
Load Transient	$V_{LOADTRAN\_LDO2}$	$I_{L2OUT} = 0mA$ to 10mA, 200ns rise time		100		mV
		$I_{L2OUT} = 0mA$ to 100mA, 200ns rise time		200		mV
Passive Discharge Resistance	$R_{PD\_LDO2}$		5	10	16	K $\Omega$
Active Discharge Current	$I_{ADL\_LDO2}$	$V_{L2IN} = 3.7V$	7	20	37	mA
Switch Mode Resistance	$R_{ON\_LDO2}$	$V_{L2IN} = 2.7V$ , $I_{L2OUT} = 100mA$		0.46	0.76	$\Omega$
		$V_{L2IN} = 1.8V$ , $I_{L2OUT} = 50mA$		0.7	1.15	
		$V_{L2IN} = 1.2V$ , $I_{L2OUT} = 5mA$		1.7	2.6	
Turn-On Time	$t_{ON\_LDO2}$	$I_{L2OUT} = 0mA$ , time from 10% to 90% of final value		1.5	3.7	ms
		$I_{L2OUT} = 0mA$ , time from 10% to 90% of final value, Switch mode		0.25	0.65	

### Electrical Characteristics (continued)

( $V_{CHGIN} = 5.0V$ ,  $V_{BAT} = 3.7V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , all registers in their default state, unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Short-Circuit Current Limit	$I_{SHRT\_LDO2}$	$V_{L2IN} = 2.7V$ , $V_{L2OUT} = GND$	140	340	600	mA
		$V_{L2IN} = 2.7V$ , $V_{L2OUT} = GND$ , Switch mode	140	330	600	mA
Thermal-Shutdown Temperature	$T_{SHDN\_LDO2}$			150		$^{\circ}C$
Thermal-Shutdown Temperature Hysteresis	$T_{SHDN\_HYST\_LDO2}$			21		$^{\circ}C$
Output Noise	$OUT_{NOISE}$	10Hz to 100kHz, $V_{L2IN} = 5V$ , $V_{L2OUT} = 3.3V$		150		$\mu V_{rms}$
		10Hz to 100kHz, $V_{L2IN} = 5V$ , $V_{L2OUT} = 2.5V$		125		
		10Hz to 100kHz, $V_{L2IN} = 5V$ , $V_{L2OUT} = 1.2V$		90		
		10Hz to 100kHz, $V_{L2IN} = 5V$ , $V_{L2OUT} = 0.9V$		80		
L2IN UVLO	$V_{UVLO\_LDO2}$	$V_{L2IN}$ Falling	1.14	1.38		V
		$V_{L2IN}$ Rising		1.4	1.64	
<b>LDO3</b>						
(C = 1 $\mu F$ , unless otherwise noted. Typical values are at $V_{L3IN} = 3.7V$ , with $I_{L3OUT} = 10mA$ , $V_{L3OUT} = 3V$ .)						
Input Voltage	$V_{INLDO3}$	LDO mode	1.71		5.5	V
		Switch mode	1.2		5.5	V
Quiescent Supply Current	$I_{Q\_LDO3}$	$I_{L3OUT} = 0\mu A$		1	5.1	$\mu A$
		$I_{L3OUT} = 0\mu A$ , Switch mode		0.5		
Quiescent Supply Current in Dropout	$I_{QDO\_LDO3}$	$I_{L3OUT} = 0\mu A$ , $V_{L3IN} = 2.9V$ , LDO3VSet = 3V.		1.8		$\mu A$
Shutdown Supply Current with Active Discharge Enabled	$I_{SD\_LDO3}$	LDO3 disabled. LDO3ActDSC=1.		54		$\mu A$
Maximum Output Current	$I_{L3OUT\_MAX}$	$V_{L3IN} \geq 2.7V$	100			mA
		$V_{L3IN} = 1.8V$ or lower	50			mA
Output Voltage	$V_{L3OUT}$		0.9		4	V
Output Accuracy	$ACC_{LDO3}$	$V_{L3IN} = (V_{L3OUT} + 0.5V)$ or higher, $I_{L3OUT} = 100\mu A$	-2.7		+2.7	%
Dropout Voltage	$V_{DROP\_LDO3}$	$V_{L3IN} = 3V$ , $I_{L3OUT} = 100mA$ , LDO3VSet = 3V			100	mV

### Electrical Characteristics (continued)

( $V_{CHGIN} = 5.0V$ ,  $V_{BAT} = 3.7V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , all registers in their default state, unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Line Regulation Error	$V_{LINEREG\_LDO3}$	$V_{L3IN} = (V_{L3OUT} + 0.5V)$ to 5.5V	-0.4	+0.05	+0.4	%/V
Load Regulation Error	$V_{LOADREG\_LDO3}$	$I_{L3OUT} = 100\mu A$ to 100mA		0.001	0.005	%/mA
Line Transient	$V_{LINETRAN\_LDO3}$	$V_{L3IN} = 4V$ to 5V, 200ns rise time		$\pm 35$		mV
		$V_{L3IN} = 4V$ to 5V, 1 $\mu s$ rise time		$\pm 25$		mV
Load Transient	$V_{LOADTRAN\_LDO3}$	$I_{L3OUT} = 0mA$ to 10mA, 200ns rise time		100		mV
		$I_{L3OUT} = 0mA$ to 100mA, 200ns rise time		200		mV
Passive Discharge Resistance	$R_{PD\_LDO3}$		5	10	16	K $\Omega$
Active Discharge Current	$I_{ADL\_LDO3}$	$V_{L3IN} = 3.7V$	7	20	37	mA
Switch Mode Resistance	$R_{ON\_LDO3}$	$V_{L3IN} = 2.7V$ , $I_{L3OUT} = 100mA$		0.46	0.76	$\Omega$
		$V_{L3IN} = 1.8V$ , $I_{L3OUT} = 100mA$		0.7	1.15	
		$V_{L3IN} = 1.2V$ , $I_{L3OUT} = 5mA$		1.7	2.6	
Turn-On Time	$t_{ON\_LDO3}$	$I_{L3OUT} = 0mA$ , time from 10% to 90% of final value		1.5	3.7	ms
		$I_{L3OUT} = 0mA$ , time from 10% to 90% of final value, Switch mode		0.25	0.65	
Short-Circuit Current Limit	$I_{SHRT\_LDO3}$	$V_{L3IN} = 2.7V$ , $V_{L3OUT} = GND$	140	340	600	mA
		$V_{L3IN} = 2.7V$ , $V_{L3OUT} = GND$ , Switch mode	140	330	600	mA
Thermal-Shutdown Temperature	$T_{SHDN\_LDO3}$			150		$^{\circ}C$
Thermal-Shutdown Temperature Hysteresis	$T_{SHDN\_HYST\_LDO3}$			21		$^{\circ}C$
Output Noise	OUTNOISE	10Hz to 100kHz, $V_{L3IN} = 5V$ , $V_{L3OUT} = 3.3V$		150		$\mu V_{rms}$
		10Hz to 100kHz, $V_{L3IN} = 5V$ , $V_{L3OUT} = 2.5V$		125		
		10Hz to 100kHz, $V_{L3IN} = 5V$ , $V_{L3OUT} = 1.2V$		80		
		10Hz to 100kHz, $V_{L3IN} = 5V$ , $V_{L3OUT} = 0.9V$		60		
L3IN UVLO	$V_{UVLO\_LDO3}$	$V_{L3IN}$ Falling	1.14	1.38		V
		$V_{L3IN}$ Rising		1.4	1.64	

## Electrical Characteristics (continued)

( $V_{CHGIN} = 5.0V$ ,  $V_{BAT} = 3.7V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , all registers in their default state, unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>CHGIN TO SYS PATH</b> ( $V_{CHGIN} = 5.0V$ , $V_{SYS} = V_{SYS\_REG}$ )						
Allowed CHGIN Input Voltage Range	$V_{CHGIN\_RNG}$		-5.5		28	V
$V_{CHGIN}$ Detect Threshold	$V_{CHGIN\_DET}$	Rising	3.8	3.9	4.1	V
		Falling	3.0	3.1	3.2	
$V_{CHGIN}$ Overvoltage Threshold	$V_{CHGIN\_OV}$	Rising	7.2	7.5	7.8	V
$V_{CHGIN}$ Overvoltage Threshold Hysteresis	$V_{CHGIN\_OV\_HYS}$			200		mV
$V_{CHGIN}$ Valid Trip Point	$V_{CHGIN\_SYS\_TP}$	$V_{CHGIN} - V_{SYS}$ , Rising, $V_{BAT} = 4V$	+30	+145	+290	mV
$V_{CHGIN}$ Valid Trip Point Hysteresis	$V_{CHGIN\_SYS\_TP\_HYS}$			275		mV
Input Limiter Current	$I_{LIM}$	$ILimCntl[1:0] = 00$		0		mA
		$ILimCntl[1:0] = 01$		90	100	
		$ILimCntl[1:0] = 10$		450	550	
		$ILimCntl[1:0] = 11$		1000		
Internal CAP Regulator	$V_{CAP}$	$V_{CHGIN} = 5V$	3.9	4.2	4.7	V
CHGIN-SYS Regulation Voltage	$V_{CHGIN\_SYS}$	$V_{CHGIN} = 4V$ , $I_{SYS} = 1mA$		40		mV
CHGIN to SYS On-Resistance	$R_{CHGIN\_SYS}$	$V_{CHGIN} = 4.4V$ , $I_{SYS} = 500mA$		370	660	m $\Omega$
Thermal-Shutdown Temperature	$T_{CHGIN\_SHDN}$	(Note 3)		+150		$^{\circ}C$
Thermal-Shutdown Temperature Hysteresis	$T_{CHGIN\_SHDN\_HYS}$			30		$^{\circ}C$
Input Current Soft-Start Time	$t_{SFST\_LIM}$			1		ms
Internal Supply Switchover Threshold	$V_{CCINT\_TH}$	$V_{CHGIN} = V_{CAP}$ rising, $V_{BAT} = 4.2V$	2.5	2.8	3.0	V

### Electrical Characteristics (continued)

( $V_{CHGIN} = 5.0V$ ,  $V_{BAT} = 3.7V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , all registers in their default state, unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>SYS, BATTERY, AND VCCINT UVLOs</b>						
SYS UVLO Threshold	$V_{SYSUVLO\_R}$	Rising		2.64	2.69	V
	$V_{SYSUVLO\_F}$	Falling	2.57	2.62	2.67	V
SYS UVLO Threshold Hysteresis	$V_{SYSUVLO\_HYS}$	Hysteresis		26		mV
SYS UVLO Falling Debounce Time	$t_{SYSUVLO\_FDEB}$	SYS Falling		20		$\mu s$
VCCINT UVLO Threshold (POR)	$V_{UVLO}$	VCCINT Rising	0.8	1.82	2.6	V
VCCINT UVLO Threshold Hysteresis	$V_{UVLO\_HYS}$			140		mV
BAT UVLO Threshold	$V_{BAT\_UVLO}$	Rising (Valid only when CHGIN is present. When $V_{BAT} < V_{BAT\_UVLO}$ , the BAT-SYS switch opens and BAT is connected to SYS through a diode.)	1.9	2.05	2.2	V
BAT UVLO Threshold Hysteresis	$V_{BAT\_UVLO\_HYS}$	Hysteresis		50		mV
<b>BATTERY CHARGER (See Figure 5a and Figure 5b)</b>						
(V <sub>BAT</sub> = 4.2V. Typical values are at V <sub>CHGIN</sub> = 5.0V, V <sub>SYS</sub> = V <sub>SYS_REG</sub> )						
Allowed BAT Voltage Range	$V_{BAT\_RNG}$		0		5.5	V
BAT to SYS On-Resistance	$R_{BAT-SYS}$	$V_{BAT} = 4.2V$ , $I_{BAT} = 300mA$		80	140	m $\Omega$
Current Reduce Thermal Threshold Temperature	$T_{CHG\_LIM}$	(Note 4)		120		$^{\circ}C$
BAT-to-SYS Switch-On Threshold	$V_{BAT-SYS-ON}$	SYS falling	10	22	35	mV
BAT-to-SYS Switch-Off Threshold	$V_{BAT-SYS-OFF}$	SYS rising	-3	-1.5	0	mV
SYS-BAT Regulation Voltage	$V_{SYS\_REG}$	$V_{CHGIN} = 5V$ , $I_{SYS} = 1mA$	$V_{BatReg} + 140mV$	$V_{BatReg} + 200mV$	$V_{BatReg} + 260mV$	V



### Electrical Characteristics (continued)

( $V_{CHGIN} = 5.0V$ ,  $V_{BAT} = 3.7V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , all registers in their default state, unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYS Threshold Voltage Charger Limiting Current (Note 5)	$V_{SYS\_LIM}$	SysMin = 000, $V_{BAT} > 3.6V$		$V_{BAT} + 0.1$		V
		SysMin = 000, $V_{BAT} < 3.4V$		3.6		
		SysMin = 001, $V_{BAT} < 3.4V$		3.7		
		SysMin = 010, $V_{BAT} < 3.4V$		3.8		
		SysMin = 011, $V_{BAT} < 3.4V$		3.9		
		SysMin = 100, $V_{BAT} < 3.4V$	3.86	4	4.14	
		SysMin = 101, $V_{BAT} < 3.4V$		4.1		
		SysMin = 110, $V_{BAT} < 3.4V$		4.2		
		SysMin = 111, $V_{BAT} < 3.4V$		4.3		
Charger Current Soft-Start Time	$t_{CHG\_SOFT}$			1		ms
<b>PRECHARGE</b>						
Precharge Current	$I_{PCHG}$	$IPChg = 00$		5		% $I_{FChg}$
		$IPChg = 01$	9	10	11	
		$IPChg = 10$		20		
		$IPChg = 11$		30		
Prequalification Threshold	$V_{BAT\_PChg}$	$VPChg = 000$		2.1		V
		$VPChg = 001$	2.15	2.25	2.35	
		$VPChg = 010$		2.40		
		$VPChg = 011$		2.55		
		$VPChg = 100$		2.7		
		$VPChg = 101$		2.85		
		$VPChg = 110$		3.0		
		$VPChg = 111$		3.15		
Prequalification Threshold Hysteresis	$V_{BAT\_PChg\_HYS}$			90		mV

### Electrical Characteristics (continued)

( $V_{CHGIN} = 5.0V$ ,  $V_{BAT} = 3.7V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , all registers in their default state, unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>FAST CHARGE</b>							
SET Current Gain Factor	$K_{SET}$			2000		A/A	
SET Regulation Voltage	$V_{SET}$			1		V	
Fast-Charge Current	$I_{FChg}$	$R_{SET} = 400k\Omega$		5		mA	
		$R_{SET} = 40k\Omega$	45	50	55		
		$R_{SET} = 4k\Omega$	450	500	550		
Fast-Charge Current Accuracy (Note 6)	$I_{FChg\_ACC}$	$R_{SET}$ Range = 4k $\Omega$ to 40k $\Omega$	-10		+10	%	
<b>MAINTAIN CHARGE</b>							
Charge Done Qualification	$I_{Chg\_DONE}$	ChgDone = 00		5		% $I_{FChg}$	
		ChgDone = 01	8.5	10	11.5		
		ChgDone = 10		20			
		ChgDone = 11		30			
BAT Regulation Voltage (Note 7)	$V_{BatReg}$	BatReg = 0000		4.05		V	
		BatReg = 0001		4.10			
		BatReg = 0010		4.15			
		BatReg = 0011	$T_A = +25^{\circ}C$	4.179	4.2		4.221
			$T_A = 0$ to $+45C$	4.168	4.2		4.232
		BatReg = 0100		4.25			
		BatReg = 0101		4.3			
		BatReg = 0110		4.35			
		BatReg = 0111		4.4			
		BatReg = 1000		4.45			
		BatReg = 1001		4.5			
		BatReg = 1010		4.55			
		BatReg = 1011		4.6			
BAT Recharge Threshold	$V_{BatReChg}$	BatReChg = 00		$V_{BatReg} - 70$		mV	
		BatReChg = 01		$V_{BatReg} - 120$			
		BatReChg = 10		$V_{BatReg} - 170$			
		BatReChg = 11		$V_{BatReg} - 220$			

## Electrical Characteristics (continued)

( $V_{CHGIN} = 5.0V$ ,  $V_{BAT} = 3.7V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , all registers in their default state, unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>CHARGER TIMER</b>						
Maximum Prequalification Time	$t_{PChg}$	PChgTmr = 00		30		min
		PChgTmr = 01		60		
		PChgTmr = 10		120		
		PChgTmr = 11		240		
Maximum Fast-Charge Time	$t_{FChg}$	FChgTmr = 00		75		min
		FChgTmr = 01		150		
		FChgTmr = 10		300		
		FChgTmr = 11		600		
Maintain-Charge Time	$t_{TOChg}$	TOChgTmr = 00		0		min
		TOChgTmr = 01		15		
		TOChgTmr = 10		30		
		TOChgTmr = 11		60		
Timer Accuracy	$t_{CHG\_ACC}$		-10		+10	%
Timer Extend Threshold	TIMEXD_THRES	If charge current is reduced due to ILIM or TDIE this is the percentage of charge current below which timer clock operates at half speed		50		% $I_{FChg}$
Timer Suspend Threshold	TIMSUS_THRES	If charge current is reduced due to ILIM or TDIE this is the percentage of charge current below which timer clock pauses		20		% $I_{FChg}$
<b>THERMISTOR MONITOR AND NTC DETECTION</b>						
THM Hot Threshold	$T_4$	$V_{THM}$ falling, MAX14745A/ MAX14745C	30.9	32.9	34.9	%CAP
		$V_{THM}$ falling, MAX14745D/ MAX14745E	21.3	23.3	25.3	
THM Warm Threshold	$T_3$	$V_{THM}$ falling, MAX14745A/ MAX14745C	48	50	52	
		$V_{THM}$ falling, MAX14745D/ MAX14745E	30.9	32.9	34.9	
THM Cool Threshold	$T_2$	$V_{THM}$ rising	62.5	64.5	66.5	
THM Cold Threshold	$T_1$	$V_{THM}$ rising	71.9	73.9	75.9	
THM Disable Threshold	THMDIS	$V_{THM}$ rising	91	93	95	
THM Threshold Hysteresis	THMHYS			60		
THM Input Leakage	$I_{LKG\_THM}$		-1		1	$\mu A$

## Electrical Characteristics (continued)

( $V_{CHGIN} = 5.0V$ ,  $V_{BAT} = 3.7V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , all registers in their default state, unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>START UP TIMING (See Figure 2)</b>						
Boot Delay	$t_{RST}$	BootDly = 00		80		ms
		BootDly = 01		120		
		BootDly = 10		220		
		BootDly = 11		420		
Boot Delay Timer Accuracy	$t_{RST\_ACC}$		-10		10	%
<b>DIGITAL SIGNALS</b>						
Input Logic-High (SDA, SCL, MPC0, MPC1, PFN1, PFN2)	$V_{IH}$		1.4			V
Input Logic-Low (SDA, SCL, MPC0, MPC1, PFN1, PFN2)	$V_{IL}$				0.5	V
Output Logic-Low (SDA, $\overline{RST}$ , $\overline{INT}$ , LED, PFN2)	$V_{OL}$	$I_{OL} = 4mA$			0.4	V
High Level Leakage Current (SDA, $\overline{RST}$ , $\overline{INT}$ , LED, PFN2)	$I_{LK}$				1	$\mu A$
SCL Clock Frequency	$f_{SCL}$				400	kHz
Bus Free Time Between a STOP and START Condition	$t_{BUF}$		1.3			$\mu s$
START Condition (Repeated) Hold Time	$t_{HD:STA}$	(Note 8)	0.6			$\mu s$
Low Period of SCL Clock	$t_{LOW}$		1.3			$\mu s$
High Period of SCL Clock	$t_{HIGH}$		0.6			$\mu s$
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			$\mu s$
Data Hold Time	$t_{HD:DAT}$	(Note 9)	0		0.9	$\mu s$
Data Setup Time	$t_{SU:DAT}$	(Note 9)	100			ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			$\mu s$
Spike Pulse Widths Suppressed by Input Filter	$t_{SP}$	(Note 10)		50		ns

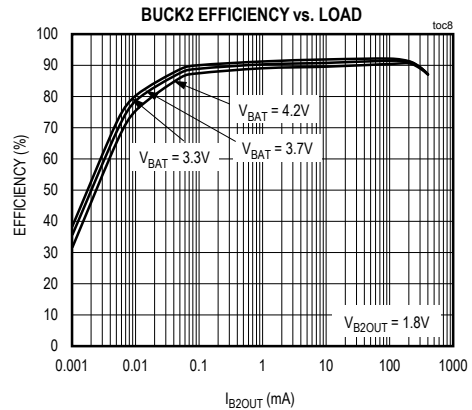
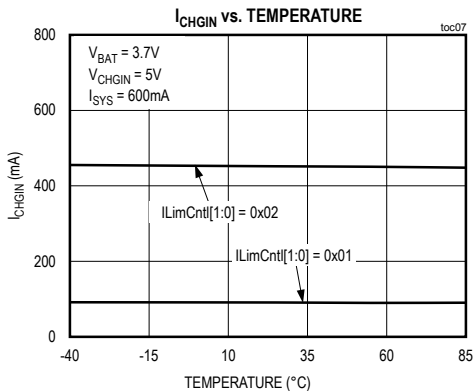
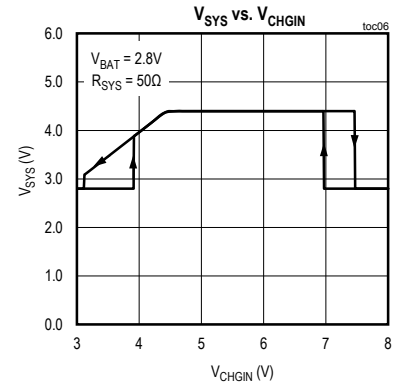
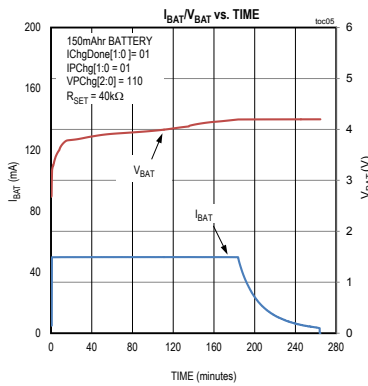
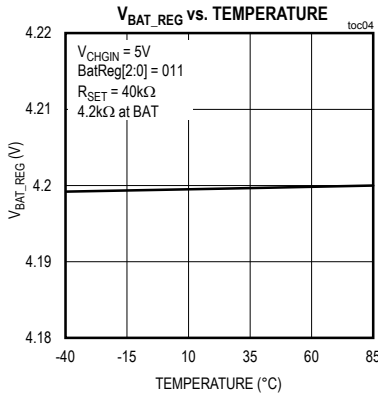
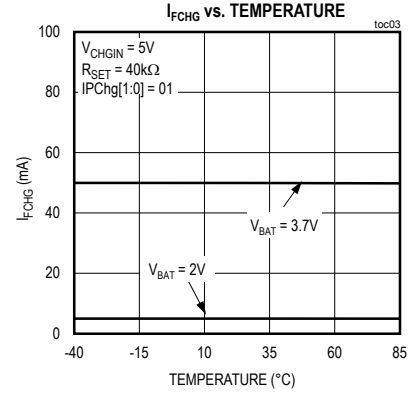
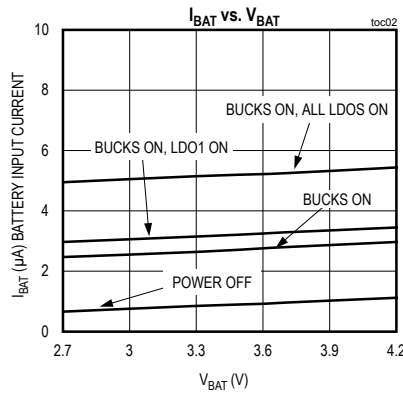
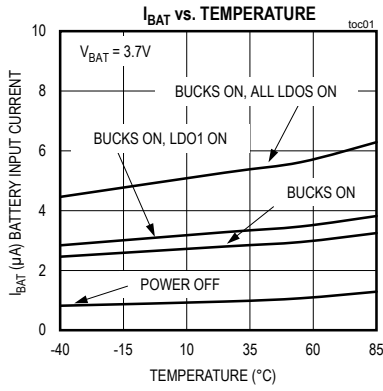
## Electrical Characteristics (continued)

( $V_{\text{CHGIN}} = 5.0\text{V}$ ,  $V_{\text{BAT}} = 3.7\text{V}$ ,  $T_{\text{A}} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , all registers in their default state, unless otherwise noted. Typical values are at  $T_{\text{A}} = +25^{\circ}\text{C}$ .) (Note 1)

- Note 1:** All devices are 100% production tested at  $T_{\text{A}} = +25^{\circ}\text{C}$ . Limits over the operating temperature range guaranteed by design.
- Note 2:** This value is included in the  $I_{\text{BAT}}$  quiescent current values for the ON states.
- Note 3:** When the die temperature exceeds  $T_{\text{CHGIN\_SHDN}}$ , the CHGIN to SYS path opens, and the charger is turned off.
- Note 4:** When the die temperature exceeds  $T_{\text{CHG\_LIM}}$ , the charger current starts to decrease.
- Note 5:** This is the threshold at which the charger starts to limit the current due to SYS dropping; if  $V_{\text{SYS}}$  drops below this value the charger will not move to maintain charge.
- Note 6:** Fast charge current accuracy tested only at 50mA and 500mA, all other values guaranteed by design.
- Note 7:** Values over temperature are not production tested and guaranteed by characterization.
- Note 8:**  $f_{\text{SCL}}$  must meet the minimum clock low time plus the rise/fall times.
- Note 9:** The maximum  $t_{\text{HD:DAT}}$  has to be met only if the device does not stretch the low period ( $t_{\text{LOW}}$ ) of the SCL signal.
- Note 10:** Filters on SDA and SCL suppress noise spikes at the input buffers and delay the sampling instant.

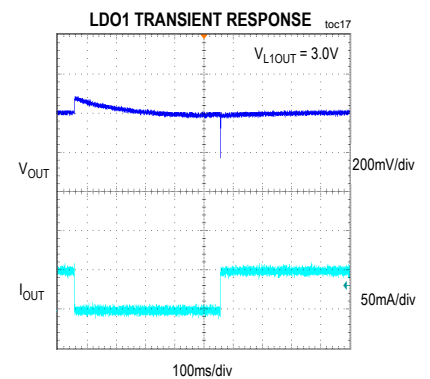
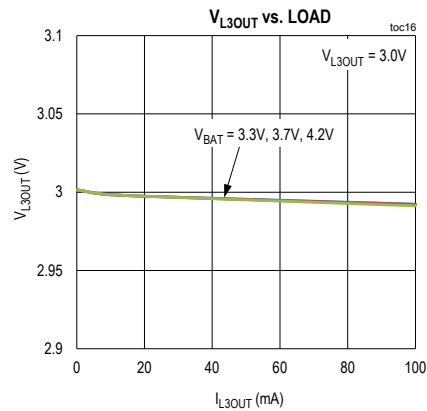
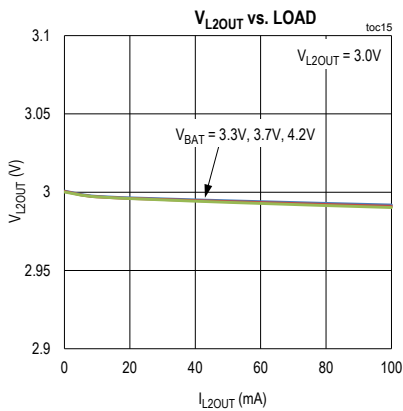
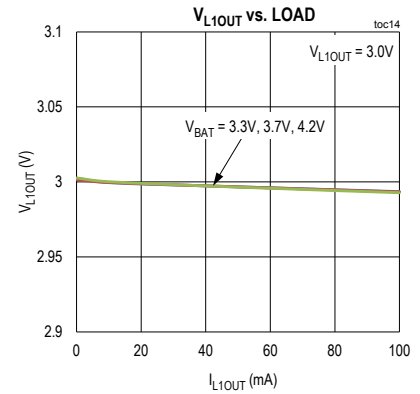
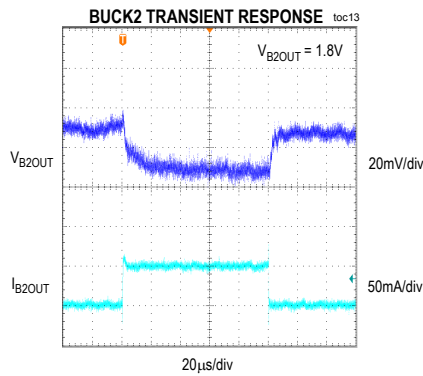
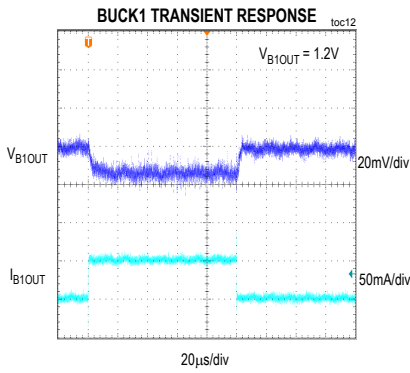
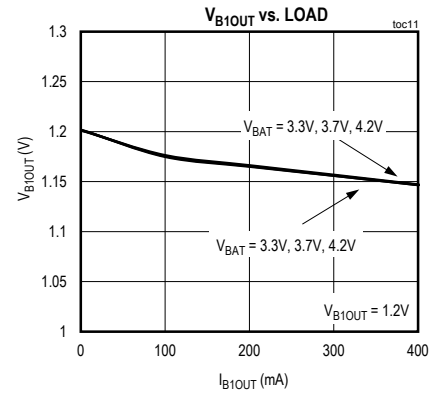
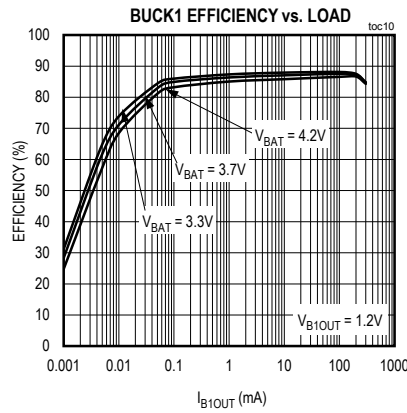
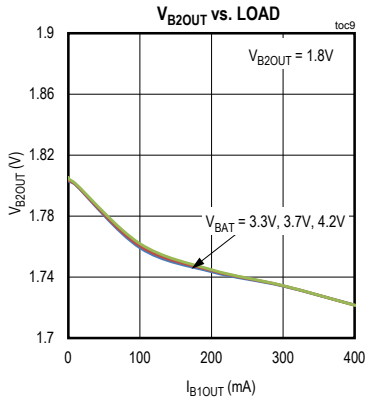
Typical Operating Characteristics

( $V_{BAT} = 3.7V$ ,  $V_{CHGIN} = 0V$ , registers in their default state,  $T_A = +25^\circ C$ , unless otherwise noted.)



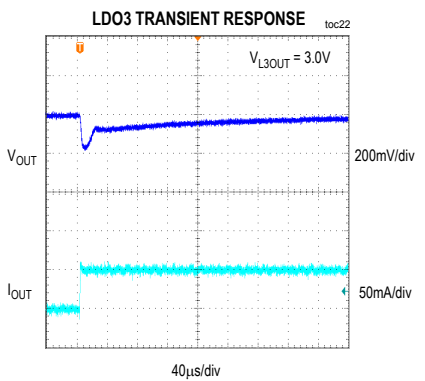
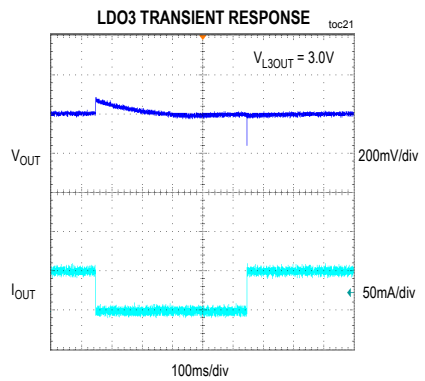
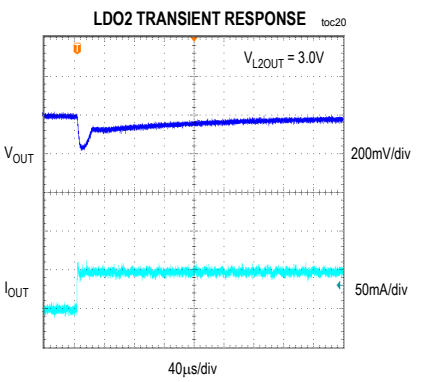
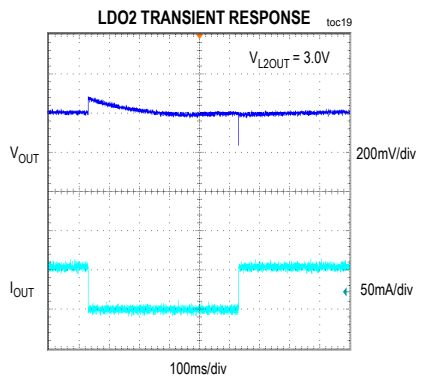
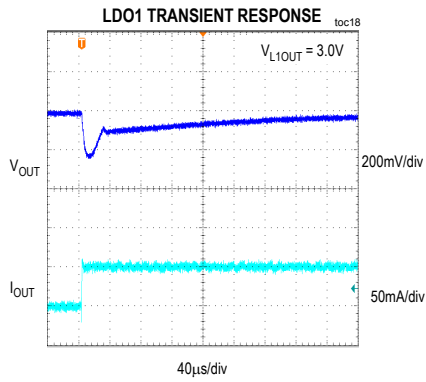
Typical Operating Characteristics (continued)

( $V_{BAT} = 3.7V$ ,  $V_{CHGIN} = 0V$ , registers in their default state,  $T_A = +25^\circ C$ , unless otherwise noted.)



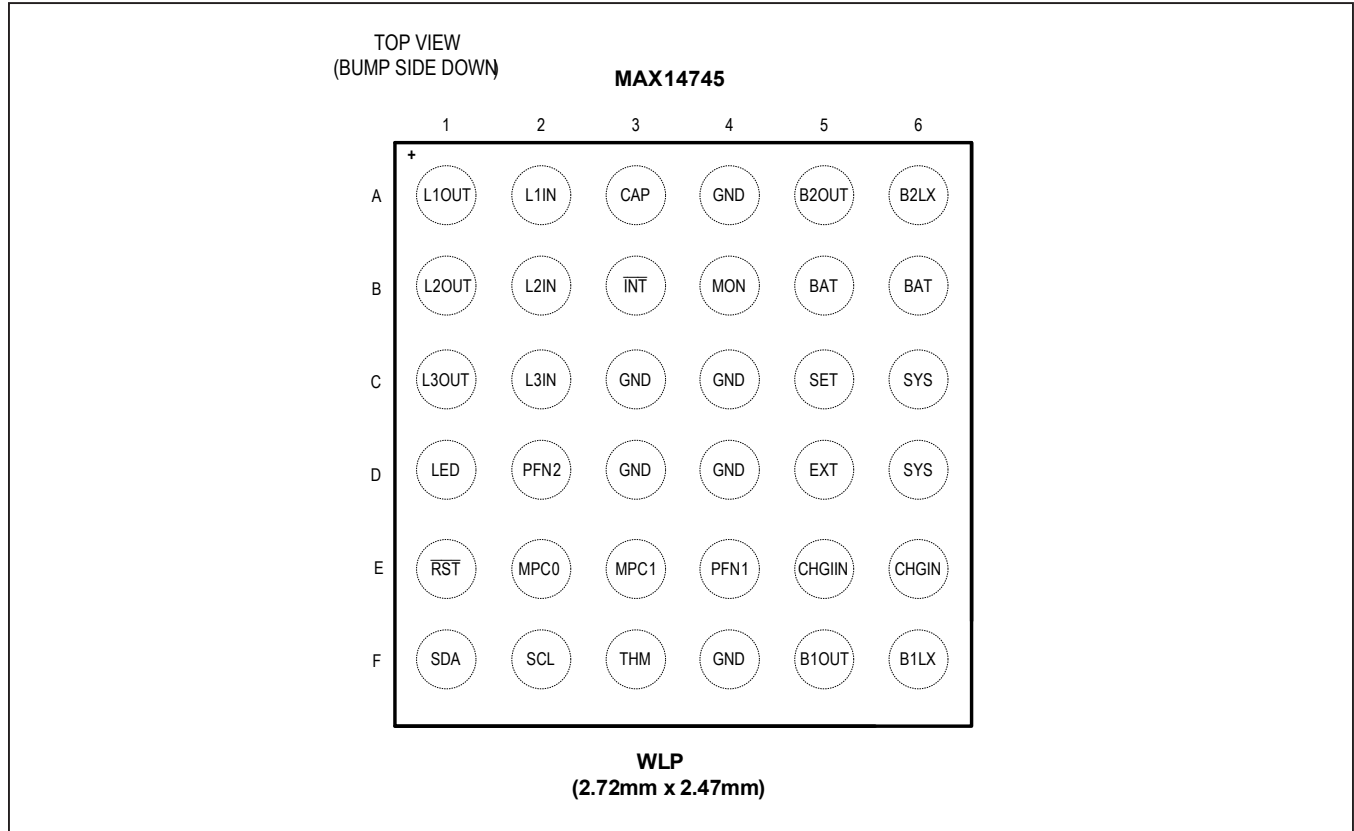
**Typical Operating Characteristics (continued)**

( $V_{BAT} = 3.7V$ ,  $V_{CHGIN} = 0V$ , registers in their default state,  $T_A = +25^{\circ}C$ , unless otherwise noted.)





### Bump Configuration



### Bump Description

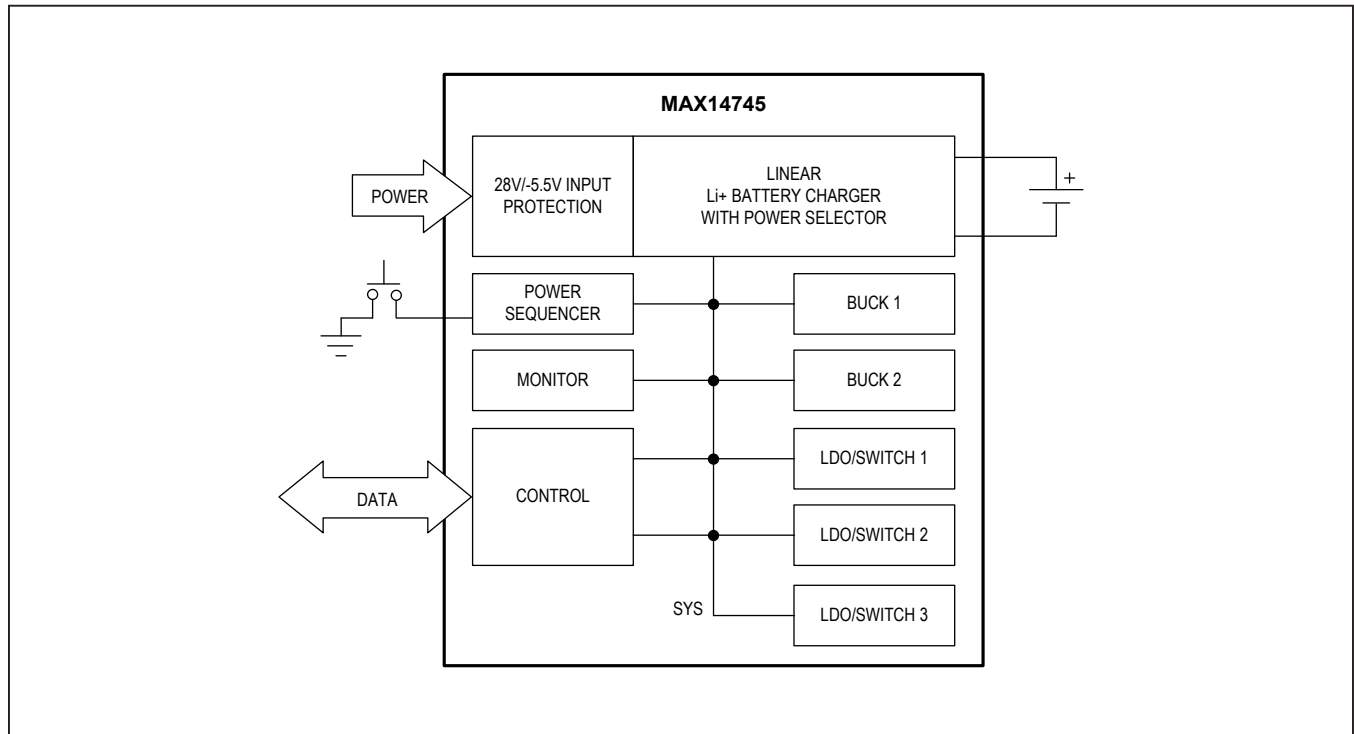
BUMP	NAME	FUNCTION
A1	L1OUT	LDO1 Output. Bypass with a minimum 1µF capacitor to GND.
A2	L1IN	LDO1 Input
A3	CAP	Bypass for Internal LDO. Bypass with a 1µF capacitor to GND.
A4, C3, C4 D3, D4, F4	GND	Ground
A5	B2OUT	0.8V – 3.95V Buck Regulator Output Feedback. Bypass with a 10µF capacitor to GND.
A6	B2LX	0.8V – 3.95V Buck Regulator Switch. Connect 2.2µH inductor to B2OUT.
B1	L2OUT	LDO2 Output. Bypass with a minimum 1µF capacitor to GND.
B2	L2IN	LDO2 Input
B3	INT	Open-Drain, Active-Low Interrupt Output.
B4	MON	Voltage Monitor Pin
B5, B6	BAT	Battery Connection. Connect BAT to a positive battery terminal, bypass BAT with a minimum 1µF capacitor to GND.

### Bump Description (continued)

PIN	NAME	FUNCTION
C1	L3OUT	LDO3 Output. Bypass with a minimum 1 $\mu$ F capacitor to GND.
C2	L3IN	LDO3 Input
C5	SET	External Resistor For Battery Charge Current Level Setting. Do not connect any external capacitance on this pin; maximum allowed capacitance ( $C_{SET} < 5\mu s/R_{SET}$ ) pF.
C6, D6	SYS	System Load Connection. Connect SYS to the system load. Bypass SYS with a minimum 10 $\mu$ F low-ESR ceramic capacitor to GND.
D1	LED	LED Open-Drain Pulldown Current. Add an external current limiting pullup resistor.
D2	PFN2	Power Function Control Input/Output. Programmable functionality via PwrFnMode. See Table 1.
D5	EXT	Push-Pull Gate Drive for Optional External pFET from BAT-to-SYS. Output is pulled to GND when charger is disconnected and internal BAT-SYS FET is switched on. Otherwise, this output is pulled high to the SYS voltage.
E1	$\overline{RST}$	Power-On Reset Output. Active-low, open-drain.
E2	MPC0	Multipurpose Configuration Input 0
E3	MPC1	Multipurpose Configuration Input 1
E4	PFN1	Power Function Control Input. Programmable functionality via PwrFnMode. See Table 1.
E5, E6	CHGIN	-5.5V/+28V Protected Charger Input. Bypass CHGIN with 1 $\mu$ F capacitor to GND.
F1	SDA	Open-Drain, I <sup>2</sup> C Serial Data Input/Output.
F2	SCL	I <sup>2</sup> C Serial Clock Input
F3	THM	Battery Temperature Thermistor Measurement Connection. Connect a 10k $\Omega$ resistor from THM to CAP and a 10k $\Omega$ , 3380A NTC thermistor from THM to GND.
F5	B1OUT	0.8V – 2.375V Buck Regulator Output Feedback. Bypass B1OUT with a 10 $\mu$ F capacitor to GND.
F6	B1LX	0.8V – 2.375V Buck Regulator Switch Terminal. Connect B1LX to B1OUT with a 2.2 $\mu$ H inductor.

**Note:** All capacitance values listed in this document refer to effective capacitance. Be sure to specify capacitors that will meet these requirements under typical system operating conditions taking into consideration the effects of voltage and temperature.

### Block Diagram



### Detailed Description

#### Power Regulation

The MAX14745 family includes two high-efficiency, low quiescent current buck regulators, and three low quiescent current linear regulators that are also configurable as power switches. Excellent light-load efficiency allows the switching regulators to run continuously without significant energy cost.

#### Power On/Off and Reset Control

The behavior of power function control pins (PFN1 and PFN2) is preconfigured to support one of the multiple types of wearable application cases. [Table 1](#) describes the behavior of the PFN1 and PFN2 pins based on the PwrRstCfg[3:0] bits and [Figure 1](#) shows basic flow diagrams associated with each mode.

A Soft-Reset generates a 10ms logic low pulse at  $\overline{RST}$  and resets all registers to their default values. A Hard-Reset initiates a complete Power-On Reset sequence and generates a 50ms logic-low pulse at  $\overline{RST}$ .

Table 1. Power Function Input Control Modes

PwrRstCfg[3:0]**	PFN1**	PFN1 PU/PD PFNxResEna = 1	PFN2**	PFN2 PU/PD PFNxResEna = 1	Available PwrCmd		
					OFF	HARD	SOFT
On/ $\overline{\text{Off}}$	ENABLE	PULLDOWN	Manual Reset	PULLUP*	NO	NO	YES
	On/Off Mode with 10ms debounce. PFN1 is the active-high on/off control input. PFN2 is the active-low soft-reset input.						
$\overline{\text{On}}$ /Off	DISABLE	PULLUP*	Manual Reset	PULLUP*	NO	NO	YES
	On/Off Mode with 10ms debounce. PFN1 is the active-low on/off control. PFN2 is the active-low soft-reset input.						
AON	Hard-Reset on PFN1 Rising	PULLDOWN	Soft-Reset on PFN2 Rising	PULLDOWN	YES	YES	YES
	Always-On Mode. A rising edge on PFN1 generates a hard reset after a 200ms delay. A rising edge on PFN2 generates a soft-reset after a 200ms delay. In this mode, the device can only enter the off state by writing to the PwrCmd register.						
$\overline{\text{AON}}$	Hard-Reset on PFN1 Falling	PULLUP*	Soft-Reset on PFN2 Falling	PULLUP*	YES	YES	YES
	Always-On Mode. A falling edge on PFN1 generates a hard-reset after a 200ms delay. A falling edge on PFN2 generates a soft-reset after a 200ms delay. In this mode, the device can only enter the off state by writing to the PwrCmd register.						
CR High	Hard-Reset on CHGIN insertion When PFN1 High	PULLDOWN	Soft-Reset CHGIN Insertion When PFN2 High	PULLDOWN	YES	YES	YES
	Charger Reset High Mode. When PFN1 is high, a CHGIN insertion generates a hard-reset after a 200ms delay. When PFN2 is high, a CHGIN insertion generates a soft-reset after a 200ms delay. In this mode, the device can only enter the off state by writing to the PwrCmd register.						
CR Low	Hard-Reset on CHGIN Insertion When PFN1 low	PULLUP*	Soft-Reset on CHGIN Insertion When PFN2 Low	PULLUP*	YES	YES	YES
	Charger Reset Low Mode. When PFN1 is low, a CHGIN insertion generates a Hard-Reset after a 200ms delay. When PFN2 is low, a CHGIN insertion generates a Soft-Reset after a 200ms delay. In this mode, the device can only enter the off state by writing to the PwrCmd register.						
$\overline{\text{KIN}}$	$\overline{\text{KIN}}$	PULLUP*	$\overline{\text{KOUT}}$	NONE	YES	YES	YES
	Custom Button Mode. PFN1 is the active-low $\overline{\text{KIN}}$ button input. PFN2 is the open-drain $\overline{\text{KOUT}}$ output, which buffers the $\overline{\text{KIN}}$ input. The device can enter the off state by either a $\overline{\text{KIN}}$ press (>12s) or by writing to the PwrCmd register. A CHGIN insertion or a $\overline{\text{KIN}}$ press (>400ms) can exit the off state.						
CSR1	$\overline{\text{KIN}}$	PULLUP*	$\overline{\text{KOUT}}$	NONE	YES	NO	NO
	Custom Soft Reset 1. PFN1 is the active-low $\overline{\text{KIN}}$ button input. PFN2 is the open-drain $\overline{\text{KOUT}}$ output, which buffers the $\overline{\text{KIN}}$ input. A $\overline{\text{KIN}}$ press (>12s) generates a soft-reset. The device can only enter the off state through the PwrCmd register. A CHGIN insertion or a $\overline{\text{KIN}}$ press (>3s) can exit the off state.						
CSR2	$\overline{\text{KIN}}$	PULLUP*	Manual Reset	NONE	YES	YES	YES
	Custom Soft-Reset 2. PFN1 is the active-low $\overline{\text{KIN}}$ button input. PFN2 is the active-low soft-reset input. A PFN2 press (>12s) generates a soft-reset. In this mode, the device can only enter the off state by writing to the PwrCmd register.						

\* Pullup is connected to an internal supply,  $V_{CCINT}$ . ( $V_{CCINT} = V_{CAP}$  if  $V_{CAP} > V_{CCINT\_TH}$ , or  $V_{CCINT} = V_{BAT}$  if  $V_{CAP} < V_{CCINT\_TH}$ ).

\*\* PwrRstCfg[3:0] is read-only; the functions of PFN1 and PFN2 cannot be changed through I<sup>2</sup>C

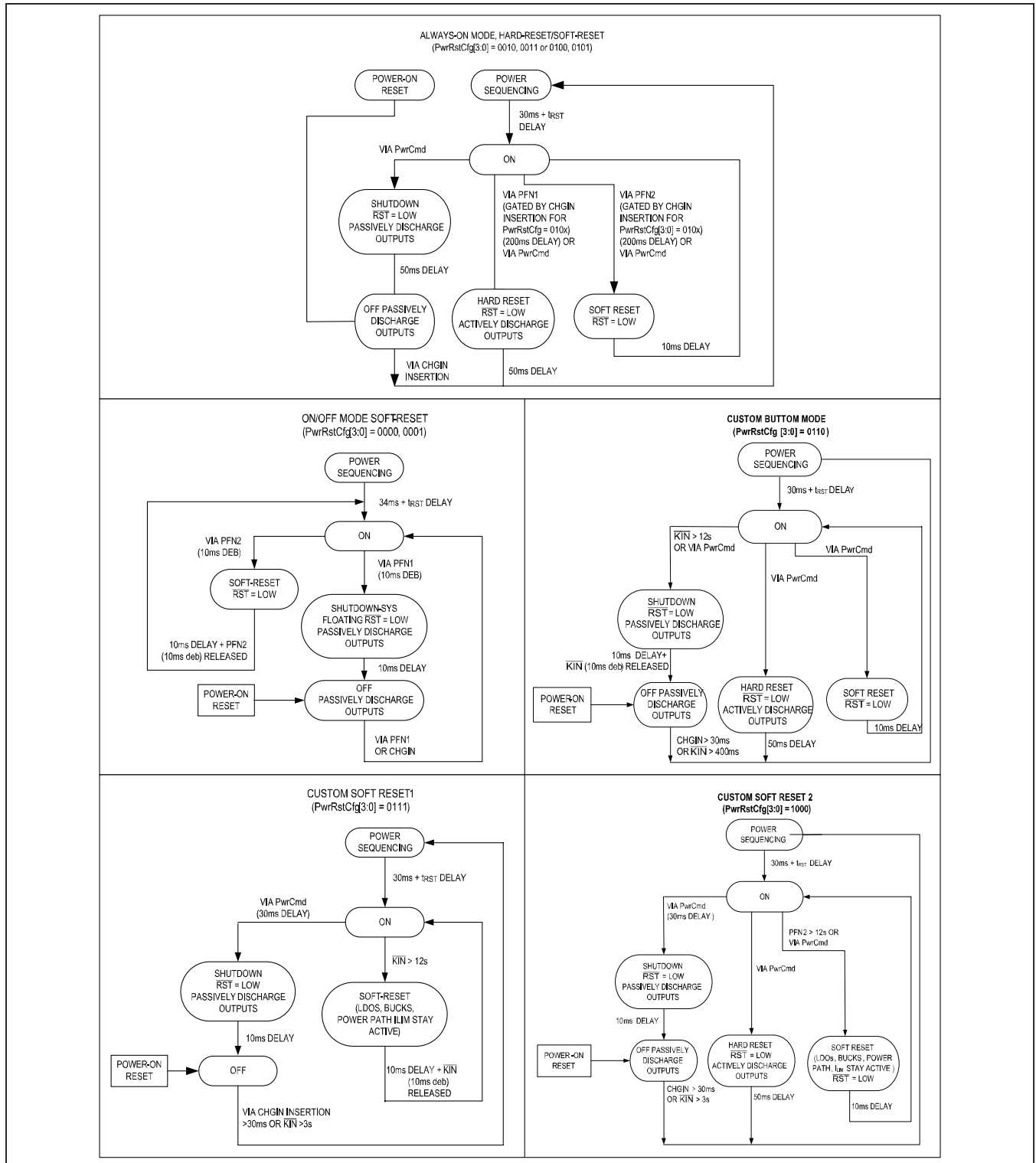


Figure 1. Power Function Input Control Modes Flow Diagrams

**Power Sequencing**

There are multiple configuration options for the sequencing of the buck regulators and LDOs during power-on. See [Table 1](#) for details. Regulators can be configured to turn on at one of the four points during the power-on process: 0%  $t_{RST}$ , 25%  $t_{RST}$ , 50%  $t_{RST}$ , and 100%  $t_{RST}$ . The reset delay  $t_{RST}$  can be set to 80ms, 120ms, 220ms, or 420ms by `BootDly[1:0]` in the `BootCfg` register. The power-on sequencing is depicted in [Figure 2a](#) and [Figure 2b](#).

Additionally, the regulators can be selected to default off and can be turned on with an I<sup>2</sup>C command after  $\overline{RST}$  is released. Each LDO regulator can be configured to be always-on as long as SYS or BAT is present.

In general, if an undervoltage condition is detected on SYS the device goes into the off state. However if there is a valid voltage on CHGIN the behavior is determined by the `ChgAlwTry` setting. If `ChgAlwTry = 0`, and an undervoltage condition is detected on SYS during the sequencing process the device turns SYS and all other external resources off and waits for CHGIN removal. On CHGIN removal the device enters the off state to avoid draining the battery. If `ChgAlwTry = 1`, the process will continually recheck the SYS undervoltage condition every 500ms until it is no longer valid before continuing with the sequencing process.

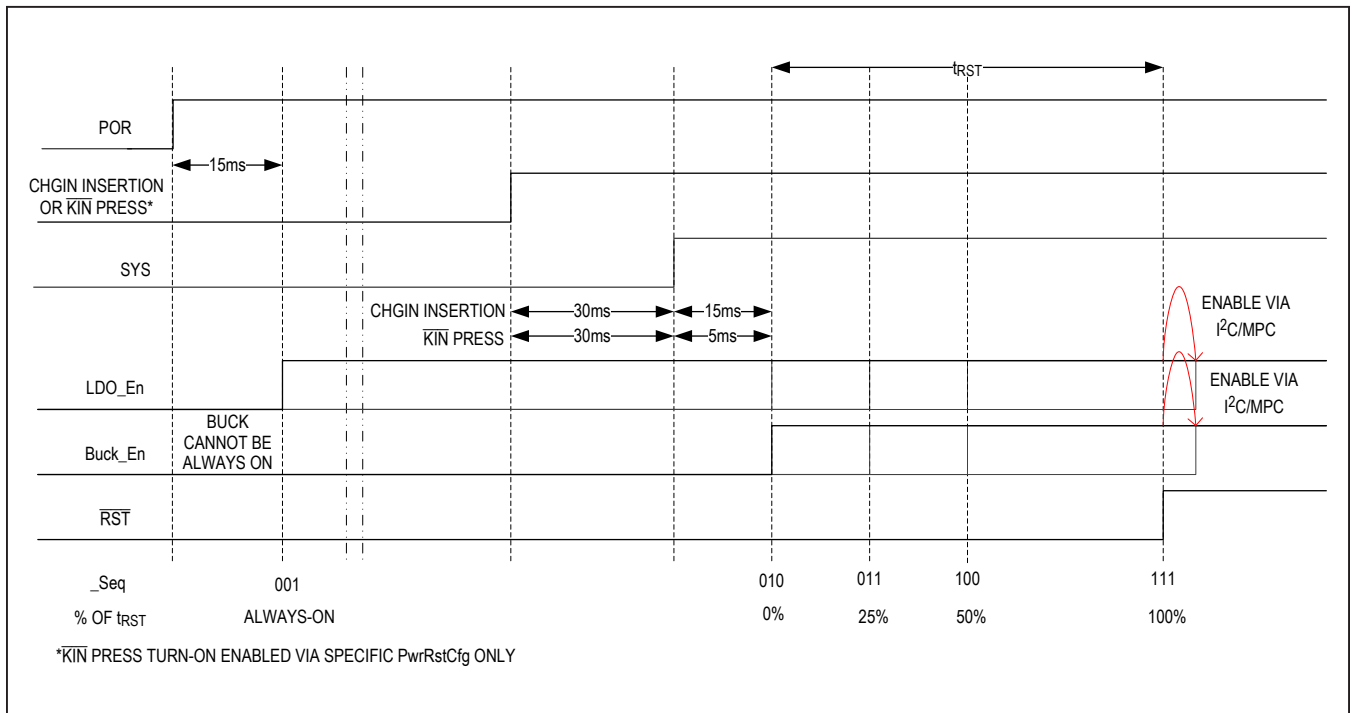


Figure 2a. Power-On Sequencing

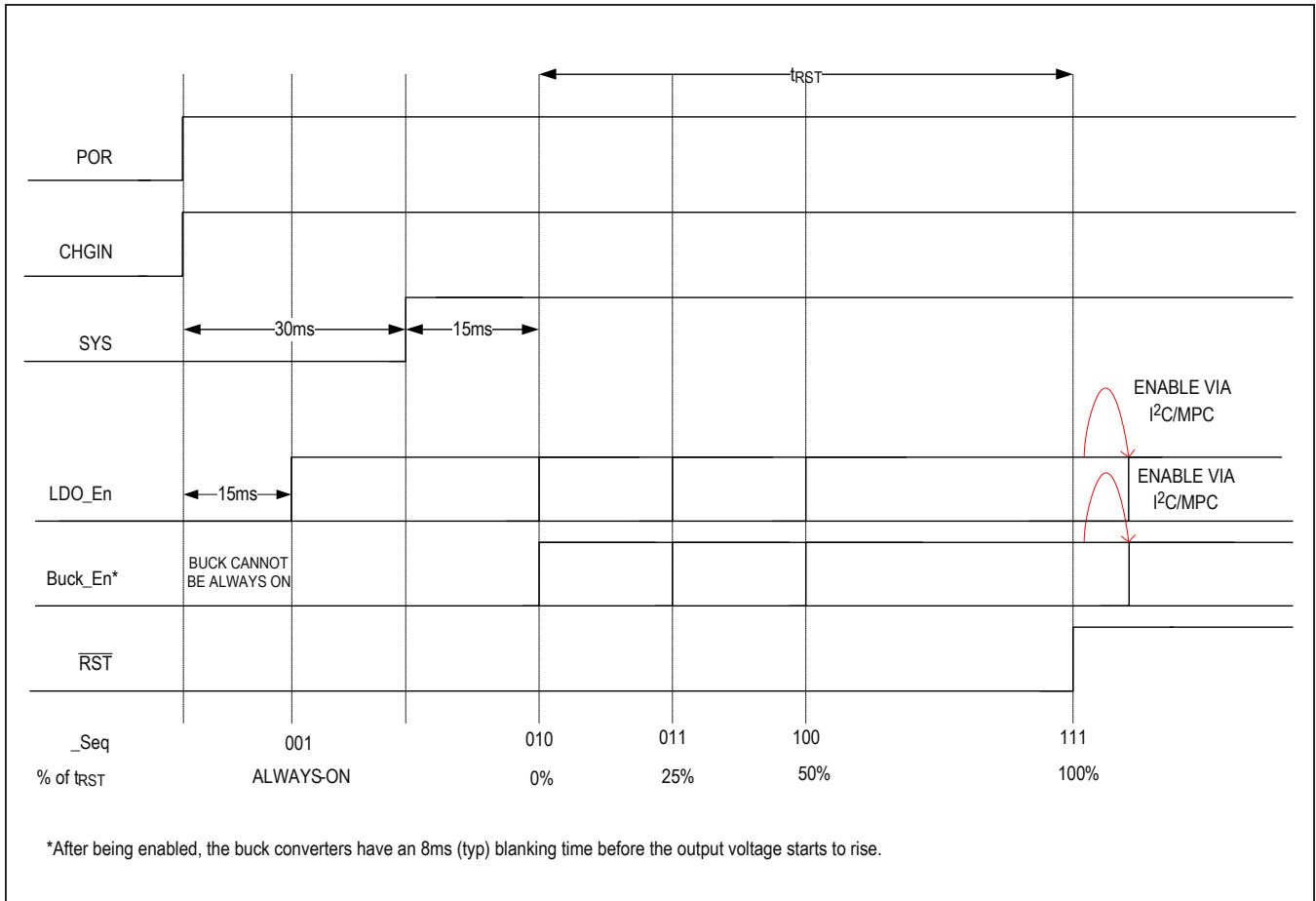


Figure 2b. Power-On Sequencing Without Battery

### Smart Power Selector

The smart power selector seamlessly distributes power from the external CHGIN input to the battery (BAT) and the system (SYS). With both an external adapter and battery connected, the smart power selector basic functions are:

- When the system load requirements are less than the input current limit, the battery is charged with residual power from the input.
- When the system load requirements exceed the input current limit, the battery supplies supplemental current to the load.

- When the battery is connected and there is no external power input, the system is powered from the battery.

### Thermal Current Regulation

In case the die temperature exceeds the normal limit, the MAX14745 will attempt to limit the temperature increase by reducing the input current from CHGIN. In this condition, the system load has priority over charger current, so the input current is first reduced by lowering the charge current. If the junction temperature continues to rise and reaches the maximum operating limit, no input current is drawn from CHGIN and the battery powers the entire system load.

### System Load Switch

An internal 80mΩ (typ) MOSFET connects SYS to BAT when no voltage source is available on CHGIN. When an external source is detected at CHGIN, this switch opens and SYS is powered from the input source through the input current limiter. The SYS-to-BAT switch also prevents  $V_{SYS}$  from falling below  $V_{BAT}$  when the system load exceeds the input current limit. If  $V_{SYS}$  drops to  $V_{BAT}$  due to the current limit, the load switch turns on so the load is supported by the battery. If the system load continuously exceeds the input current limit the battery is not charged. This is useful for handling loads that are nominally below the input current limit but have high current peaks exceeding the input current limit. During these peaks, battery energy is used, but at all other times the battery charges. See [Figure 3](#).

The pin EXT can drive the gate of an external pMOS connected between SYS (source, bulk) and BAT (drain) in parallel to the internal one.

When  $V_{CHGIN} < V_{BDET}$  the EXT voltage is the buffered version of the internal gate command that controls the internal 80mΩ (typ) MOSFET.

**Note:** The body diode of an external pMOS connected between BAT and SYS remains present when the device is in off mode.

### Input Limiter

The input limiter distributes power from the external adapter to the system load and battery charger. In addition to the input limiter's primary function of passing power to the system load and charger, it performs several additional functions to optimize use of available power:

**Invalid CHGIN Voltage Protection:** If CHGIN is above the overvoltage threshold, the MAX14745 enters overvoltage lockout (OVL). OVL protects the MAX14745 and downstream circuitry from high-voltage stress up to 28V and down to -5.5V. During OVL, the internal circuit remains powered and an interrupt is sent to the host. During OVL, the charger turns off and the system load switch closes, allowing the battery to power SYS. CHGIN is also invalid if it is less than  $V_{BAT}$ , or less than the USB undervoltage threshold. With an invalid input voltage, the SYS-to-BAT load switch closes and allows the battery to power SYS.

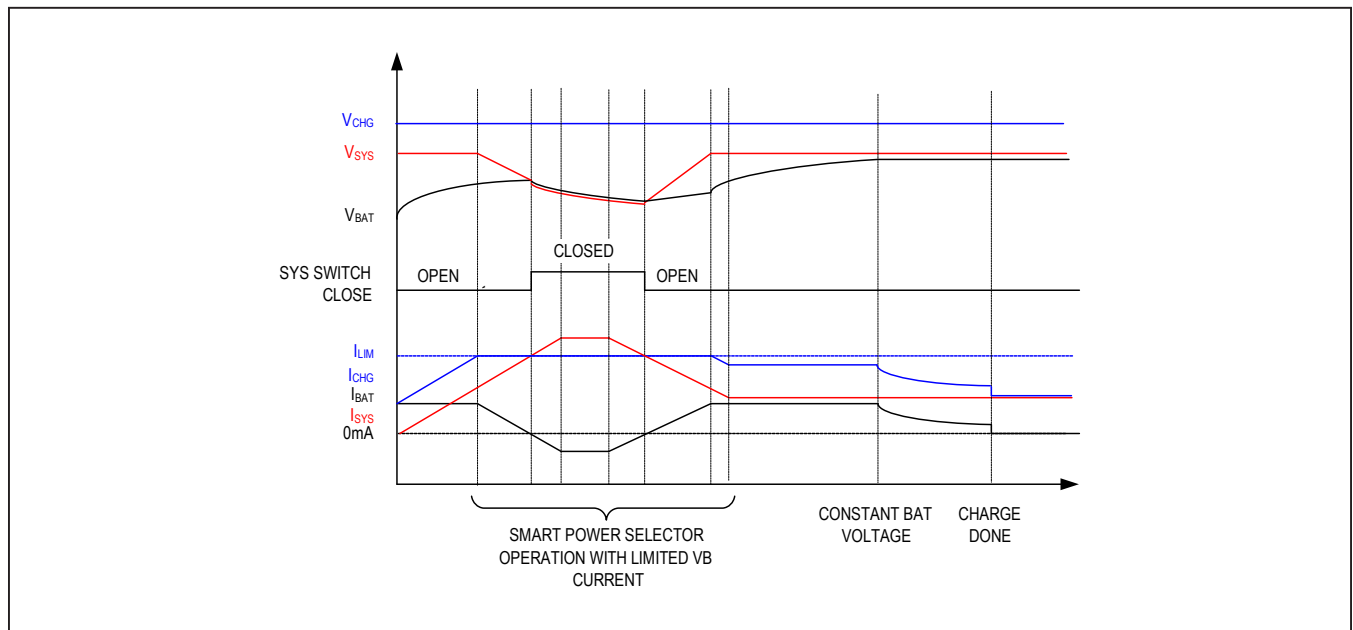


Figure 3. Smart Power Selector Current/Voltage Behavior



**CHGIN Adaptive Input Current Limit:** The CHGIN input current is limited to prevent input overload. The input current limit is controlled by I<sup>2</sup>C. However, if the voltage at CHGIN collapses because the source is not able to supply either the current programmed in I<sup>2</sup>C, or the total current required by the battery charger and system load, the input current limit will be adaptively reduced.

**Thermal Limiting:** In case the die temperature exceeds the normal limit (T<sub>CHG\_LIM</sub>), the MAX14745 attempts to limit temperature increase by reducing the input current from CHGIN. In this condition, the system load has priority over the charger current, so the input current is first reduced by lowering the charge current. If the junction temperature continues to rise and reaches the maximum operating limit (T<sub>CHGIN\_SHDN</sub>), no input current is drawn from CHGIN and the battery powers the entire system load.

**Adaptive Battery Charging:** While the system is powered from CHGIN, the charger draws power from SYS to charge the battery. If the total load exceeds the input current limit, an adaptive charger control loop reduces charge current to prevent V<sub>SYS</sub> from collapsing.

When the charge current is reduced below 50% due to I<sub>LIM</sub> or T<sub>DIE</sub>, the timer clock operates at half speed. When the charge current is reduced below 20% due to I<sub>LIM</sub> or T<sub>DIE</sub>, the timer clock is paused.

### Fast-Charge Current Setting

The MAX14745 uses an external resistor connected from SET to GND to set the fast-charge current. The pre-charge and charge-termination currents are programmed as a percentage of this value through I<sup>2</sup>C registers. The fast-charge current resistor can be calculated as:

$$R_{SET} = K_{SET} \times V_{SET} / I_{FChg}$$

where K<sub>SET</sub> has a typical value of 2000A/A and V<sub>SET</sub> has a typical value of 1V. The range of acceptable resistors for R<sub>SET</sub> is 4kΩ to 400kΩ

### Thermistor Monitoring with Charger Shutdown

The MAX14745 features three modes for controlling charger behavior based on battery-pack temperature: Thermistor Monitoring, JEITA Monitoring 1, and JEITA Monitoring 2. The divider formed by a pull-up resistor (RPU) to CAP, optional parallel resistor (RPA) from THM to ground, and NTC thermistor (RTHM) from THM to ground, provides a voltage at THM that is proportional to temperature as a fraction of the CAP voltage. Two sets of preconfigured default thresholds (0°C/10°C/45°C/60°C or 0°C/10°C/25°C/45°C as a %CAP) optimized for beta 3380 thermistors are available (see [Table 38](#)). The four default thresholds create five temperature zones, and the fractional CAP voltage measured at the THM pin is compared to the thresholds to determine the active temperature zone during operation.

The behavior in each temperature zone is determined by the configuration of bits in the I<sup>2</sup>C registers. The active monitoring mode is selected by ThermEn[1:0] in the ThrmCfrg register. In all modes, the T2IFchg[2:0] and T2T3IFchg[2:0], and T3T4IFchg[2:0] fields in the ThrmCfrg registers set the fast charge current in three temperature zones, T1\_T2, T2\_T3, and T3\_T4. In Thermistor Monitoring mode, charging is enabled only in T1\_T2 and T2\_T3 and the battery termination voltage is equal to V<sub>BATREG</sub>, as shown in [Figure 4a](#). In both JEITA Monitoring 1 and JEITA Monitoring 2 the charger is active in the T1\_T2, T2\_T3, and T3\_T4 zones. However, JEITA Monitoring 1 sets the battery termination voltage to V<sub>BATREG</sub> for all zones, while JEITA Monitoring 2 sets the battery termination voltage to V<sub>BATREG</sub> - 150mV for zones T1\_2 and T3\_T4, as shown in [Figure 4b](#). The behavior of all three modes is summarized in [Table 2](#).

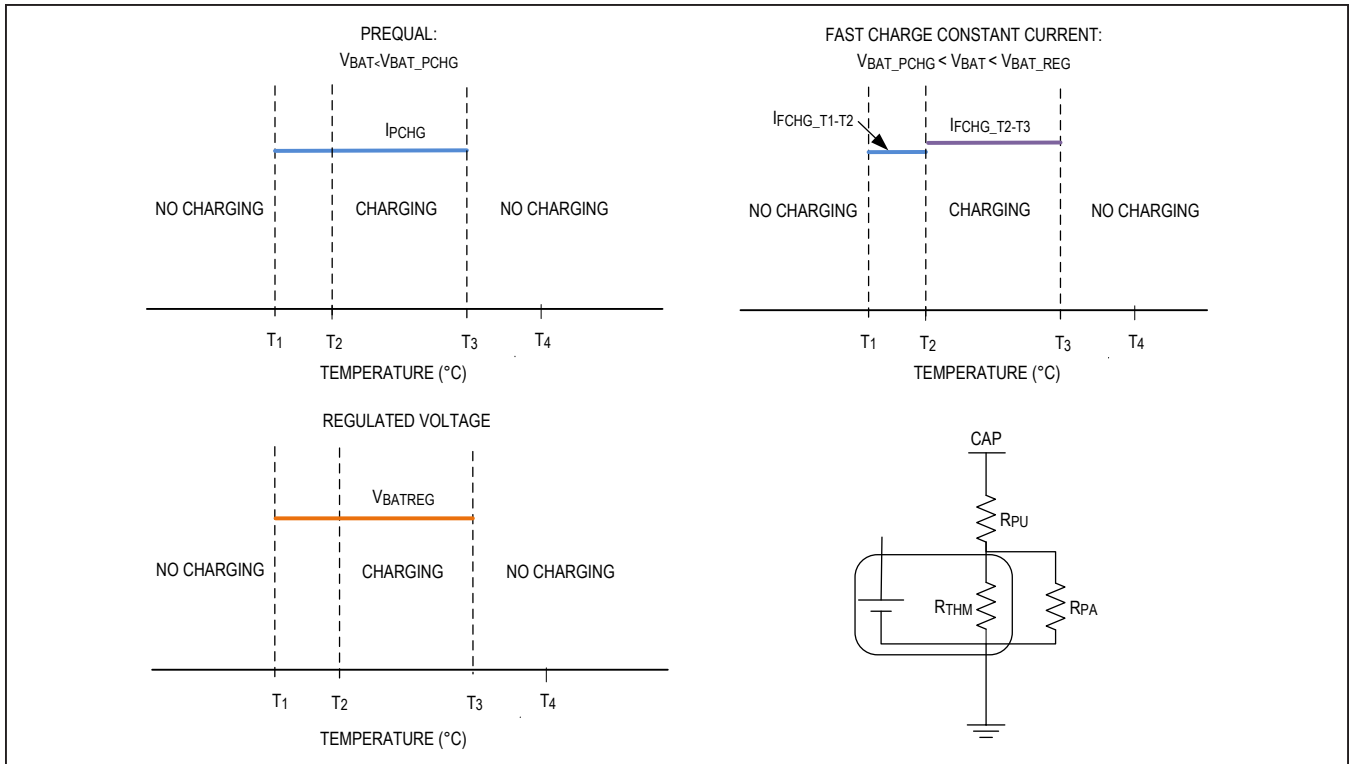


Figure 4a. Charging Behavior Using Thermistor Monitoring Mode

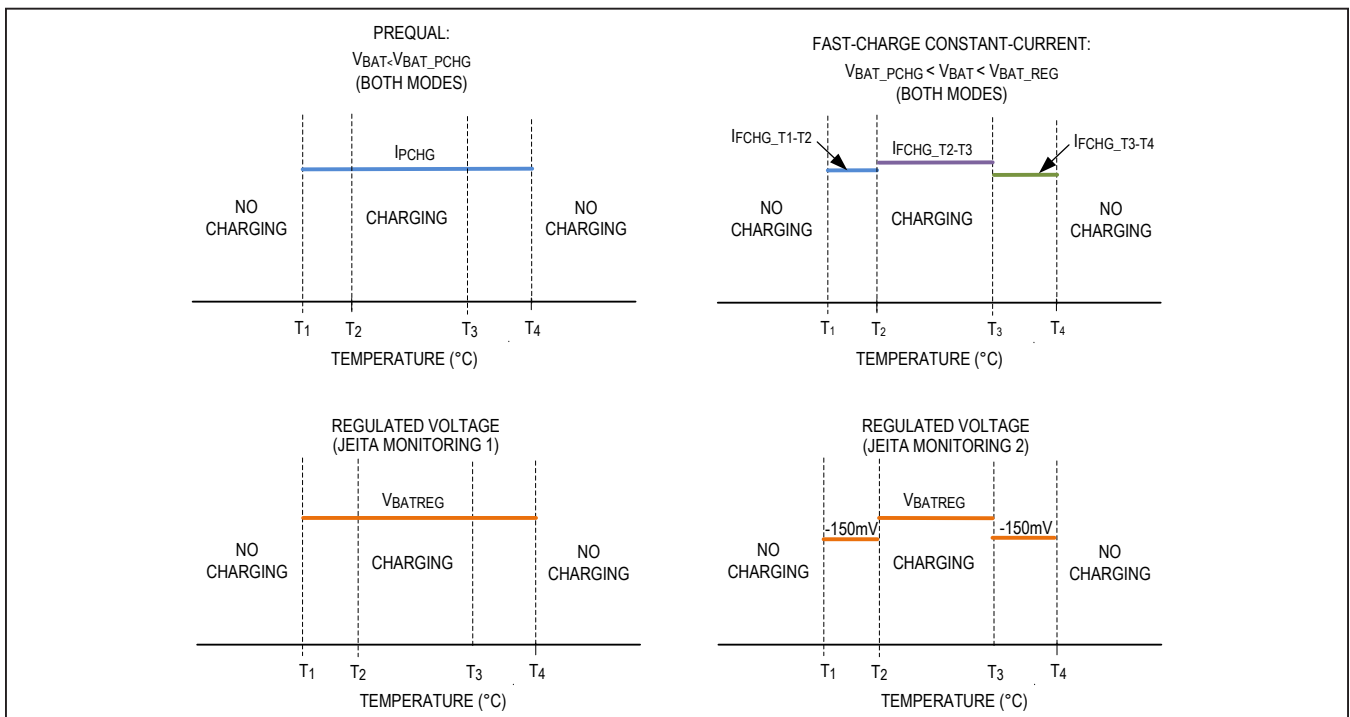


Figure 4b. Charging Behavior Using JEITA Monitoring 1 and 2 Modes

**Table 2. Thermistor Monitoring/JEITA Monitoring Enable Control**

ThermEn[1:0]	DESCRIPTION	CHARGER MODE				
		T < T1	T1 < T < T2	T2 < T < T3	T3 < T < T4	T > T4
00	Thermistor/ JEITA Monitoring OFF	As per I <sup>2</sup> C settings				
01	Thermistor Monitoring ON	OFF	I <sub>PCHG</sub> = IPChg, I <sub>FChg</sub> = T1T2IFchg, Regulated Voltage = V <sub>BATREG</sub>	I <sub>PCHG</sub> = IPChg, I <sub>FChg</sub> = T2T3IFchg, Regulated Voltage = V <sub>BATREG</sub>	OFF	OFF
10	JEITA Monitoring 1 ON	OFF	I <sub>PCHG</sub> = IPChg, I <sub>FChg</sub> = T1T2IFchg, Regulated Voltage = V <sub>BATREG</sub>	I <sub>PCHG</sub> = IPChg, I <sub>FChg</sub> = T2T3IFchg Regulated Voltage = V <sub>BATREG</sub>	I <sub>PCHG</sub> = IPChg, I <sub>FChg</sub> = T3T4IFchg Regulated Voltage = V <sub>BATREG</sub>	OFF
11	JEITA Monitoring 2 ON	OFF	I <sub>PCHG</sub> = IPChg, I <sub>FChg</sub> = T1T2IFchg, Regulated Voltage = V <sub>BATREG</sub> - 150mV	I <sub>PCHG</sub> = IPChg, I <sub>FChg</sub> = T2T3IFchg, Regulated Voltage = V <sub>BATREG</sub>	I <sub>PCHG</sub> = IPChg, I <sub>FChg</sub> = T3T4IFchg, Regulated Voltage = V <sub>BATREG</sub> - 150mV	OFF

**I<sup>2</sup>C Interface**

The device uses the two-wire I<sup>2</sup>C interface to communicate with the host microcontroller. The configuration settings and status information provided through this interface are detailed in the register descriptions.

**I<sup>2</sup>C Addresses**

The registers of the MAX14745 are accessed through the slave address of 0101000 (0x50 for writes/0x51 for reads).

Thermistor Monitoring with Charger Shutdown

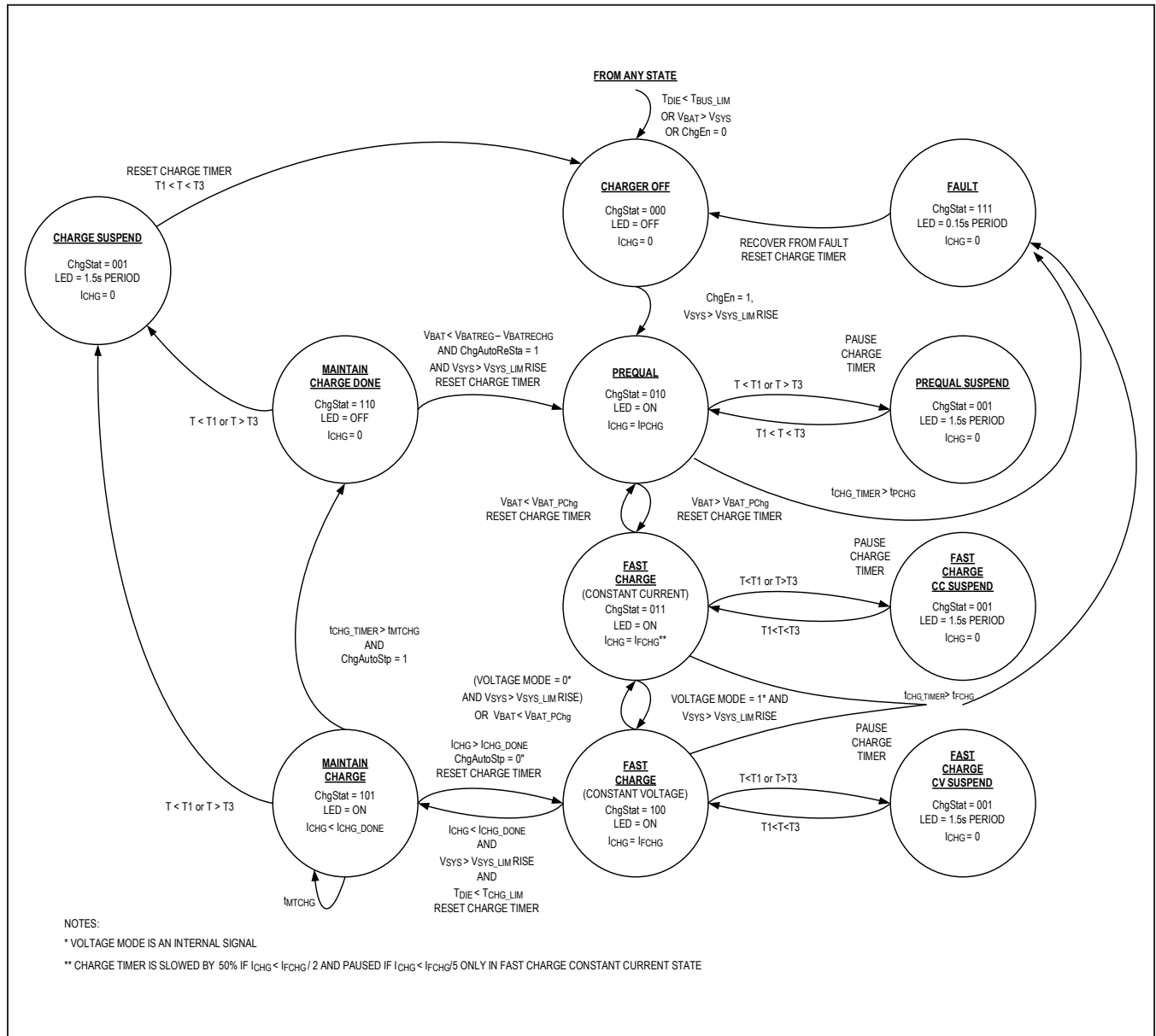


Figure 5a. Charger State Diagram (Thermistor Monitoring with Charger Shutdown)

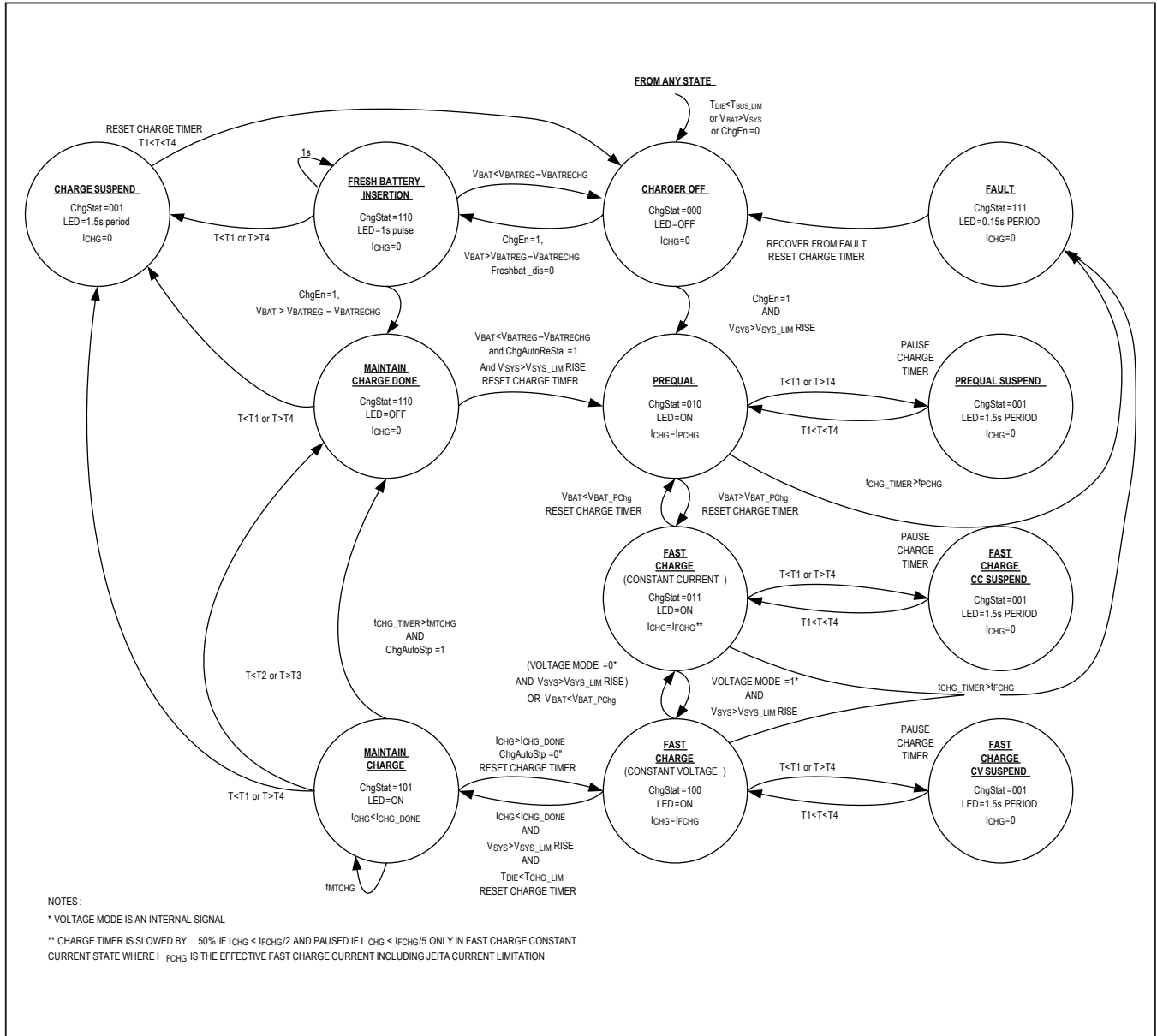


Figure 5b. Battery Charger State Diagram (JEITA Monitoring with Charger Shutdown)

### I<sup>2</sup>C Interface

The MAX14745 contain an I<sup>2</sup>C-compatible interface for data communication with a host controller (SCL and SDA). The interface supports a clock frequency of up to 400kHz. SCL and SDA require pullup resistors that are connected to a positive supply.

#### Start, Stop, And Repeated Start Conditions

When writing to the MAX14745 using I<sup>2</sup>C, the master sends a START condition (S) followed by the MAX14745 I<sup>2</sup>C address. After the address, the master sends the register address of the register that is to be programmed. The master then ends communication by issuing a STOP condition (P) to relinquish control of the bus, or a REPEATED START condition (Sr) to communicate to another I<sup>2</sup>C slave. See [Figure 6](#).

**Table 3. I<sup>2</sup>C Slave Addresses**

ADDRESS FORMAT	HEX	BINARY
7-Bit Slave ID	0x28	0101000
Write Address	0x50	01010000
Read Address	0x51	01010001

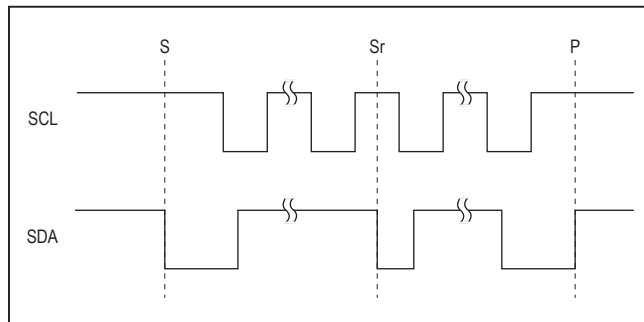


Figure 6. I<sup>2</sup>C START, STOP and REPEATED START Conditions

#### Slave Address

Set the Read/Write bit high to configure the MAX14745 to read mode ([Table 3](#)). Set the Read/Write bit low to configure the MAX14745 to write mode. The address is the first byte of information sent to the MAX14745 after the START condition.

#### Bit Transfer

One data bit is transferred on the rising edge of each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals (see the [Start, Stop, And Repeated Start Conditions](#) section). Both SDA and SCL remain high when the bus is not active.

#### Single-Byte Write

In this operation, the master sends an address and two data bytes to the slave device ([Figure 7](#)). The following procedure describes the single byte write operation:

- 1) The master sends a START condition
- 2) The master sends the 7-bit slave address plus a write bit (low)
- 3) The addressed slave asserts an ACK on the data line
- 4) The master sends the 8-bit register address
- 5) The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- 6) The master sends 8 data bits
- 7) The slave asserts an ACK on the data line
- 8) The master generates a STOP condition

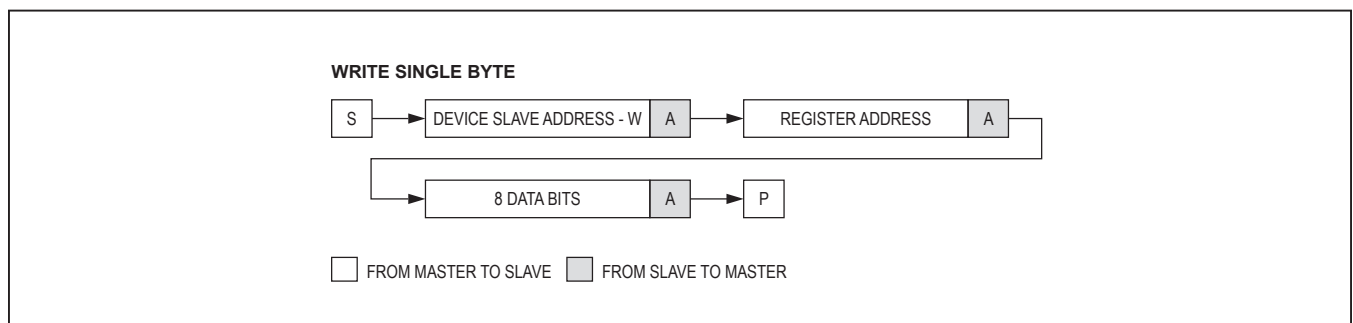


Figure 7. Write Byte Sequence

**Burst Write**

In this operation, the master sends an address and multiple data bytes to the slave device (Figure 8). The slave device automatically increments the register address after each data byte is sent. The following procedure describes the burst write operation:

- 1) The master sends a START condition
- 2) The master sends the 7-bit slave address plus a write bit (low)
- 3) The addressed slave asserts an ACK on the data line
- 4) The master sends the 8-bit register address
- 5) The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- 6) The master sends eight data bits
- 7) The slave asserts an ACK on the data line
- 8) Repeat 6 and 7 N-1 times
- 9) The master generates a STOP condition

**Single Byte Read**

In this operation, the master sends an address plus two data bytes and receives one data byte from the slave device (Figure 9). The following procedure describes the single byte read operation:

- 1) The master sends a START condition
- 2) The master sends the 7-bit slave address plus a write bit (low)
- 3) The addressed slave asserts an ACK on the data line
- 4) The master sends the 8-bit register address
- 5) The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- 6) The master sends a REPEATED START condition
- 7) The master sends the 7-bit slave address plus a read bit (high)
- 8) The addressed slave asserts an ACK on the data line
- 9) The slave sends eight data bits
- 10) The master asserts a NACK on the data line
- 11) The master generates a STOP condition

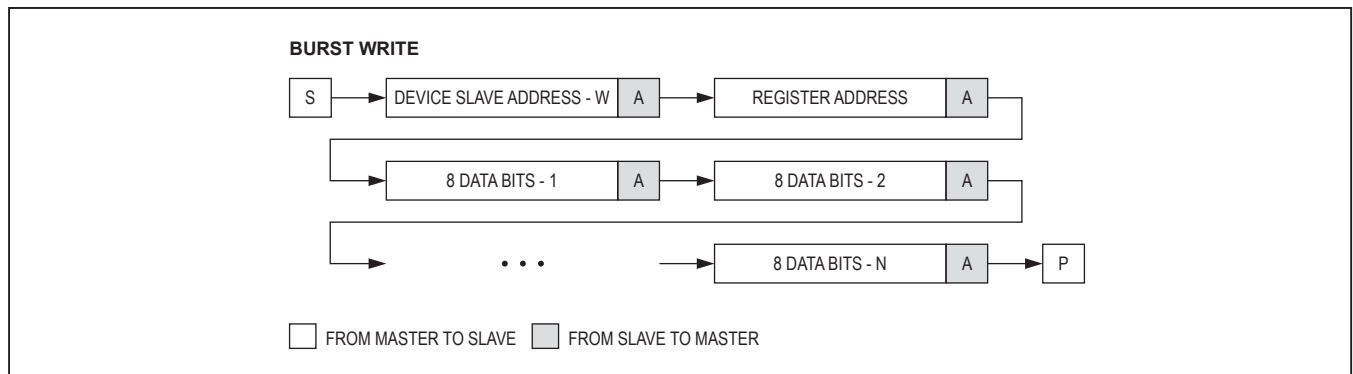


Figure 8. Burst Write Sequence

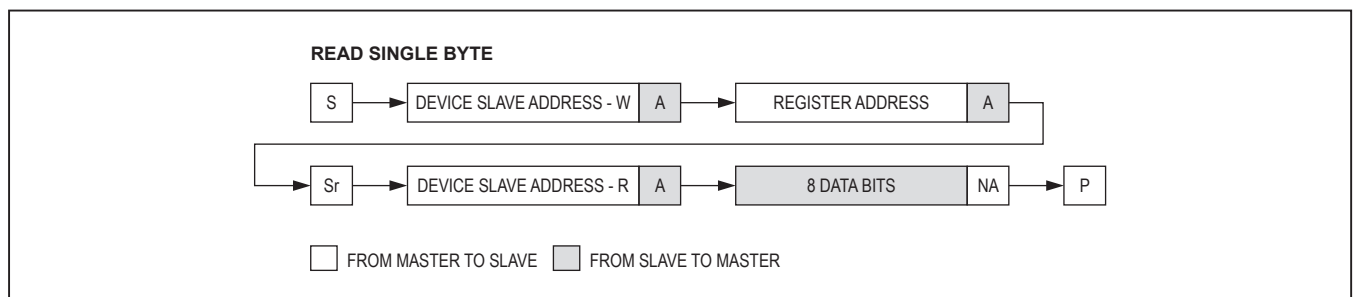


Figure 9. Read Byte Sequence

**Burst Read**

In this operation, the master sends an address plus two data bytes and receives multiple data bytes from the slave device (Figure 10). The following procedure describes the burst byte read operation:

- 1) The master sends a START condition
- 2) The master sends the 7-bit slave address plus a write bit (low)
- 3) The addressed slave asserts an ACK on the data line
- 4) The master sends the 8-bit register address
- 5) The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- 6) The master sends a REPEATED START condition
- 7) The master sends the 7-bit slave address plus a read bit (high)
- 8) The slave asserts an ACK on the data line
- 9) The slave sends eight data bits
- 10) The master asserts an ACK on the data line
- 11) Repeat 9 and 10 N-2 times
- 12) The slave sends the last eight data bits
- 13) The master asserts a NACK on the data line
- 14) The master generates a STOP condition

**Acknowledge Bits**

Data transfers are acknowledged with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the MAX14745 generate ACK bits. To generate an ACK, pull SDA low before the rising edge of the ninth clock pulse and hold it low during the high period of the ninth clock pulse (see Figure 11). To generate a NACK, leave SDA high before the rising edge of the ninth clock pulse and leave it high for the duration of the ninth clock pulse. Monitoring for NACK bits allows for detection of unsuccessful data transfers.

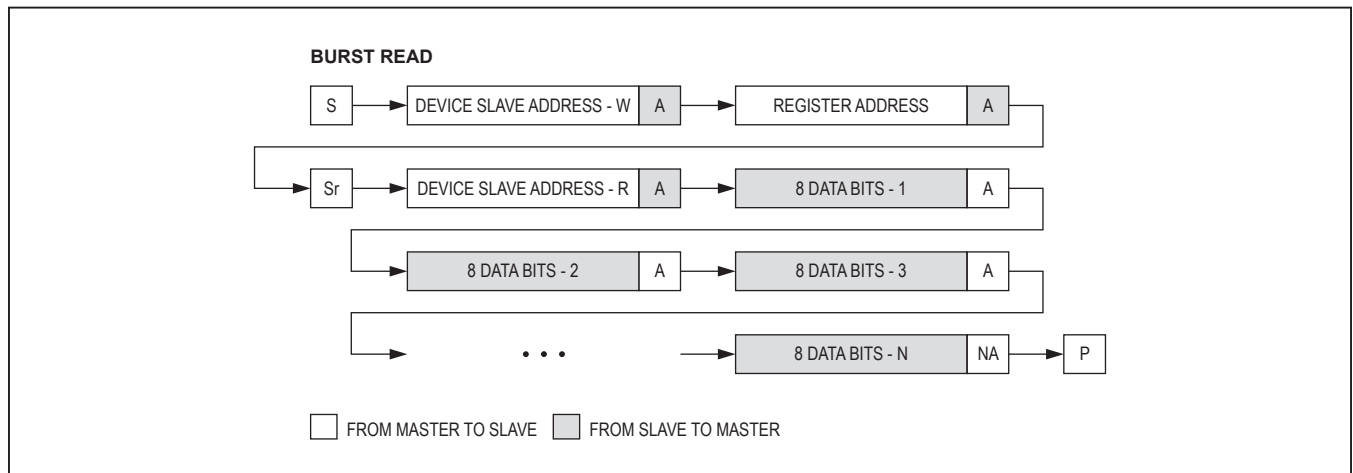


Figure 10. Burst Read Sequence

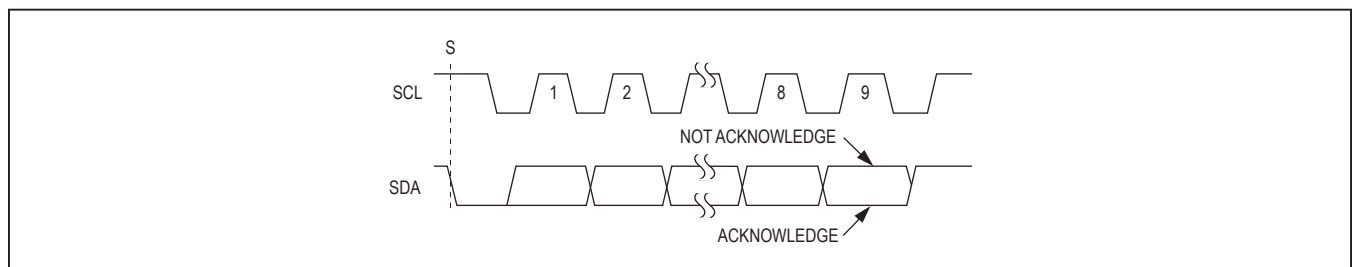


Figure 11. Acknowledge



I<sup>2</sup>C Register Map

REGISTER ADDRESS	REGISTER NAME	R/W	B7	B6	B5	B4	B3	B2	B1	B0
0x00	ChipId	R	Chip_Id[7:1:0] (Read-Only)							
0x01	ChipRev	R	Chip_Rev[7:0] (Read-Only)							
0x02	StatusA	R	—	JeitaStat[2:0]		ChgStat[2:0]				
0x03	StatusB	R	UVLOLOD2	UVLOLOD3	ILim	UsbOVP	UsbOk	ThrmSd	ChgThrmReg	ChgTmo
0x04	StatusC	R	—	SysBatLim	ChgSysLim	ThrmBk1	ThrmBk2	ThrmLDO1	ThrmLDO2	ThrmLDO3
0x05	IntA	COR	ThermStatInt	ChgStatInt	ILimInt	UsbOVPInt	UsbOkInt	ChgThrmSdInt	ChgThrmRegInt	ChgTmoInt
0x06	IntB	COR	—	SysBatLimInt	ChgSysLimInt	ThrmBk1Int	ThrmBk2Int	ThrmLDO1Int	ThrmLDO2Int	ThrmLDO3Int
0x07	IntMaskA	R/W	ThermStatIntM	ChgStatIntM	ILimIntM	UsbOVPIntM	UsbOkIntM	ChgThrmSdIntM	ChgThrmRegIntM	ChgTmoIntM
0x08	IntMaskB	R/W	—	SysBatLimIntM	ChgSysLimIntM	ThrmBk1IntM	ThrmBk2IntM	ThrmLDO1IntM	ThrmLDO2IntM	ThrmLDO3IntM
0x09*	ILimCntl	R/W**	SysMin[2:0]	SysMin[2:0]	SysMin[2:0]	—	—	—	ILimCntl[1:0]	—
0x0A*	ChgCntlA	R/W**	—	BatReChg[1:0]	BatReg[3:0]	—	—	—	—	ChgEn
0x0B*	ChgCntlB	R/W**	—	—	VPChg[2:0]	—	—	IPChg[1:0]	ChgDone[1:0]	—
0x0C*	ChTmr	R/W**	ChgAutoStp	ChgAutoReSta	MtChgTmr[1:0]	—	—	FChgTmr[1:0]	PChgTmr[1:0]	—
0x0D	Buck1Cfgr	R/W	Buck1Seq[2:0]	Buck1Seq[2:0]	Buck1En[1:0]	—	—	Reserved	Reserved	Reserved
0x0E	Buck1VSet	R/W**	Buck1LowEMI	—	—	Buck1VSet[5:0]	—	—	—	—
0x0F	Buck2Cfgr	R/W	Buck2Seq[2:0]	Buck2Seq[2:0]	Buck2En[1:0]	—	—	Reserved	Reserved	Reserved
0x10	Buck2VSet	R/W**	Buck2LowEMI	—	—	Buck2VSet[5:0]	—	—	—	—
0x11	Buck1/2ISet	R/W	Buck2ISet[3:0]		Buck1ISet[3:0]		Buck1ISet[3:0]			
0x12	LDO1Cfgr	R/W	LDO1Seq[2:0]		LDO1En[1:0]		LDO1En[1:0]			

I<sup>2</sup>C Register Map (continued)

REGISTER ADDRESS	REGISTER NAME	R/W	B7	B6	B5	B4	B3	B2	B1	B0
0x13	LDO1VSet	R/W**	—	—	—	—	—	LDO1VSet[4:0]		
0x14	LDO2Cfgr	R/W	LDO2Seq[2:0]		—	—	LDO2 ActDSC	LDO2En[1:0]		LDO2Mode
0x15	LDO2VSet	R/W**	—	—	—	—	LDO2VSet[4:0]			
0x16	LDO3Cfgr	R/W	LDO3Seq[2:0]		—	—	LDO3 ActDSC	LDO3En[1:0]		LDO3Mode
0x17	LDO3VSet	R/W**	—	—	—	—	LDO3VSet[4:0]			
0x18*	ThrmCfgr	R/W	T1T2Fchg[2:0]		T2T3Fchg[2:0]		ThermEn[1:0]			
0x19*	ThrmCfgr	R/W	—	—	—	—	—	T3T4Fchg[2:0]		
0x1A	MONCfgr	R/W	MONRatioCfgr[1:0]		MONHiZ		MONCtr[2:0]			
0x1B	BootCfgr	R/W	PwrRstCfgr[3:0]			SftRstCfgr		BootDly[1:0]		ChgAlwTry
0x1C	PinStat	R/W	ILim_T[2:0]		—	—	PFN1	PFN2	MPC1	MPC0
0x1D	Buck1/2Extra	R/W	Buck2AdptEnb	Buck2Fst	Buck2 ActDsc	Buck2FFET	Buck1AdptEnb	Buck1Fst	Buck1ActDSC	Buck1FFET
0x1E	PwrCfgr	R/W	PFNxResEna	—	—	—	—	—	—	StayOn
0x1F	PwrCmd	R/W	PWR_CMD							

**Note:** COR = Clear-on-read

\*Register is reset to default value upon CHGIN rising edge.

\*\* R if WriteProtect enabled (Table 38).

All R/W registers are reset to default value when entering the off state.

Reserved bits must not be modified from their default states to ensure proper operation.

## I<sup>2</sup>C Register Descriptions

**Table 4. ChipId Register (0x00)**

<b>ADDRESS:</b>	0x00							
<b>MODE:</b>	Read-Only							
<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	Chip_Id[7:0]							
<b>Chip_Id[7:0]</b>	Chip_Id[7:0] bits show information about the version of the MAX14745.							

**Table 5. ChipRev Register (0x01)**

<b>ADDRESS:</b>	0x01							
<b>MODE:</b>	Read-Only							
<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	Chip_Rev[7:0]							
<b>Chip_Rev[7:0]</b>	Chip_Rev[7:0] bits show information about the revision of the MAX14745 silicon.							

**Table 6. StatusA Register (0x02)**

<b>ADDRESS:</b>	0x02							
<b>MODE:</b>	Read-Only							
<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	—	—	ThermStat[2:0]			ChgStat[2:0]		
<b>ThermStat[2:0]</b>	<p>Status of Thermistor Monitoring</p> <p>000 = T &lt; T1</p> <p>001 = T1 &lt; T &lt; T2</p> <p>010 = T2 &lt; T &lt; T3</p> <p>011 = T3 &lt; T &lt; T4</p> <p>100 = T &gt; T4</p> <p>101 = No thermistor detected (THM high due to external pullup). Note that if a parallel resistor is used for thermistor monitoring, this mode may not function properly.</p> <p>110 = NTC input disabled through ThermEn[1:0]</p> <p>111 = Detection disabled due to CHGIN not present.</p>							
<b>ChgStat[2:0]</b>	<p>Status of Charger Mode</p> <p>000 = Charger off</p> <p>001 = Charging suspended due to temperature (see Figure 5a and Figure 5b)</p> <p>010 = Pre-charge in progress</p> <p>011, 100 = Fast charge in progress</p> <p>101 = Maintain charge in progress</p> <p>110 = Maintain charger timer done</p> <p>111 = Charger fault condition (see Figure 5a and Figure 5b)</p>							

**Table 7. StatusB Register (0x03)**

<b>ADDRESS:</b>	<b>0x03</b>							
<b>MODE:</b>	<b>Read-Only</b>							
<b>BIT</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>NAME</b>	UVLOLD02	UVLOLD03	ILim	UsbOVP	UsbOk	Chg ThrmSd	Chg ThrmReg	ChgTmo
<b>UVLOLD02</b>	Status of LDO2 UVLO 0 = LDO2 in normal operating mode 1 = Undervoltage-lockout on LDO2							
<b>UVLOLD03</b>	Status of LDO3 UVLO 0 = LDO3 in normal operating mode 1 = Undervoltage-lockout on LDO3							
<b>ILim</b>	CHGIN Input Current Limit 0 = CHGIN input current is within limit. 1 = CHGIN input is in current limit.							
<b>UsbOVP</b>	Status of CHGIN OVP 0 = CHGIN OVP is not active. 1 = CHGIN OVP is active.							
<b>UsbOk</b>	Status of CHGIN Input 0 = CHGIN Input is not present or outside of valid range. 1 = CHGIN Input is present and valid.							
<b>ChgThrmSd</b>	Status of Thermal Shutdown 0 = Charger and input current limiter is in normal operating mode. 1 = Charger and input current limiter is in thermal shutdown.							
<b>ChgThrmReg</b>	Status of Thermal Regulation 0 = Charger is functioning normally, or disabled. 1 = Charger is running in thermal regulation mode and charging current is being actively reduced to prevent device overheating.							
<b>ChgTmo</b>	Status of Time-Out Condition 0 = Charger is running normally, or disabled. 1 = Charger has reached a time-out condition. ChgStat =1 11 in this condition (see Figure 5).							

**Table 8. StatusC Register (0x04)**

ADDRESS:	0x04							
MODE:	Read-Only							
BIT	7	6	5	4	3	2	1	0
NAME	—	SysBLim	VLim	ThrmBuck1	ThrmBuck2	ThrmLDO1	ThrmLDO2	ThrmLDO3
<b>SysBLim</b>	<p>Status of Minimum SYS-BAT Voltage Limit. While the system is powered from VBUS, the charger draws power from SYS to charge the battery. If the total load exceeds the input current limit, an adaptive charger control loop reduces charge current to prevent VSYS from collapsing. The regulation of the charge current starts when either one of the following two conditions is true: 1. <math>V_{SYS} - V_{BAT} = 100\text{mV}</math> (typ) OR 2. <math>V_{SYS} = V_{SYS\_LIM}</math> (falling)</p> <p>0 = Charge Current is normal.  1 = Charge Current is being actively reduced to prevent SYS collapse.</p>							
<b>VLim</b>	<p>Status of CHGIN-SYS Voltage Limit. This bit indicates if the input current limit is being actively reduced to maintain a 40mV drop between CHGIN-SYS. This adaptive input current limit prevents adapter collapse in the case that a power adapter with insufficient load capability, or a high resistance charging cable is used.</p> <p>0 = CHGIN input current limit is functioning normally.  1 = CHGIN input current limit is being actively reduced to maintain 40mV drop between CHGIN-SYS.</p>							
<b>ThrmBuck1</b>	<p>0 = Buck1 NOT in Thermal Off mode  1 = Buck1 in Thermal Off Mode</p>							
<b>ThrmBuck2</b>	<p>0 = Buck2 NOT in Thermal Off mode  1 = Buck2 in Thermal Off Mode</p>							
<b>ThrmLDO1</b>	<p>0 = LDO1 NOT in Thermal Off mode  1 = LDO1 in Thermal Off Mode</p>							
<b>ThrmLDO2</b>	<p>0 = LDO2 NOT in Thermal Off mode  1 = LDO2 in Thermal Off Mode</p>							
<b>ThrmLDO3</b>	<p>0 = LDO3 NOT in Thermal Off mode  1 = LDO3 in Thermal Off Mode</p>							

**Table 9. IntA Register (0x05)**

<b>ADDRESS:</b>	<b>0x05</b>							
<b>MODE:</b>	<b>Clear On Read</b>							
<b>BIT</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>NAME</b>	Therm StatInt	ChgStatInt	ILimInt	UsbOVPInt	UsbOk	Chg ThrmSdInt	Therm RegInt	Chg Tmolnt
<b>ThermStatInt</b>	Change in ThermStat caused interrupt.							
<b>ChgStatInt</b>	Change in ChgStat caused interrupt, or first detection complete after POR.							
<b>ILimInt</b>	Input current limit triggered caused interrupt.							
<b>UsbOVPInt</b>	Change in UsbOVP caused interrupt.							
<b>UsbOk</b>	Change in UsbOk caused interrupt.							
<b>ChgThrmSdInt</b>	Change in ChgThrmSd caused interrupt.							
<b>ThermRegInt</b>	Change in ChgThrmReg caused interrupt.							
<b>ChgTmolnt</b>	Change in ChgTmo caused interrupt.							

**Table 10. IntB Register (0x06)**

<b>ADDRESS:</b>	<b>0x06</b>							
<b>MODE:</b>	<b>Clear On Read</b>							
<b>BIT</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>NAME</b>	—	SysBLimInt	VLimInt	Thrm Buck1Int	Thrm Buck2Int	Thrm LDO1Int	Thrm LDO2Int	Thrm LDO3Int
<b>SysBLimInt</b>	Minimum SYS-BAT voltage limit caused interrupt							
<b>VLimInt</b>	Input Voltage Limit caused interrupt							
<b>ThrmBuck1Int</b>	Change in ThrmBuck1 caused interrupt.							
<b>ThrmBuck2Int</b>	Change in ThrmBuck2 caused interrupt.							
<b>ThrmLDO1Int</b>	Change in ThrmLDO1 caused interrupt.							
<b>ThrmLDO2Int</b>	Change in ThrmLDO2 caused interrupt.							
<b>ThrmLDO3Int</b>	Change in ThrmLDO3 caused interrupt.							

**Table 11. IntMaskA Register (0x07)**

<b>ADDRESS:</b>	0x07							
<b>MODE:</b>	Read/Write							
<b>BIT</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>NAME</b>	Therm StatIntM	Chg StatIntM	ILimIntM	Usb OVPIntM	UsbOkM	ChgThrm SdIntM	Therm RegIntM	Chg TmolntM
<b>ThermStatIntM</b>	ThermStatIntM masks the ThermStatInt interrupt in the IntA register (0x05). 0 = Mask 1 = Not masked							
<b>ChgStatIntM</b>	ChgStatIntM masks the ChgStatInt interrupt in the IntA register (0x05). 0 = Mask 1 = Not masked							
<b>ILimIntM</b>	ILimIntM masks the ILimInt interrupt in the IntB register (0x06). 0 = Mask 1 = Not masked							
<b>UsbOVPIntM</b>	UsbOVPIntM masks the UsbOVPInt interrupt in the IntA register (0x05). 0 = Mask 1 = Not masked							
<b>UsbOkM</b>	UsbOkM masks the UsbOk interrupt in the IntB register (0x06). 0 = Mask 1 = Not masked							
<b>ChgThrm SdIntM</b>	ChgThrmSdIntM masks the ChgThrmSdInt interrupt in the IntB register (0x06). 0 = Mask 1 = Not masked							
<b>ThermRegIntM</b>	ThermRegIntM masks the ThermRegInt interrupt in the IntA register (0x05). 0 = Mask 1 = Not masked							
<b>ChgTmolntM</b>	ChgTmolntM masks the ChgTmolnt interrupt in the IntA register (0x05). 0 = Mask 1 = Not masked							

**Table 12. IntMaskB Register (0x08)**

ADDRESS:	0x08							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	—	SysB LimIntM	VLimIntM	Thrm Buck1IntM	Thrm Buck2IntM	Thrm LDO1IntM	Thrm LDO2IntM	Thrm LDO3IntM
<b>SysBLimIntM</b>	SysBLimIntM masks the SysBLimInt interrupt in the IntB register (0x06). 0 = Mask 1 = Not masked							
<b>VLimIntM</b>	VLimIntM masks the VLimInt interrupt in the IntB register (0x06). 0 = Mask 1 = Not masked							
<b>ThrmBuck1 IntM</b>	0 = Mask 1 = Not masked							
<b>ThrmBuck2 IntM</b>	0 = Mask 1 = Not masked							
<b>ThrmLDO1 IntM</b>	0 = Mask 1 = Not masked							
<b>ThrmLDO2 IntM</b>	0 = Mask 1 = Not masked							
<b>ThrmLDO3 IntM</b>	0 = Mask 1 = Not masked							

**Table 13. ILimCntl Register (0x09)**

ADDRESS:	0x09								
MODE:	Read/Write* or Read-Only if Write-Protect Enabled (see Table 38)								
BIT	7	6	5	4	3	2	1	0	
NAME	SysMin[2:0]				—	—	—	ILimCntl [1:0]	
<b>SysMin[2:0]</b>	SysMin sets System Voltage Minimum Threshold. When SYS drops to this level, the charger current is reduced. 000 = 3.6V 001 = 3.7V 010 = 3.8V 011 = 3.9V 100 = 4.0V 101 = 4.1V 110 = 4.2V 111 = 4.3V								
<b>ILimCntl[1:0]</b>	CHGIN Custom Input Current Limit (see Electrical Characteristics table for details) 00 = 0mA 01 = 100mA 10 = 500mA 11 = 1000mA								

\*Register is reset to default value upon CHGIN rising edge.



**Table 14. ChgCntlA Register (0x0A)**

<b>ADDRESS:</b>	0x0A							
<b>MODE:</b>	Read/Write* or Ready-Only if Write-Protect Enabled (see Table 38)							
<b>BIT</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>NAME</b>		BatReChg[1:0]		BatReg[3:0]				ChgEn
<b>BatReChg[1:0]</b>	Recharge Threshold in Relation to BatReg 00 = BatReg - 70mV 01 = BatReg - 120mV 10 = BatReg - 170mV 11 = BatReg - 220mV							
<b>BatReg[3:0]</b>	Setting the Battery Regulation Threshold 0000 = 4.05V 0001 = 4.10V 0010 = 4.15V 0011 = 4.20V 0100 = 4.25V 0101 = 4.30V 0110 = 4.35V 0111 = 4.4V 1000 = 4.45V 1001 = 4.5V 1010 = 4.55V 1011 = 4.6V 1100...1111 = Reserved							
<b>ChgEn</b>	On/Off Control for Charger (does not affect SYS node). 0 = Charger disabled. 1 = Charger enabled.							

\*Register is reset to default value upon CHGIN rising edge.

**Table 15. ChgCntlB Register (0x0B)**

ADDRESS:	0x0B							
MODE:	Read/Write* or Ready-Only if Write-Protect Enabled (see Table 38)							
BIT	7	6	5	4	3	2	1	0
NAME	-	VPChg[2:0]			IPChg[1:0]		ChgDone[1:0]	
<b>VPChg[2:0]</b>	Pre-charge voltage threshold setting 000 = 2.10V 001 = 2.25V 010 = 2.40V 111 = 2.55V 100 = 2.70V 101 = 2.85V 110 = 3.00V 111 = 3.15V							
<b>IPChg[1:0]</b>	Pre-charge current setting 00 = 0.05 x I <sub>FChg</sub> 01 = 0.1 x I <sub>FChg</sub> 10 = 0.2 x I <sub>FChg</sub> 11 = 0.3 x I <sub>FChg</sub>							
<b>ChgDone[1:0]</b>	Charge Done Threshold Setting 00 = 0.05 x I <sub>FChg</sub> 01 = 0.1 x I <sub>FChg</sub> 10 = 0.2 x I <sub>FChg</sub> 11 = 0.3 x I <sub>FChg</sub>							

\*Register is reset to default value upon CHGIN rising edge.

**Table 16. ChTmr Register (0x0C)**

ADDRESS:	0x0C							
MODE:	Read/Write* or Ready-Only if Write-Protect Enabled (see Table 38)							
BIT	7	6	5	4	3	2	1	0
NAME	ChgAutoStp		ChpAutoReSta		MtChgTmr[1:0]		PChgTmr[1:0]	
<b>ChgAutoStp</b>	Charger Auto-Stop. Controls the transition from Maintain Charger to Maintain Charger Done. 0 = Auto-stop disabled. 1 = Auto-stop enabled.							
<b>ChgAutoReSta</b>	Charger Auto-Restart Control 0 = Charger remains in maintain charge done even when VBAT is less than charge restart threshold (see Charger state diagram) 1 = Charger automatically restarts when VBAT drops below charge restart threshold							
<b>MtChgTmr [1:0]</b>	Maintain Charge Timer Setting 00 = 0min 01 = 15min 10 = 30min 11 = 60min							
<b>FChgTmr[1:0]</b>	Fast-Charge Timer Setting 00 = 75min 01 = 150min 10 = 300min 11 = 600min							
<b>PChgTmr[1:0]</b>	Precharge Timer Setting 00 = 30min 01 = 60min 10 = 120min 11 = 240min							

\*Register is reset to default value upon CHGIN rising edge.

**Table 17. Buck1Cfg Register (0x0D)**

ADDRESS:	0x0D								
MODE:	Read/Write								
BIT	7	6	5	4	3	2	1	0	
NAME	Buck1Seq[2:0] (Read-only)				Buck1En[1:0]		Reserved		Reserved
<b>Buck1Seq[2:0]</b>	Buck1 Enable Configuration (Read-Only) 000 = Disabled 001 = Reserved 010 = Enabled at 0% of Boot/POR Process Delay Control 011 = Enabled at 25% of Boot/POR Process Delay Control 100 = Enabled at 50% of Boot/POR Process Delay Control 101 = Reserved 110 = Reserved 111 = Controlled by Buck1En[1:0] after 100% of Boot/POR Process Delay Control								
<b>Buck1En[1:0]</b>	Buck1 Enable Configuration (effective only when Buck1Seq = 111) 00 = Disabled (Buck1 OUT not actively discharged unless in Hard Reset/ShutDown/Off Mode) 01 = Enabled 10 = Enabled when MPC0 is high (regardless of MPC1) 11 = Enabled when MPC1 is high (regardless of MPC0)								

**Table 18. Buck1VSet Register (0x0E)**

<b>ADDRESS:</b>	0x0E							
<b>MODE:</b>	Read/Write							
<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	Buck1LowEMI	—	Buck1VSet[5:0]					
<b>Buck1LowEMI</b>	Buck1 BLX Rising/Falling Slopes Setting 0 = Normal rising/falling slopes on BLX 1 = Reduce the rising/falling slopes on BLX by a factor of three.							
<b>Buck1VSet [5:0]</b>	Buck1 Output Voltage Setting Linear Scale from 0.8V to 2.375V in 25mV increments 000000 = 0.8V 000001 = 0.825V ... 111111 = 2.375V							

Changes in output voltages are digitally ramped in 25mV increments every 80 $\mu$ s giving a maximum slew rates of 312.5V/s.

**Table 19. Buck2Cfg Register (0x0F)**

<b>ADDRESS:</b>	0x0F							
<b>MODE:</b>	Read/Write or Read-Only if Write-Protect Enabled (See Table 38)							
<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	Buck2Seq[2:0] (Read-only)			Buck2En[1:0]		Reserved	Reserved	
<b>Buck2Seq[2:0]</b>	Buck2 Enable Configuration (Read-only) 000 = Disabled 001 = Reserved 010 = Enabled at 0% of Boot/POR Process Delay Control 011 = Enabled at 25% of Boot/POR Process Delay Control 100 = Enabled at 50% of Boot/POR Process Delay Control 101 = Reserved 110 = Reserved 111 = Controlled by Buck2En [1:0] after 100% of Boot/POR Process Delay Control							
<b>Buck2En[1:0]</b>	Buck2 Enable Configuration (effective only when Buck2Seq = 111) 00 = Disabled (Buck2 OUT not actively discharged unless in Hard Reset/ShutDown/Off Mode) 01 = Enabled 10 = Enabled when MPC0 is high (regardless of MPC1) 11 = Enabled when MPC1 is high (regardless of MPC0)							

**Table 20. Buck2VSet Register (0x10)**

<b>ADDRESS:</b>	0x10							
<b>MODE:</b>	Read/Write or Read-Only if WriteProtect Enabled (see Table 38)							
<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	Buck2LowEMI	—	Buck2VSet[5:0]					
<b>Buck2LowEMI</b>	Buck1 BLX Rising/Falling Slopes Setting 0 = Normal rising/falling slopes on BLX 1 = Reduce the rising/falling slopes on BLX by a factor of three.							
<b>Buck2VSet [5:0]</b>	Buck2 Output Voltage Setting Linear Scale from 0.8V to 3.95V in 50mV increments 000000 = 0.80V 000001 = 0.85V ... 111111 = 3.95V							

Changes in output voltages are digitally ramped in 50mV increments every 40µs giving a maximum slew rates of 1250V/s.

**Table 21. Buck1/2ISet Register (0x11)**

<b>ADDRESS:</b>	0x11							
<b>MODE:</b>	Read/Write							
<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	Buck2ISet[3:0]				Buck1ISet[3:0]			
<b>Buck2ISet[3:0]</b>	Buck2 Inductor Peak current setting. 25mA step 0000 = Reserved 0001 = Reserved 0010 = 50mA ... 1111 = 375mA							
<b>Buck1ISet[3:0]</b>	Buck1 Inductor Peak Current Setting. 25mA step 0000 = Reserved 0001 = Reserved 0010 = 50mA ... 1111 = 375mA							

**Table 22. LDO1Cfg Register (0x12)**

ADDRESS:	0x12							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	LDO1Seq[2:0] (Read Only)			—	LDO1Act DSC	LDO1En[1:0]		LDO1Mode
<b>LDO1Seq[2:0]</b>	LDO1 Enable Configuration (Read-only) 000 = Disabled 001 = Enabled always when BAT/SYS is present 010 = Enabled at 0% of Boot/POR Process Delay Control 011 = Enabled at 25% of Boot/POR Process Delay Control 100 = Enabled at 50% of Boot/POR Process Delay Control 101 = Disabled 110 = Disabled 111 = Controlled by LDO1En[1:0] after 100% of Boot/POR Process Delay Control							
<b>LDO1ActDSC</b>	LDO1 Active Discharge Control 0: LDO1 output will be actively discharged only in HardReset mode 1: LDO1 output will be actively discharged in HardReset mode and also when its Enable goes Low. The active discharge circuit will continue to draw additional quiescent current as long as this bit is set to 1, even when the LDO is disabled. (See EC table.)							
<b>LDO1En[1:0]</b>	LDO1 Enable Configuration (effective only when LDO1Seq = 111) 00 = Disabled 01 = Enabled 10 = Enabled when MPC0 is high (regardless of MPC1) 11 = Enabled when MPC1 is high (regardless of MPC0)							
<b>LDO1Mode</b>	LDO1 Mode Control 0 = Normal LDO operating mode 1 = Load switch mode. FET is either fully ON or OFF depending on state of LDO1En. When FET is ON, the output is unregulated. This setting is internally latched and can change only when the LDO is disabled.							

**Table 23. LDO1VSet Register (0x13)**

ADDRESS:	0x13							
MODE:	Read/Write or Read-Only if WriteProtect Enabled (see Table 38)							
BIT	7	6	5	4	3	2	1	0
NAME	-	-	-	LDO1Vset[4:0]				
<b>LDO1VSet[4:0]</b>	LDO1 Output Voltage Setting Linear Scale from 0.8V to 3.6V in 100mV increments 00000 = 0.8V 00001 = 0.9V ... 11100 = 3.6V >11101 = N/A							

**Table 24. LDO2Cfg Register (0x14)**

ADDRESS:	0x14							
MODE:	Read/Write or Read-Only if Write-Protect Enabled (See Table 38)							
BIT	7	6	5	4	3	2	1	0
NAME	LDO2Seq[2:0] (Read Only)			—	LDO2Act DSC	LDO2En[1:0]		LDO2 Mode
<b>LDO2Seq[2:0]</b>	LDO2 Enable Configuration (Read only) 000 = Disabled 001 = Enabled always when BAT/SYS is present 010 = Enabled at 0% of Boot/POR Process Delay Control 011 = Enabled at 25% of Boot/POR Process Delay Control 100 = Enabled at 50% of Boot/POR Process Delay Control 101 = Disabled 110 = Disabled 111 = Controlled by LDO2En[1:0] after 100% of Boot/POR Process Delay Control							
<b>LDO2ActDSC</b>	LDO2 Active Discharge Control 0 = LDO2 output will be actively discharged only in HardReset mode 1 = LDO2 output will be actively discharged in HardReset mode and also when its Enable goes Low. The active discharge circuit will continue to draw additional quiescent current as long as this bit is set to 1, even when the LDO is disabled. (See <i>Electrical Characteristics</i> table.)							
<b>LDO2En[1:0]</b>	LDO2 Enable Configuration (effective only when LDO2Seq = 111) 00 = Disabled – LDO's OUT not actively discharged unless HardReset/ShutDown/Off Mode 01 = Enabled 10 = Enabled when MPC0 is high (regardless of MPC1) 11 = Enabled when MPC1 is high (regardless of MPC0)							
<b>LDO2Mode</b>	LDO2 Mode Control 0 = Normal LDO operating mode 1 = Load switch mode. FET is either fully ON or OFF depending on state of LDO2En. When FET is ON, the output is unregulated. This setting is internally latched and can change only when the LDO is disabled.							

**Table 25. LDO2VSet Register (0x15)**

ADDRESS:	0x15							
MODE:	Read/Write or Read-Only if WriteProtect Enabled (see Table 38)							
BIT	7	6	5	4	3	2	1	0
NAME	—	—	—	LDO2Vset[4:0]				
<b>LDO2VSet[4:0]</b>	LDO2 Output Voltage Setting Linear Scale from 0.9V to 4.0V in 100mV increments 00000 = 0.9V 00001 = 1.0V ... 11111 = 4.0V							

**Table 26. LDO3Cfg Register (0x16)**

ADDRESS:	0x16							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	LDO3Seq[2:0] (Read-Only)		—	LDO3Act DSC	LDO3En[1:0]		LDO3 Mode	
<b>LDO3Seq[2:0]</b>	LDO3 Enable Configuration (Read only) 000 = Disabled 001 = Enabled always when BAT/SYS is present 010 = Enabled at 0% of Boot/POR Process Delay Control 011 = Enabled at 25% of Boot/POR Process Delay Control 100 = Enabled at 50% of Boot/POR Process Delay Control 101 = Disabled 110 = Disabled 111 = Controlled by LDO3En[1:0] after 100% of Boot/POR Process Delay Control							
<b>LDO3ActDSC</b>	LDO3 Active Discharge Control 0 = LDO3 output will be actively discharged only in HardReset mode 1 = LDO3 output will be actively discharged in HardReset modes and also when its Enable goes Low. The active discharge circuit will continue to draw additional quiescent current as long as this bit is set to 1, even when the LDO is disabled. (See EC table.)							
<b>LDO3En[1:0]</b>	LDO3 Enable Configuration (effective only when LDO3Seq == 111) 00 = Disabled. LDO's OUT not actively discharged unless in HardReset/ShutDown/Off Mode 01 = Enabled 10 = Enabled when MPC0 is high (regardless of MPC1) 11 = Enabled when MPC1 is high (regardless of MPC0)							
<b>LDO3Mode</b>	LDO3 Mode Control 0 = Normal LDO operating mode 1 = Load switch mode. FET is either fully ON or OFF depending on state of LDO3En. When FET is ON, the output is unregulated. This setting is internally latched and can change only when the LDO is disabled.							

**Table 27. LDO3VSet Register (0x17)**

ADDRESS:	0x17							
MODE:	Read/Write or Read-Only if WriteProtect Enabled (see Table 38)							
BIT	7	6	5	4	3	2	1	0
NAME	—	—	—	LDO3Vset[4:0]				
<b>LDO3VSet[4:0]</b>	LDO3 Output Voltage Setting Linear Scale from 0.9V to 4.0V in 100mV increments 00000 = 0.9V 00001 = 1.0V ... 11111 = 4.0V							



**Table 28. ThrmCfg Register (0x18)**

ADDRESS:	0x18							
MODE:	Read/Write* or Read-Only if WriteProtect Enabled (see Table 38)							
BIT	7	6	5	4	3	2	1	0
NAME	T1T2IFchg[2:0]			T2T3IFchg[2:0]			ThermEn[1:0]	
<b>T1T2IFchg[2:0]</b>	Fast Charge Current for T1-T2 Temperature Zone 000 = 0.2 x I <sub>FChg</sub> 001 = 0.3 x I <sub>FChg</sub> 010 = 0.4 x I <sub>FChg</sub> 011 = 0.5 x I <sub>FChg</sub> 100 = 0.6 x I <sub>FChg</sub> 101 = 0.7 x I <sub>FChg</sub> 110 = 0.8 x I <sub>FChg</sub> 111 = 1 x I <sub>FChg</sub>							
<b>T2T3IFchg[2:0]</b>	Fast Charge Current for T2-T3 Temperature Zone 000 = 0.2 x I <sub>FChg</sub> 001 = 0.3 x I <sub>FChg</sub> 010 = 0.4 x I <sub>FChg</sub> 011 = 0.5 x I <sub>FChg</sub> 100 = 0.6 x I <sub>FChg</sub> 101 = 0.7 x I <sub>FChg</sub> 110 = 0.8 x I <sub>FChg</sub> 111 = 1 x I <sub>FChg</sub>							
<b>ThermEn[1:0]</b>	Thermistor Monitoring Mode 00 = Thermistor Monitoring Disabled 01 = Charging enabled between T1 and T3 10 = Charging enabled between T1 and T4 11 = Charging enabled between T1 and T4, Voltage reduced below T2 and above T3							

\*Register is reset to default value upon CHGIN rising edge.

**Table 29. ThrmCfg Register (0x19)**

<b>ADDRESS:</b>	0x19							
<b>MODE:</b>	Read/Write* or Read-Only if WriteProtect Enabled (see Table 38)							
<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	—	—	—	—	—	T3T4IFchg[2:0]		
<b>T3T4IFchg[2:0]</b>	Fast Charge Current for T3-T4 Temperature Zone 000 = 0.2 x I <sub>FChg</sub> 001 = 0.3 x I <sub>FChg</sub> 010 = 0.4 x I <sub>FChg</sub> 011 = 0.5 x I <sub>FChg</sub> 100 = 0.6 x I <sub>FChg</sub> 101 = 0.7 x I <sub>FChg</sub> 110 = 0.8 x I <sub>FChg</sub> 111 = 1 x I <sub>FChg</sub>							

\*Register is reset to default value upon CHGIN rising edge.

**Table 30. MONCfg Register (0x1A)**

<b>ADDRESS:</b>	0x1A							
<b>MODE:</b>	Read/Write							
<b>BIT</b>	7	6	5	4	3	2	1	0
<b>NAME</b>	—	—	MONRatioCfg[1:0]		MONHiZ	MONCtr[2:0]		
<b>MONRatioCfg</b>	MON Resistive Partition Selector 00 = 4:1 01 = 3:1 10 = 2:1 11 = 1:1							
<b>MONHiZ</b>	MON OFF MODE condition 0 = Pulled LOW by 100k pull-down resistor 1 = Hi-Z							
<b>MONCtr[2:0]</b>	MON Pin Source selection (40µs BBM after any change of MONCtr) 000 = MON is not connected to any internal node and its state depends on MONHiZ 001 = MON connected to a resistive partition of BATT 010 = MON connected to a resistive partition of SYS 011 = MON connected to a resistive partition of BUCK1 OUT 100 = MON connected to a resistive partition of BUCK2 OUT 101 = MON connected to a resistive partition of LDO1 OUT 110 = MON connected to a resistive partition of LDO2 OUT 111 = MON connected to a resistive partition of LDO3 OUT							

**Table 31. BootCfg Register (0x1B)**

ADDRESS:	0x1B							
MODE:	Read-Only							
BIT	7	6	5	4	3	2	1	0
NAME	PwrRstCfg[3:0]				SftRstCfg	BootDly[1:0]		ChgAlwTry
<b>PwrRstCfg [3:0]</b>	See Table 1							
<b>SftRstCfg</b>	Soft Reset Register Default 0 = Registers do not reset to default values on soft reset 1 = Registers reset to default values on soft reset							
<b>BootDly[1:0]</b>	Reset Delay Control (see Figure 2a, 2b) 00 = 80ms 01 = 120ms 10 = 220ms 11 = 420ms							
<b>ChgAlwTry</b>	UVLO Automatic Retry If SYS UVLO condition occurs during boot process: 0 = Part latches off until CHGIN is removed and replaced 1 = Part retries after delay							

**Table 32. PinStat Register (0x1C)**

ADDRESS:	0x1C								
MODE:	Read Only								
BIT	7	6	5	4	3	2	1	0	
NAME	ILim_T[2:0]				-	PFN1	PFN2	MPC1	MPC0
<b>ILim_T[2:0]</b>	Monitor of The Input limiter Current Setting 000 = Input Limiter Off 001 = 100mA 010 = 500mA 100 = 1A								
<b>PFN1</b>	PFN1 Input State 0 = pin low 1 = pin high								
<b>PFN2</b>	PFN2 In/Out State 0 = pin low 1 = pin high								
<b>MPC1</b>	MPC1 Input State 0 = pin low 1 = pin high								
<b>MPC0</b>	MPC0 Input State 0 = pin low 1 = pin high								

**Table 33. Buck1/2Extra Control Register (0x1D)**

ADDRESS:	0x1D							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	Buck2IAdptEnb	Buck2Fst	Buck2 ActDSC	Buck2 FFET	Buck1IAdptEnb	Buck1Fst	Buck1 ActDSC	Buck1 FFET
<b>Buck2IAdptEnb</b>	Buck 2 Peak Current 0 = Enable adaptive peak current 1 = Peak current set by Buck2ISet[3:0]							
<b>Buck2Fst</b>	Buck2 Fast Start 0 = Normal startup current limit 1 = Double the startup current to reduce the startup time by half							
<b>Buck2ActDSC</b>	Buck2 Active Discharge Control 0 = Buck2 output will be actively discharged only in HardReset mode 1 = Buck2 output will be actively discharged in HardReset mode and also when its Enable goes Low. Note, when BuckActDSC=1, the active discharge circuit will remain active and draw additional quiescent current even when Buck2 is disabled.							
<b>Buck2FFET</b>	Buck2 Force FET scaling (reduces active FET size by 50% and increases efficiency for loads <100mA.) 0 = FET Scaling disabled 1 = FET Scaling enabled							
<b>Buck1IAdptEnb</b>	Buck 1 Peak Current 0 = Enable adaptive peak current 1 = Peak current set by Buck1ISet[3:0]							
<b>Buck1Fst</b>	Buck1 Fast Start 0 = Normal startup current limit 1 = Double the startup current to reduce the startup time by half							
<b>Buck1ActDSC</b>	Buck1 Active Discharge Control 0 = Buck1 output will be actively discharged only in HardReset mode 1 = Buck1 output will be actively discharged in HardReset mode and also when its Enable goes Low. Note, when BuckActDSC=1, the active discharge circuit will remain active and draw additional quiescent current even when Buck2 is disabled.							
<b>Buck1FFET</b>	Buck1 Force FET Scaling (reduces active FET size by 50% and increases efficiency for loads <100mA.) 0 = FET Scaling only enabled during the Buck1 Turn-On Sequence 1 = FET Scaling enabled during the Buck1 Turn-On Sequence and also in the Buck1 Steady ON state							

**Table 34. PwrCfg Register (0x1E)**

<b>ADDRESS:</b>	0x1E							
<b>MODE:</b>	Read/Write							
<b>BIT</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>NAME</b>	PFNx ResEna	–	–	–	–	–	–	StayOn
<b>PFNxResEna</b>	PFN_ PFNx Automatic Internal Pull-Up/Pull-Down Enable 0 = No internal pullup/pulldown 1 = Automatic internal pullup/pulldown as per Table 1							
<b>StayOn</b>	This bit is used to ensure that the processor booted correctly. This bit must be set within 5s of power-on to prevent the part from shutting down and returning to the power-off condition. This bit has no effect after being set. 0 = Shut down 5s after power-on 1 = Stay on							

**Table 35. PwrCmd Register (0x1F)**

<b>ADDRESS:</b>	0x1F							
<b>MODE:</b>	Read/Write							
<b>BIT</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>NAME</b>	PWR_CMD[7:0]							
<b>PWR_CMD [7:0]</b>	Power Command Register Writing the following values issues the command listed: 0xB2 = places the part in off mode 0xC3 = issues a hard reset (power cycle) 0xD4 = issues a soft reset (reset pulse only)  After the written value has been validated by the internal logic, this register is cleared automatically. Any other commands will be ignored. See Table 1 for the available PwrCmd for each PwrRstCfg value.							

## Applications Information

The buck converters of the MAX14745 are optimized for use with a tiny inductor and small ceramic capacitors. The correct selection of external components ensures high efficiency, low output ripple, and fast transient response.

### Inductor Selection

A 2.2 $\mu$ H inductor is recommended for use with the MAX14745 buck converters. [Table 36](#) lists recommended inductors for use depending on whether a given application requires highest efficiency, or a compromise between high efficiency and small size.

### Output Capacitor Selection

The output capacitors of the MAX14745 buck converters are required to keep the output voltage ripple small and to ensure regulation loop stability. A 10 $\mu$ F output capacitor with Buck\_ISet[3:0] = 150mA and Buck\_IAdptEnb = 0 is suggested to cover all the possible output voltage/load current cases. If a lower output cap are needed, please refer to [Table 37](#) for the minimum allowed capacitor size). Ceramic capacitors are recommended due to their small size and low ESR and care should be taken to ensure that the selected capacitor maintains its capacitance over temperature and voltage bias. Capacitors with X5R or X7R temperature characteristics perform well in most applications.

### Input Capacitor Selection

The input capacitors of the buck converters reduce the current peaks drawn from the battery or input power source and reduces switching noise in the IC. The impedance of the input capacitors at the switching frequency should be kept very low. Ceramic capacitors are recommended due to their small size and low ESR. Make sure the capacitor maintains its capacitance over temperature and DC bias. Capacitors with X5R or X7R temperature characteristics perform well in most applications.

### PCB Layout and Routing

High switching frequencies and large peak currents make PCB layout a very important part of design. Good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors. Connect the inductor, input capacitor, and output capacitor as close together as possible, and keep their traces short, direct, and wide. Connect the two GND pins under the IC and directly to the grounds of the input and output capacitors. Keep noisy traces, such as the LX node, as short as possible.

**Table 36. Suggested Inductors**

MANUFACTURER	SERIES	INDUCTANCE ( $\mu$ H)	DC RESISTANCE (m $\Omega$ )	CURRENT RATING (mA)	DIMENSIONS L x W x H (mm)	NOTES
BOURNS	SRP2010	2.2	168	2200	2.0 x 1.6 x 1.0	Optimized for highest efficiency
MURATA	MFD160810	2.2	310	1400	1.6 x 0.8 x 1.0	Optimized for smallest size

**Table 37. Output Capacitor Values\***

BUCK_ISET[3:0]	OUTPUT VOLTAGE (V)	OUTPUT CAPACITOR MINIMUM VALUES ( $\mu$ F)
<150mA	>1.4V	2.2
<200mA	>1.2V	4.7
<175mA	>0.8	10

\*Minimum Output Capacitor Values are given for L = 2.2 $\mu$ H

Table 38. Register Bit Default Values

REGISTER BITS	MAX14745A	MAX14745C	MAX14745D	MAX14745E	MAX14745F	MAX14745G	MAX14745H	MAX14745J	MAX14745K
Buck1IZC Set[1:0]	20mA	30mA	20mA	20mA	20mA	30mA	10mA	20mA	20mA
Buck1VSet[5:0]	1.2V	1.95V	1.8V	1.2V	1.2V	1.8V	0.95V	1.2V	1.2V
Buck1ISet[3:0]	125mA	150mA	125mA	150mA	125mA	125mA	150mA	150mA	150mA
Buck1En[1:0]	Disabled	Disabled	Disabled	Enabled	Disabled	Disabled	Disabled	Disabled	Disabled
Buck1Seq[2:0]	Buck1En	0% Boot	Buck1En	25% Boot	Buck1En	0% Boot	Buck1En	Buck1En	Buck1En
Buck2IZC Set[1:0]	20mA	40mA	30mA	30mA	20mA	20mA	30mA	30mA	30mA
Buck2VSet[5:0]	1.8V	3.3V	3V	1.8V	1.8V	1.2V	2V	2.85V	1.8V
Buck2ISet[3:0]	125mA	150mA	300mA	150mA	125mA	125mA	150mA	150mA	150mA
Buck2En[1:0]	Disabled	Disabled	Disabled	Enabled	Disabled	Disabled	Enabled	Enabled	Enabled
Buck2Seq[2:0]	0% Boot	50% Boot	50% Boot	25% Boot	0% Boot	0% Boot	25% boot	25% Boot	0% Boot
LDO1Mode	LDO	LDO	Switch	LDO	LDO	LDO	LDO	LDO	LDO
LDO1VSet[4:0]	3V	1.8V	1.8V	1.8V	3V	3V	3.1V	1.8V	1.8V
LDO1En[1:0]	Disabled	Enabled	Disabled	Enabled	Disabled	Disabled	Disabled	Disabled	Disabled
LDO1Seq[2:0]	LDO1En	25% Boot	LDO1En	Always On	LDO1En	LDO1En	LDO1En	LDO1En	LDO1En
LDO2Mode	Switch	LDO	Switch	LDO	Switch	Switch	Switch	LDO	LDO
LDO2VSet[4:0]	3.5V	1.8V	1.8V	2.8V	3.5V	3.5V	1.8V	1.2V	3V
LDO2En[1:0]	Disabled	Enabled	Disabled	Enabled	Disabled	Disabled	Disabled	Disabled	Disabled
LDO2Seq[2:0]	LDO2En	25% Boot	LDO2En	50% Boot	LDO2En	LDO2En	LDO2En	LDO2En	LDO2En
LDO3Mode	Switch	LDO	Switch	LDO	Switch	Switch	LDO	LDO	LDO
LDO3VSet[4:0]	3.5V	1.8V	1.8V	3.3V	3.5V	3.5V	1.8V	3V	3V
LDO3En[1:0]	Disabled	Enabled	Disabled	Enabled	Disabled	Disabled	Disabled	Disabled	Disabled
LDO3Seq[2:0]	LDO3En	25% Boot	LDO3En	LDO3En	LDO3En	LDO3En	LDO3En	LDO3En	LDO3En
VPchg[2:0]	2.85V	3.00V	2.85V	3.00V	2.85V	2.85V	3.00V	3.00V	3.00V
IPCchg[1:0]	0.10 x IFChg	0.10 x IFChg	0.20 x IFChg	0.20 x IFChg	0.10 x IFChg	0.10 x IFChg	0.10 x IFChg	0.10 x IFChg	0.20 x IFChg
PCchgTmr[1:0]	30min	120min	30min	30min	30min	30min	60min	30min	30min
FCchgTmr[1:0]	300min	150min	600min	300min	300min	300min	300min	150min	300min
MfchgTmr[1:0]	60min	15min	0min	30min	60min	60min	0min	0min	30min
BatReg[3:0]	4.20V	4.40V	4.35V	4.20V	4.20V	4.20V	4.30V	4.20V	4.35V

Table 38. Register Bit Default Values (continued)

REGISTER BITS	MAX14745A	MAX14745C	MAX14745D	MAX14745E	MAX14745F	MAX14745G	MAX14745H	MAX14745J	MAX14745K
BatReChg[1:0]	-120mV Enabled	-220mV Enabled	-120mV Enabled	-120mV Enabled	-100mV Enabled	-100mV Enabled	-150mV Enabled	-150mV Disabled	-100mV Enabled
ChgEn	0.05 x IFChg Enabled	0.10 x IFChg Enabled	0.05 x IFChg Enabled	0.20 x IFChg Enabled	0.05 x IFChg Enabled	0.05 x IFChg Enabled	0.05 x IFChg Enabled	0.05 x IFChg Enabled	0.10 x IFChg Enabled
ChgDone[1:0]	0.05 x IFChg Enabled	0.10 x IFChg Enabled	0.05 x IFChg Enabled	0.20 x IFChg Enabled	0.05 x IFChg Enabled	0.05 x IFChg Enabled	0.05 x IFChg Enabled	0.05 x IFChg Enabled	0.10 x IFChg Enabled
ChgAutoStp	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled
ChgAutoSta	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled
FishBatDis	Done	Charge	Charge	Charge	Done	Done	Charge	Charge	Charge
ThermEn[1:0]	Thermistor	JEITA 1	Thermistor	Thermistor	JEITA 1	JEITA 1	JEITA 1	Thermistor	Thermistor
T1_T2_IFchg[2:0]	1.0 x IFChg	0.5 x IFChg	0.5 x IFChg	1.0 x IFChg	1.0 x IFChg	1.0 x IFChg	1.0 x IFChg	0.2 x IFChg	0.2 x IFChg
T2_T3_IFchg[2:0]	1.0 x IFChg	1.0 x IFChg	1.0 x IFChg	1.0 x IFChg	1.0 x IFChg	1.0 x IFChg	1.0 x IFChg	1.0 x IFChg	1.0 x IFChg
T3_T4_IFchg[2:0]	1.0 x IFChg	0.5 x IFChg	0.2 x IFChg	1.0 x IFChg	1.0 x IFChg	1.0 x IFChg	1.0 x IFChg	0.2 x IFChg	0.2 x IFChg
ChgAlwTry	Retry	Latch Off	Latch Off	Retry	Retry	Retry	Latch Off	Retry	Retry
ILimCntl[1:0]	500mA	500mA	500mA	500mA	500mA	500mA	500mA	100mA	500mA
PwrRstCfg[3:0]	KIN (0110)	CR Low (0101)	On/Off (0000)	KIN (0110)	KIN (0110)	KIN (0110)	Custom1 (0111)	Custom2 (1000)	KIN(0110)
PFNxResEna	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled
BootDly[1:0]	(120 + 34)ms	(120 + 34)ms	(420 + 34)ms	(420 + 34)ms	(120 + 34)ms	(120 + 34)ms	(120 + 34)ms	(120 + 34)ms	(80 + 34)ms
SftRstCfg	Hold	Reset	Reset	Reset	Hold	Hold	Reset	Reset	Reset
SysMin[2:0]	3.6V	3.6V	3.6V	3.6V	3.6V	3.6V	3.6V	3.8V	3.6V
Write-Protect	Writable	Writable	Writable	Writable	Writable	Writable	Writable	Writable	Writable
StayOn	Stay On	Stay On	Stay On	Stay On	Stay On	Stay On	Stay On	Stay On	Stay On
T1, T2, T3, T4	0, 10, 25, 45°C	0, 10, 25, 45°C	0, 10, 45, 60°C	0, 10, 45, 60°C	0, 10, 25, 45 °C	0, 10, 25, 45 °C	0, 10, 45, 60 °C	0, 10, 45, 60°C	0, 10, 45, 60°C



Table 39. Register Default Values

REGISTER ADDRESS	REGISTER NAME	MAX14745A	MAX14745C	MAX14745D	MAX14745E	MAX14745F	MAX14745G	MAX14745H	MAX14745J	MAX14745K
0x00	ChipId	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02
0x01	ChipRev	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x07	IntMaskA	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x08	IntMaskB	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x09	ILimCntl	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x41	0x02
0x0A	ChgCntlA	0x27	0x6F	0x2D	0x27	0x27	0x27	0x4B	0x46	0x2D
0x0B	ChgCntlB	0x54	0x65	0x58	0x6A	0x54	0x54	0x64	0x64	0x69
0x0C	ChTmr	0xF8	0xD6	0xCC	0xE8	0xF8	0xF8	0xC9	0xC4	0xE8
0x0D	Buck1Cfg	0xE1	0x42	0xE1	0x69	0xE1	0x42	0xE0	0xE1	0xE1
0x0E	Buck1VSet	0x10	0x2E	0x28	0x10	0x10	0x28	0x06	0x10	0x10
0x0F	Buck2Cfg	0x41	0x83	0x82	0x6A	0x41	0x41	0x6A	0x6A	0x4A
0x10	Buck2Vset	0x14	0x32	0x2C	0x14	0x14	0x08	0x18	0x29	0x14
0x11	BucklSet	0x55	0x66	0xC5	0x66	0x55	0x55	0x66	0x66	0x66
0x12	LDO1Cfg	0xE0	0x62	0xE1	0x22	0xE0	0xE0	0xE0	0xE0	0xE0
0x13	LDO1VSet	0x16	0x0A	0x0A	0x0A	0x16	0x16	0x17	0x0A	0x0A
0x14	LDO2Cfg	0xE1	0x62	0xE1	0x82	0xE1	0xE1	0xE1	0xE0	0xE0
0x15	LDO2VSet	0x1A	0x09	0x09	0x13	0x1A	0x1A	0x09	0x03	0x15
0x16	LDO3Cfg	0xE1	0x62	0xE1	0xE2	0xE1	0xE1	0xE0	0xE0	0xE0
0x17	LDO3VSet	0x1A	0x09	0x09	0x18	0x1A	0x1A	0x09	0x15	0x15
0x18	THRMCFA	0xFD	0x7E	0x7D	0xFD	0xFE	0xFE	0xFE	0x1D	0x1D
0x19	THRMCFB	0x07	0x03	0x00	0x07	0x07	0x07	0x07	0x00	0x00
0x1A	MONCFG	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x1B	BOOTCFG	0x63	0x5A	0x0E	0x2F	0x63	0x63	0x7A	0x8B	0x69
0x1D	Buck1/2Extra	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x1E	PwrCfg	0x81	0x81	0x81	0x81	0x81	0x81	0x81	0x81	0x81
0x1F	PwrCmd	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
<b>MAX14745AEWX+</b>	-40°C to +85°C	36 WLP
MAX14745AEWX+T	-40°C to +85°C	36 WLP
<b>MAX14745BEWX+*</b>	-40°C to +85°C	36 WLP
MAX14745BEWX+T*	-40°C to +85°C	36 WLP
<b>MAX14745CEWX+</b>	-40°C to +85°C	36 WLP
MAX14745CEWX+T	-40°C to +85°C	36 WLP
<b>MAX14745DEWX+</b>	-40°C to +85°C	36 WLP
MAX14745DEWX+T	-40°C to +85°C	36 WLP
<b>MAX14745EEWX+</b>	-40°C to +85°C	36 WLP
MAX14745EEWX+T	-40°C to +85°C	36 WLP
<b>MAX14745FEWX+</b>	-40°C to +85°C	36 WLP
MAX14745FEWX+T	-40°C to +85°C	36 WLP
<b>MAX14745GEWX+</b>	-40°C to +85°C	36 WLP
MAX14745GEWX+T	-40°C to +85°C	36 WLP
<b>MAX14745HEWX+*</b>	-40°C to +85°C	36 WLP
MAX14745HEWX+T*	-40°C to +85°C	36 WLP
<b>MAX14745JEWX+</b>	-40°C to +85°C	36 WLP
MAX14745JEWX+T	-40°C to +85°C	36 WLP
<b>MAX14745KEWX+*</b>	-40°C to +85°C	36 WLP
MAX14745KEWX+T*	-40°C to +85°C	36 WLP

+Denotes a lead(Pb)-free package/RoHS-compliant package.

T = Tape and reel.

\*Future Product—contact factory for availability.

See [Table 38](#) and [Table 39](#) for the device differences.

## Chip Information

PROCESS: BiCMOS

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/16	Initial release	—
1	10/16	Added new part numbers and corrected various errors	4–7, 15, 16, 24, 26, 31, 47, 50, 53, 58, 59
2	11/16	Changed future product status of MAX14745C/MAX14745D and various updates	5, 23–25, 36, 46–48, 60
3	3/17	Removed future product asterisks from MAX14745EEWX+ and MAX14745EEWX+T in the <i>Ordering Information</i> table.	61
4	5/17	MAX14745E no longer future product. Updated Table 38 and Table 39	58–61
5	6/17	Removed future product asterisks from MAX14745FEWX+ and MAX14745FEWX+T in the <i>Ordering Information</i> table.	61
6	8/17	Updated Tables 38, 39, and added MAX14745GEWX, MAX14745GEWX+T, MAX14745HEWX, MAX14745HEWX+T to the <i>Ordering Information</i> table	63–66
7	10/17	Removed future product asterisks from MAX14745GEWX+ and MAX14745GEWX+T in the <i>Ordering Information</i> table.	66
8	2/18	Added new parts to the <i>Ordering Information</i> table. Updated Tables 23, and 38–39	54, 63–66

For information on other Maxim Integrated products, visit Maxim Integrated's website at [www.maximintegrated.com](http://www.maximintegrated.com).

Maxim Integrated cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim Integrated product. No circuit patent licenses are implied. Maxim Integrated reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.