

# **FURUNO Multi-GNSS Disciplined Oscillator**

Models GF-8704, GF-8705

# **Hardware Specifications**

(Document No. SE17-410-001-00)



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# **Revision History**

| Version | Changed contents                                    | Date       |
|---------|---|------------|
| 0       | Initial release. All revised from G14-000-10-030-1. | 2017.02.27 |



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#### 1 Outline

GF-8704 and GF-8705 (GF-8704/05) are FURUNO Multi-GNSS Disciplined Oscillators (GNSSDO). Main features are as follows:

- Supports GPS, GLONASS, SBAS and QZSS<sup>1)</sup>
- Provides highly accurate PPS signal synchronized with UTC
- Provides the clock (10 MHz: VCLK and VCLK\_SIN) synchronized with PPS
- Software upgrade capability by Flash ROM
- Active Anti-jamming capability to suppress effects of CW jammers
- · Multi path mitigation effects
- GPS high sensitivity (-161 dBm (Hot acquisition))
- It is not necessary for user to use the power of high accuracy, high stability and low noise because the LDO is built in.
- These GNSSDO are pin compatible.<sup>2)</sup>

#### Notes:

- 1) These satellite systems are called as GNSS collectively.
- 2) The specifications of the power consumption, PPS and 10 MHz are different.

# 2 Block Diagram

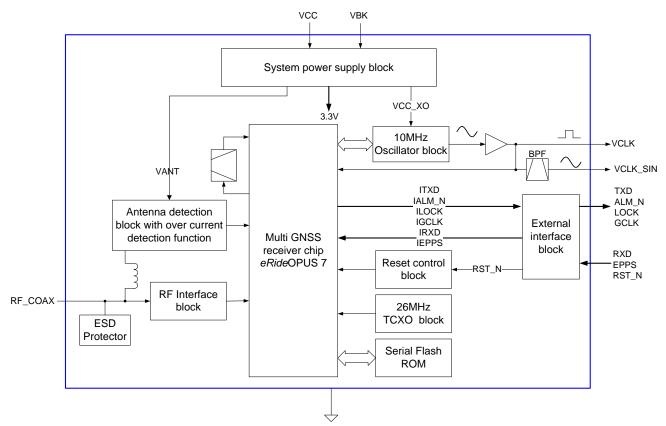


Figure 2.1 GF-8704/05 Block Level Diagram



# 3 GNSS General Specifications

**Table 3.1 General Specifications** 

| Items                     | Description                 | on      | Notes                              |
|---------------------------|-----------------------------|---------|------------------------------------|
|                           | GPS L1C/A                   | 12      |                                    |
| GNSS reception            | GLONASS L1OF                | 10      |                                    |
| capability                | QZSS L1C/A                  | 2       |                                    |
|                           | SBAS L1C/A                  | 2       | WAAS, MSAS, EGNOS, GAGAN           |
| GNSS concurrent reception | GPS, GLONASS,<br>QZSS, SBAS | 26      |                                    |
| Environment robustness    | Active Anti-jamming         | 8CW     |                                    |
| performance               | Multipath Mitigation        | •       |                                    |
| Serial data format        | NMEA                        | •       | Ver. 4.10, 38400 bps <sup>3)</sup> |
| Antenna                   | Active antenna              | •       |                                    |
| Operational limits        | Altitude                    | 18,000m | Compliant with the Wassenaar       |
|                           | Velocity                    | 515 m/s | Arrangement Specifications         |

# Notes:

3) See Protocol Specifications for details.

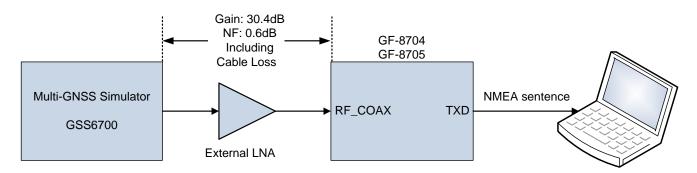


# 4 GNSS General Performance

**Table 4.1 General Performance** 

 $T_A=25$ °C

| Items               | Descripti          | ion      | Notes  |  |  |
|---------------------|--------------------|----------|--|--|--|
|                     | Hot Outdoor        | <5 s     | These are specified with the measurement   |  |  |
| TTFF                | Warm Outdoor       | 35 s     | platform shown in Figure 4.1. Simulator  |  |  |
|                     | Cold Outdoor       | 35 s     | output level is set to -130 dBm.   |  |  |
|                     | Tracking           | -161 dBm |  |  |  |
| CDS consitivity     | Hot Acquisition    | -161 dBm | _  |  |  |
| GPS sensitivity     | Cold Acquisition   | -147 dBm | _  |  |  |
|                     | Reacquisition      | -161 dBm | These are specified with the measurement   |  |  |
|                     | Tracking           | -157 dBm | platform shown in Figure 4.1.  |  |  |
| CLONACS consitivity | Hot Acquisition    | -157 dBm | _  |  |  |
| GLONASS sensitivity | Cold Acquisition   | -143 dBm | _  |  |  |
|                     | Reacquisition      |          | _  |  |  |
| Desition convenue   |                    |          | Open sky <sup>4)</sup> 24 hours continuous static test with GPS only by using recommended antenna              |  |  |
| Position accuracy   | Horizontal Outdoor | 2.0m CEP | Open sky <sup>4)</sup> 24 hours continuous static test with GPS, GLONASS and SBAS by using recommended antenna |  |  |



**Figure 4.1 Measurement Platform** 

#### Notes:

4) Open sky is a environment that is more than 50% of the number of satellites in use with signal level of over 40 dB-Hz



# 5 I/O Signal Description

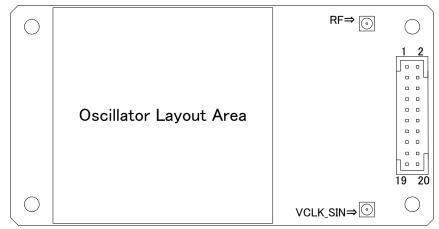


Figure 5.1 Top of View

**Table 5.1 I/O Signal Description** 

|     | Table 5.1 I/O Signal Description |                |                     |   |  |  |  |  |  |  |
|-----|----------------------------------|----------------|---------------------|---|--|--|--|--|--|--|
| #   | Pin Name                         | Туре           | PU/PD <sup>5)</sup> | Description   |  |  |  |  |  |  |
| ,   | DOT 11                           | <b>5</b>       | <b>5</b> "          | External reset signal input pin                       |  |  |  |  |  |  |
| 1   | RST_N                            | Digital input  | Pull-up             | Logic L : Reset                                       |  |  |  |  |  |  |
|     | EDDC                             | Digital inner  | مستعلم السا         | Logic H or Open : Normal operation                    |  |  |  |  |  |  |
| 2   | EPPS                             | Digital input  | Pull-down           | External synchronized PPS input pin                   |  |  |  |  |  |  |
| 3   | RESERVE                          | -              | -                   | Do not connect  |  |  |  |  |  |  |
| 4   | PPS                              | Digital output | -                   | Pulse per second output pin                           |  |  |  |  |  |  |
| _ 5 | GND                              | -              | -                   | Ground  |  |  |  |  |  |  |
| 6   | GCLK                             | Digital output | -                   | Clock output pin (from 4kHz to 40MHz)                 |  |  |  |  |  |  |
| _ 7 | GND                              | -              | -                   | Ground  |  |  |  |  |  |  |
|     |                                  |                |                     | Lock signal output pin <sup>6)</sup>                  |  |  |  |  |  |  |
| 8   | LOCK                             | Digital output | -                   | Logic L : Unlock                                      |  |  |  |  |  |  |
|     |                                  |                |                     | Logic H : Lock  |  |  |  |  |  |  |
| 9   | GND                              | -              | -                   | Ground  |  |  |  |  |  |  |
| 4.0 |                                  | <b>5</b>       |                     | Alarm signal output pin <sup>7)</sup>                 |  |  |  |  |  |  |
| 10  | ALM_N                            | Digital output | -                   | Logic L : Abnormal                                    |  |  |  |  |  |  |
|     | DECEDVE                          |                |                     | Logic H : Normal                                      |  |  |  |  |  |  |
| 11  | RESERVE                          | -              | -                   | Do not connect  |  |  |  |  |  |  |
| 12  | TXD                              | Digital output | -                   | Serial communication output pin                       |  |  |  |  |  |  |
| _13 | GND                              | -              | -                   | Ground  |  |  |  |  |  |  |
| _14 | RXD                              | Digital input  | Pull-up             | Serial communication input pin                        |  |  |  |  |  |  |
| 15  | VBK                              | Power input    | _                   | Backup power supply input pin <sup>8)</sup>           |  |  |  |  |  |  |
|     |                                  | <u>'</u>       |                     | Do not connect if battery backup function is not used |  |  |  |  |  |  |
| 16  | VCLK                             | Digital output | -                   | VCO clock output pin (10MHz) Square pulse             |  |  |  |  |  |  |
| 17  | VCC                              | Power input    | _                   | Main power supply input pin                           |  |  |  |  |  |  |
| 18  | GND                              | -              | _                   | Ground  |  |  |  |  |  |  |
| 19  | VCC                              | Power input    | _                   | Main power supply input pin                           |  |  |  |  |  |  |
| 20  | GND                              | -              | <u>-</u>            | Ground  |  |  |  |  |  |  |
|     | 0.10                             |                |                     | RF signal input connector                             |  |  |  |  |  |  |
|     | DE                               | A I            |                     | Power for antenna pre-amplifier is superimposed       |  |  |  |  |  |  |
| -   | RF                               | Analog input   | -                   | (biased) from this connector.                         |  |  |  |  |  |  |
|     |                                  |                |                     | MMCX connector receptacle /50Ω                        |  |  |  |  |  |  |
|     |                                  |                |                     | VCO clock output pin(10MHz)                           |  |  |  |  |  |  |
| -   | VCLK_SIN                         | Analog output  | -                   | Sin waveform, 9dBm(Typ)                               |  |  |  |  |  |  |
|     |                                  |                |                     | MMCX connector receptacle /50Ω                        |  |  |  |  |  |  |



#### Notes:

- 5) Pull-up and pull-down resistor values are shown in Table 6.3.
- 6) The lock output conditions are shown in Section 8.2.
- 7) The alarm output conditions are shown in Section 8.1.
- 8) The backup power is shown in Section 8.4.

# 6 Electrical Characteristics

# 6.1 Absolute Maximum Rating

The lists of absolute maximum ratings are specified over operating case temperature shown in Table 10.1. Stresses beyond those listed under those range may cause permanent damage to module.

**Table 6.1 Absolute Maximum Rating** 

| Table 6.1 Absolute Maximum Nating |                  |      |      |      |                                |  |  |  |  |
|-----------------------------------|------------------|------|------|------|--------------------------------|--|--|--|--|
| Items                             | Symbol           | Min. | Max. | Unit | Notes                          |  |  |  |  |
| VCC supply voltage                | V <sub>CC</sub>  | -0.3 | 7.0  | V    |                                |  |  |  |  |
| VBK supply voltage                | $V_{BK}$         | -0.3 | 4.0  | V    |                                |  |  |  |  |
| VANT supply voltage               | $V_{ANT}$        | -0.3 | 6.0  | V    |                                |  |  |  |  |
| Other wine DC velters             | $V_{IN}$         | -0.5 | 6.5  | V    | Input voltage at power ON/OFF  |  |  |  |  |
| Other pins DC voltage             | V <sub>OUT</sub> | -0.5 | 3.8  | V    | Output voltage at power ON/OFF |  |  |  |  |
| Other pins DC current             | -                | -    | ±50  | mA   |                                |  |  |  |  |
|                                   |                  | -    | 8    | dBm  | at 1575.42MHz & 1602MHz        |  |  |  |  |
| RF input power                    | $P_RF$           | -    | 6    | dBm  | at 900MHz                      |  |  |  |  |
|                                   |                  | -    | 8    | dBm  | at 1800MHz                     |  |  |  |  |

## 6.2 Power Supply

#### **Table 6.2 Power Supply Characteristics**

T<sub>A</sub>=25°C, unless otherwise stated

|   |         |                      |      |      | I A=                | 25°C, u | niess otnerwise stated  |
|---|---------|----------------------|------|------|---------------------|---------|---|
| Items                                       |         | Symbol               | Min. | Тур. | Max.                | Unit    | Notes   |
| Supply voltage to VCC                       |         | V <sub>CC</sub>      | 5.2  | 5.5  | 5.8                 | V       |   |
| Backup supply to VBK                        |         | $V_{BK}$             | 1.4  | -    | 3.6                 | V       | at using VBK  |
| Rising slew rate of VCC                     |         | $V_{CC\_SR}$         | -    | -    | 5.8x10 <sup>4</sup> | V/s     | See Figure 6.1  |
| Rising slew rate of VBK                     |         | $V_{BK\_SR}$         | 3.6  | -    | 3.6x10 <sup>4</sup> | V/s     | See Figure 6.1  |
| VCC current consumption                     | GF-8704 | I <sub>CC_RC04</sub> | -    | -    | 1.2                 | Α       | lust ofter starting   |
| (at inrush)                                 | GF-8705 | I <sub>CC_RC05</sub> | -    | -    | 1.2                 | Α       | - Just after starting   |
| VCC current consumption                     | GF-8704 | I <sub>CC_WU04</sub> | -    | -    | 1.0                 | Α       |   |
| (at start up)                               | GF-8705 | I <sub>CC_WU05</sub> | -    | -    | 1.0                 | Α       | Not include antenna   |
| VCC current consumption                     | GF-8704 | I <sub>CC_ST04</sub> | -    | 400  | -                   | mΑ      | <ul> <li>pre-amplifier output</li> <li>current (I<sub>APO</sub>)</li> </ul> |
| (at stable state)                           | GF-8705 | I <sub>CC_ST05</sub> | -    | 400  | -                   | mΑ      | = odironi (igpo)  |
| VBK current consumption at back up          |         | I <sub>BKN</sub>     | -    | 9    | 20                  | μA      | V <sub>CC</sub> =0V   |
| VBK current consumption at normal operation |         | I <sub>BKB</sub>     | -    | 0.4  | 2                   | μΑ      | V <sub>CC</sub> =5.5V   |

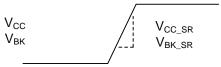


Figure 6.1 Rising Slew Rate



## 6.3 Interface Signal

#### **Table 6.3 Interface Signal**

T<sub>A</sub>=25°C, unless otherwise stated

| Items                            | Symbol          | Min. | Тур. | Max. | Unit | Notes                                 |
|----------------------------------|-----------------|------|------|------|------|---------------------------------------|
| Low-Level input voltage          | V <sub>IL</sub> | -    | -    | 0.8  | V    |                                       |
| High-Level input voltage         | $V_{IH}$        | 2.0  | 3.3  | 5.5  | V    |                                       |
| Low-Level output voltage         | $V_{OL}$        | -    | -    | 0.4  | V    | $I_{OL} = 16mA$                       |
| High-Level output voltage        | $V_{OH}$        | 2.4  | 3.3  | 3.6  | V    | $I_{OH} = -18 \text{mA}$              |
| Digital input pull-up resistor   | $R_{PU}$        | 9.5  | 10   | 10.5 | kΩ   | <ul> <li>Internal resistor</li> </ul> |
| Digital input pull-down resistor | $R_{PD}$        | 9.5  | 10   | 10.5 | kΩ   | - Internal resistor                   |
| Digital input pull-up voltage    | $V_{PU}$        | -    | 3.3  | -    | V    |                                       |

#### 6.4 Reset

#### 6.4.1 Internal Power-on Reset

GNSSDO contains an internal power-on reset circuit which detects VCC voltage and creates POR\_N (power-on reset) signal for initializing module. Table 6.4 shows the threshold voltages to detect and create POR\_N signal.

**Table 6.4 Power-on Reset Voltage** 

T<sub>A</sub>=25°C, unless otherwise stated

| Items                                      | Symbol         | Min. | Тур. | Max. | Unit | Notes |
|--|----------------|------|------|------|------|-------|
| Power On Reset threshold voltage (rising)  | $V_{RTH\_POR}$ | -    | -    | 3.3  | V    |       |
| Power On Reset threshold voltage (falling) | $V_{FTH\_POR}$ | 2.7  | -    | -    | V    |       |

#### 6.4.2 External Reset

GNSSDO is controlled by external reset signal (RST\_N) with the following sequence.

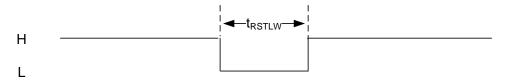


Figure 6.2 Reset Sequence

**Table 6.5 Reset Sequence** 

| Items             | Symbol             | Min. | Max. | Unit | Notes |
|-------------------|--------------------|------|------|------|-------|
| Reset pulse width | T <sub>RSTLW</sub> | 300  | -    | ms   |       |



# 6.5 UART Wake-up Timing after Reset

# 6.5.1 Internal Reset Control

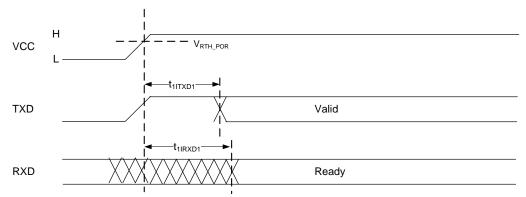


Figure 6.3 UART Wake-up Timing

**Table 6.6 UART Wake-up Timing** 

| Items   | Symbol              | Min. | Max. | Unit | Notes |
|---|---------------------|------|------|------|-------|
| Time delay from VCC reaches V <sub>RTH_POR</sub> to TXD valid | t <sub>1ITXD1</sub> | -    | 6    | S    |       |
| Time delay from VCC reaches V <sub>RTH_POR</sub> to RXD ready | t <sub>1IRXD1</sub> | -    | 6    | S    |       |

#### 6.5.2 External Reset Control

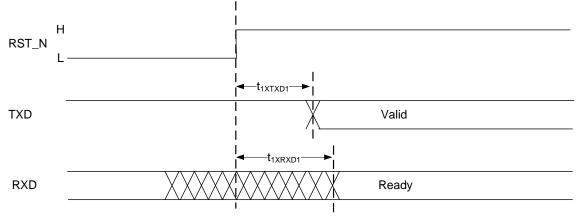


Figure 6.4 UART Wake-up Timing after RST\_N

Table 6.7 UART Wake-up Timing after RST\_N

| Items                                       | Symbol              | Min. | Max. | Unit | Notes |
|---|---------------------|------|------|------|-------|
| Time delay from RST_N set to H to TXD valid | t <sub>1XTXD1</sub> | -    | 6    | S    |       |
| Time delay from RST_N set to H to RXD ready | t <sub>1XRXD1</sub> | -    | 6    | S    |       |



#### 6.5.3 Baud Rate Setting

The baud rate clock is created from 71.5 MHz system clock, hence it has some deviation errors against ideal baud rate clock as shown in Table 6.8.

Table 6.8 Baud Rate vs. Deviation Error (TXD)

|                 | o. 2                |
|-----------------|---------------------|
| Baud rate [bps] | Deviation error [%] |
| 4800            | +0.00               |
| 9600            | +0.11               |
| 19200           | -0.11               |
| 38400           | +0.32               |
| 57600           | -0.54               |
| 115200          | -0.54               |
| 230400          | +2.08               |
| 460800          | -3.02               |
|                 |                     |

The baud rate of serial communication input RXD and the lower and upper limit of tolerance error is shown as Table 6.9.

**Table 6.9 Baud Rate and Tolerance Error (RXD)** 

| Baud rate [bps] | Tolerance error [%] Lower limit | Tolerance error [%] Upper limit |
|-----------------|---------------------------------|---------------------------------|
| 4800            | -4.64                           | 5.26                            |
| 9600            | -4.53                           | 5.38                            |
| 19200           | -4.74                           | 5.15                            |
| 38400           | -4.33                           | 5.60                            |
| 57600           | -5.15                           | 4.70                            |
| 115200          | -5.15                           | 4.70                            |
| 230400          | -2.65                           | 7.45                            |
| 460800          | -7.52                           | 2.08                            |

## 6.6 Antenna

#### 6.6.1 Recommended Antenna

**Table 6.10 Recommended Antenna** 

| Table 6.10 Recommended America |      |         |      |      |                      |
|--------------------------------|------|---------|------|------|----------------------|
| Items                          | Min. | Тур.    | Max. | Unit | Notes                |
| GPS center frequency           | -    | 1575.42 | -    | MHz  | 2.046 MHz bandwidth  |
| GLONASS center frequency       | -    | 1602    | -    | MHz  | 9 MHz bandwidth      |
| Antenna element gain           | 0    | -       | -    | dBi  |                      |
| Pre-amplifier gain             | 15   | -       | 35   | dB   | Including cable loss |
| Pre-amplifier NF               | -    | -       | 3.5  | dB   |                      |
| Impedance                      | -    | 50      | -    | Ω    |                      |
| VSWR                           | -    | -       | 2    | -    |                      |



#### 6.6.2 Antenna Amplifier Power

The power for antenna pre-amplifier is superimposed (biased) from the RF connector. The power supply is ON by default and it is able to be stopped the power supply with the command.

GNSSDO incorporates an antenna current error sensing function. In case of detecting an antenna current error, the alarm (ALM\_N) is output. If the error is an antenna short (an over current), the antenna pre-amplifier power supply is stopped.

**Table 6.11 Antenna Pre-amplifier Power Supply** 

| Items                                | Symbol           | Min. | Тур. | Max. | Unit | Notes                    |
|--------------------------------------|------------------|------|------|------|------|--------------------------|
| Antenna pre-amplifier output voltage | $V_{APO}$        | 4.5  | -    | 5.35 | V    | @ I <sub>APO</sub> =75mA |
| Antenna pre-amplifier output current | I <sub>APO</sub> | -    | -    | 75   | mΑ   |                          |
| Threshold current of antenna open    | I <sub>AOD</sub> | -    | 5    | 10   | mΑ   |                          |
| Threshold current of antenna short   | I <sub>ASD</sub> | 80   | 85   | -    | mΑ   |                          |
| Antenna current upper limitation     | I <sub>AOL</sub> | -    | -    | 200  | mΑ   | Antenna shortage         |

Multiple GNSSDO can be connected for one antenna since the antenna pre-amplifier power output incorporates a preventive function of current backflow. It is not necessary for user to use a DC cut for redundancy.



# 7 VCLK/VCLK\_SIN/GCLK/PPS Signal Specification

## 7.1 GNSS Locked State

Table 7.1 shows the specifications of GNSS locked state.

## **Table 7.1 GNSS Locked State Specifications**

VCC=5.5V

| Symbol                          | Items  |             | Specification | Unit   | Notes                |
|---------------------------------|--|-------------|---------------|--------|----------------------|
|                                 | Frequency                                    |             | 1             | Hz     | _                    |
| PPS                             | Programmable duty ratio by PPS cor           | nmand       | 50(typ)       | %      | _                    |
| FFS                             | Timing accuracy <sup>9)10)</sup>             |             | <±50          | ns     |                      |
|                                 | Timing precision (1 sigma) 9)                |             | <±15          | ns     | Temperature          |
|                                 | Frequency                                    |             | 10            | MHz    | gradient:<br>±20°C/H |
| VOLK                            | Frequency accuracy                           | GF-8704     | <±1E-12       | -      | Open Sky             |
| VCLK (24 hour average) VCLK_SIN | GF-8705                                      | <±1E-12     | -             |        |                      |
| VOLK_OIIV                       | Short term stability                         |             | <1E-10        |        | -                    |
|                                 | (Root Allan variance (τ=1s))                 | GF-8705     | <1E-10        | -      |                      |
|                                 |  |             | <-85          | dBc/Hz |                      |
|                                 |  | 10Hz        | <-120         | dBc/Hz | _                    |
| VCLK SIN                        | Phase noise                                  | 100Hz       | <-130         | dBc/Hz | -                    |
| VOLK_SIN                        |  | 1KHz        | <-140         | dBc/Hz |                      |
|                                 |  | >10KHz      | <-140         | dBc/Hz | T <sub>A</sub> =25°C |
|                                 | Accumulated phase noise                      | 10 to 10KHz | <-95          | dBc    | Open Sky             |
|                                 | Programmable frequency range by GCLK command |             | 0.004 to 40   | MHz    | _                    |
| CCLK                            | GCLK Frequency accuracy (24hour average)     |             | <±5E-11       | -      | _                    |
| GCLK                            | Frequency precision (3 sigma)                |             | <±3E-9        | -      | -                    |
|                                 | Total jitter                                 |             | <±8           | ns     |                      |

#### Notes:

- 9) Valid position mode is the Hold position survey and the Position-hold mode.
- 10) Synchronization source is selectable by TIMEALIGN command. In order to achieve the performance, the user should compensate the cable delay with PPS command correctly.



#### 7.2 Holdover

Table 7.2 shows the specification of Holdover when GNSSDO is not able to get the GNSS time data at static operation, which means that the PPS specification of Holdover is not guaranteed with the following condition:

- Mobile and vehicle application with NAV mode in SURVEY command.
- EPPS as external PPS signal source is available.
- GNSSDO has the influence of mechanical vibration.

The Holdover specification is guaranteed under the temperature condition in Table 7.2. In case the GNSSDO has a big temperature gap between Fine Lock and Holdover state, which means that the temperature of Fine Lock state is constant and the temperature of Holdover state is rapidly changed as example, the Holdover specification is not guaranteed.

**Table 7.2 Holdover Specifications** 

VCC=5.5V

| Symbol           | Items                             |              | Specification | Unit   | Notes  |
|------------------|-----------------------------------|--------------|---------------|--------|--|
|                  | Frequency                         |              | 1             | Hz     | The temperature range <sup>13)</sup> :40°C to 85°C   |
|                  | Programmable duty racommand       | atio by PPS  | 50(typ)       | %      | Ambient temperature                                  |
| PPS              | Timing accuracy <sup>11)12)</sup> | GF-8704      | <±5           | us     | change: 20 °C  |
|                  | (within 24 hours)                 | GF-8705      | <±1.5         | us     | Temperature gradient: _ +/- 5 °C/h                   |
|                  | Timing precision (1 sig           | gma)         | N/A           | -      | Integrated value of                                  |
|                  | Frequency                         |              | 10            | MHz    | temperature variation <sup>14)</sup> :<br>240 H * °C |
|                  | Fragues av a saura av             | GF-8704      | <±1E-9        | -      | Before moving to Holdover                            |
| VCLK<br>VCLK_SIN | VCLK Frequency accuracy VCLK SIN  | GF-8705      | <±1E-9        | -      | state, time to "Fine Lock" should be more than 72    |
| Sł               | Short term stability              | GF-8704      | <1E-10        | -      | hours and the time of power on should be more than 7 |
|                  | (Root Allan variance (τ=1s))      | GF-8705      | <1E-10        | -      | days.  |
|                  |                                   | 1Hz          | <-90          | dBc/Hz |  |
|                  |                                   | 10Hz         | <-120         | dBc/Hz | _  |
|                  | Phase noise                       | 100Hz        | <-130         | dBc/Hz | _  |
| VCLK_SIN         |                                   | 1KHz         | <-140         | dBc/Hz | _  |
|                  |                                   |              | <-140         | dBc/Hz | _  |
|                  | Accumulated phase noise           | 10 to 10KHz  | <-95          | dBc    | T <sub>A</sub> =25°C                                 |
|                  | Programmable freque GCLK command  | ncy range by | 0.004 to 40   | MHz    | -  |
| GCLK             | Frequency accuracy ( average)     | 24hour       | N/A           | -      | -  |
|                  | Total jitter                      |              | <±8           | ns     |  |

#### Notes:

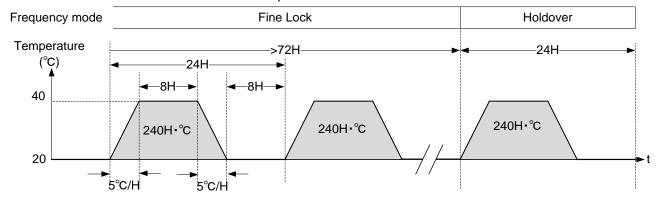
- 11) These are measured at the environment shown in Figure 7.1.
- 12) Valid position mode is the Hold position survey and the Position-hold mode.
- 13) Terminal temperature of the product.
- 14) The time integrated value [H\*°C] of temperature variation. The integrated value per 24 hours based on the temperature of the beginning of Holdover.

**Figure 7.1 Holdover Measurement Environment** 



## 7.3 Time to Fine Lock

Table 7.3 shows the time to Fine Lock from power-on to GNSS lock.



**Table 7.3 Fine Lock Specifications** 

T<sub>A</sub>=25°C, unless otherwise stated Open sky

| VCC OFF time        | VBK state | State before VCC OFF   | Adjusting time                          |
|---------------------|-----------|--|---|
| 5 seconds and more  | -         |  | va ODC "E main                          |
|                     | N/A       | - •  | ·vs GPS···<5 min<br>— ·vs UTC···<15 min |
| less than 5 seconds |           | Other than the below state                                       | — ·vs o ro…< 13 iiiiii                  |
| less than 5 seconds | Available | •UTC(USNO) or UTC(SU) alignment <sup>15)</sup>                   | ∙vs GPS…<5 min                          |
|                     |           | <ul><li>pps status: UTC(USNO) or UTC(SU)<sup>16)</sup></li></ul> | ∙vs UTC…<5 min                          |

#### Notes

- 15) This is selectable by TIMEALIGN command. The default is UTC(USNO) alignment.
- 16) See field 7 in CRW(TPS1) sentence about the pps status.



# 7.4 Phase Relation between PPS, VCLK and VCLK\_SIN

Figure 7.2 shows the phase relation between PPS and VCLK. This relation is coherent.

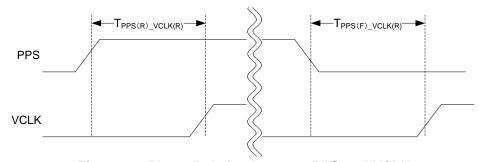


Figure 7.2 Phase Relation between PPS and VCLK

Table 7.4 Phase Relation between PPS and VCLK

| Symbol                      | Description  | Condition                       | Min. | Max. | Unit |
|-----------------------------|--|---------------------------------|------|------|------|
| T <sub>PPS(R)_VCLK(R)</sub> | VCLK rising delay time after voltage of PPS is valid   | Valid frequency mode:           | 35   | 55   | ns   |
| T <sub>PPS(F)_VCLK(R)</sub> | VCLK rising delay time after voltage of PPS is invalid | Pull-In, Coarse Lock, Fine Lock | 35   | 55   | ns   |

Figure 7.3 shows the phase relation between PPS and VCLK\_SIN. This relation is coherent.

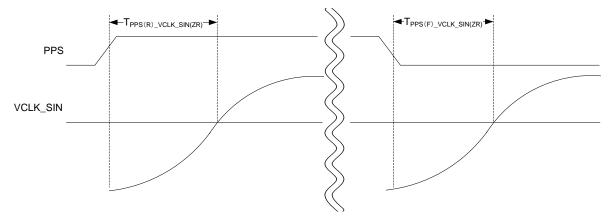


Figure 7.3 Phase Relation between PPS and VCLK\_SIN

Table 7.5 Phase Relation between PPS and VCLK SIN

|                                  | 14515 116 1 11455 11514115  |                                 |      |      |      |
|----------------------------------|---|---------------------------------|------|------|------|
| Symbol                           | Description   | Condition                       | Min. | Max. | Unit |
| T <sub>PPS(R)_VCLK_SIN(ZR)</sub> | VCLK_SIN zero cross rising delay time after voltage of PPS is valid   | Valid frequency mode:           | 15   | 35   | ns   |
| T <sub>PPS(F)_VCLK_SIN(ZR)</sub> | VCLK_SIN zero cross rising delay time after voltage of PPS is invalid | Pull-In, Coarse Lock, Fine Lock | 15   | 35   | ns   |



# 8 Interface Signal Specification

# 8.1 Alarm Signal (ALM\_N)

It is able to confirm the alarm signal (ALM\_N) status by "alarm" field in CRZ (TP4) sentence. Table 8.1 shows the protocol specifications of alarm signal.

**Table 8.1 Alarm Signal Specifications** 

| CRZ(TPS4) "alarm" field | ALM_N pin | Description |
|-------------------------|-----------|-------------|
| 00                      | Logic H   | Normal      |
| Other than 00           | Logic L   | Abnormal    |

# 8.2 Lock Signal (LOCK)

It is able to confirm the lock signal (Lock) status by "frequency mode" field in CRZ (TP4) sentence and to set the lock pin output condition by "Lock post set" field in MODESET command. Table 8.2 shows the protocol specifications of lock signal.

**Table 8.2 Lock Signal Specifications** 

| MODESET "Lock port set" field | CRZ(TPS4) "frequency mode" field | LOCK pin |
|-------------------------------|----------------------------------|----------|
|                               | 2, 3, 4                          | Logic H  |
|                               | other than above values          | Logic L  |
| 1 (default)                   | 2, 3                             | Logic H  |
| r (derauit)                   | other than above values          | Logic L  |
| 2                             | 3                                | Logic H  |
| <u>Z</u>                      | other than above value           | Logic L  |
| 2                             | 3,4                              | Logic H  |
| 3                             | other than above values          | Logic L  |

# 8.3 PPS Input Signal for External Synchronization (EPPS)

When 1PPS is input to the EPPS pin and the command is set up, the VCLK and the PPS will be synchronized with the pulse. The synchronous target is the rising edge of the pulse to be input to the EPPS. Refer to the "EXTSYNC" in the protocol specification to set the external synchronized function.

## 8.4 Backup Power Supply (VBK)

When using the backup power supply, the information obtained from the navigation message of each satellite, the positioning result and the input value of the command set by the user are saved into the backup RAM (BBRAM) in the GNSSDO at the main power-off. With this backup function, when the GNSSDO returns from the main power-off, the TTFF and the time to GNSS Lock State will be reduced. However, the almanac and ephemeris data should be received before the main power shut down. Refer to the protocol specifications for the data to be saved into BBRAM.

#### 9 State Transition

It is able to confirm the state transition by "frequency mode" field in CRZ (TPS4) sentence. See the protocol specifications about this sentence.



# 10 Environmental Specifications

**Table 10.1 Environmental Specifications** 

| Items                 | Specification | Unit | Notes                                  |
|-----------------------|---------------|------|--|
| Operating temperature | -40 to +85    | °C   |  |
| Storage temperature   | -40 to +85    | °C   |  |
| Operation humidity    | 85 (MAX)      | %R.H | T <sub>A</sub> = 60°C, No condensation |

# 11 RoHS

This product is RoHS compliant.

# 12 Flame Retardancy Rank

UL94V-1 compliance.

# **13 FIT**

GF-8704 ---3210FIT GF-8705 --- 3210FIT

# Calculation requirements

- Telcordia 332 issue3
- Parts count method
- Environmental factor: GF
- Operating temperature: 50°C
- Quality level: level 0
- Using the failure rate from manufacturer: Yes

# 14 Reliability Test

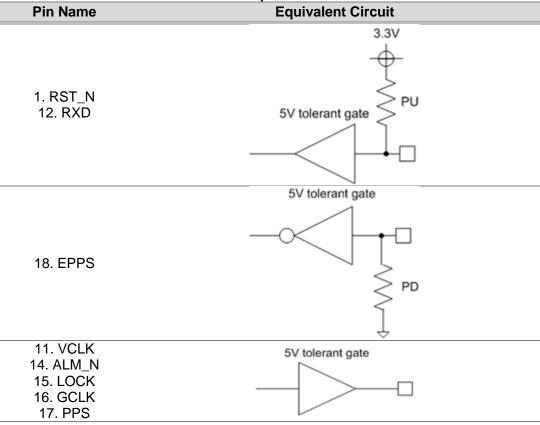
| # | Test Item                                   | Conditions  |
|---|---|---|
| 1 | High temperature high humidity bias life    | 1000 hours, T <sub>A</sub> = 85°C, RH =85%  |
| 2 | High temperature high humidity storage life | 1000 hours, T <sub>A</sub> = 85°C, RH =85%  |
| 3 | Low temperature operating life              | 500 hours, $T_A = -40^{\circ}C$   |
| 4 | Low temperature storage life                | 500 hours, $T_A = -40^{\circ}C$   |
| 5 | Drop Test                                   | With packing, 50cm natural drop   |
| 6 | Vibration Test                              | The each three direction (x,y,z), 10 to 55Hz 4.7G (46m/s <sup>2</sup> ) 30 minutes (Not operating). |
| 7 | ESD Test                                    | JIS C 61000-4-2 Contact   |



# 15 Equivalent Circuit

Table 15.1 shows the equivalent circuits of digital signal port.

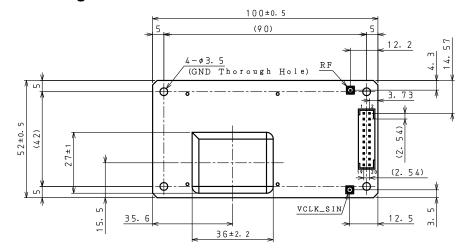
**Table 15.1 Equivalent Circuit** 

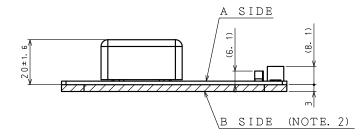


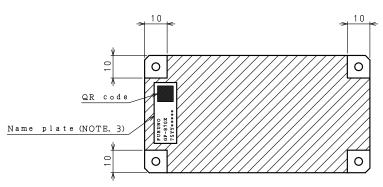


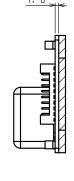
# 16 Mechanical Specifications

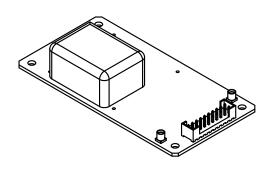
# 16.1 Outline Drawing











GF-8704/8705 External view

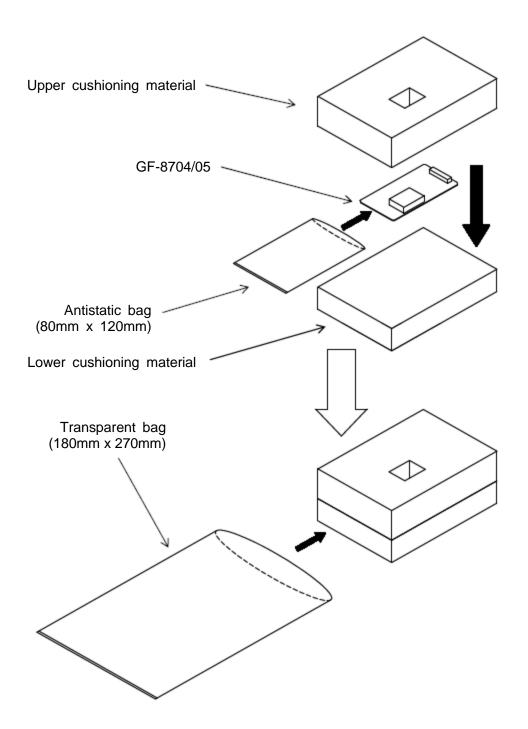
#### Notes:

- 1. Tolerance dimension is ±0.2mm unless otherwise stated.
- 2. Keep the hatching area for preventing the component interference between the GF-8704/05 and the user platform.
- 3. Products label specifications.
  - X: Products number code
  - 4: GF-8704 5: GF-8705
  - YY: Products unique code
  - 11: GF-8704 12: GF-8705
  - \*\*\*\*\*: Serial number
- 4. Interface connector product number: PS-20PLB-D4T1-FL1E (JAE)
- 5. RF and VCLK\_SIN connector product number: MMCX1-4024 (CONNEKT)



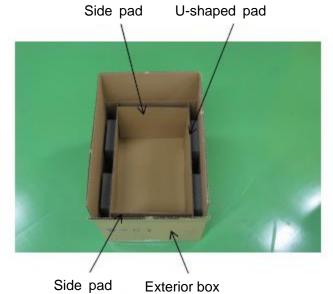
# 17 Packaging

[Interior packaging]



[Exterior packaging]

Prepare the exterior box.



Put the products in the exterior box.



Put the upper pad on the products.



Upper pad



[Exterior packaging]

Close the cover with sealing tape, and attach the product label.



# 18 Warranty

The warranty term of this product is one year after the delivery.



# 19 Special Attention

#### 19.1 Precautions for Use

- (1) A GNSS receiver receives very weak signals sent by the GNSS satellites. Using an antenna with band limitations or insufficient preamplifier could be disrupted by transmitted power from TV broadcast, mobile phone, MCA or similar transmitting devices causing unstable reception status. Therefore use an antenna equipped with a SAW filter on the preamplifier front stage to ensure stable GNSS reception.
- (2) It is recommended to install the antenna vertically outdoors in a location where there are no obstacles within its elevation angle of 5°. GNSS signals may reflect from buildings, trees or ground surfaces and reach a GNSS antenna via the reflected (delayed) route. Therefore install a GNSS antenna in environment where there are no reflected waves. Therefore avoid mounting near buildings or other obstructions.
- (3) Radio waves transmitted by handheld transmitters or transmitting antennas may adversely affect GNSS signal reception by superimposing interfering signal onto the GNSS antenna. When locating the GNSS antenna ensure is not located in the direction of offending transmitting antenna beam.
- (4) RF noise may interfere via the GNSS antenna and adversely affect the GNSS signal reception. Avoid using GNSS devices near equipment emitting RF noise.
- (5) Considering the information above check tracking status of the GNSS satellites and positioning information. Possibly for an extended period of time (8 to 24 hours) to ensure no multipath signal or other reception issues exist. Also check the overall environment where the GNSS antenna will be located.
- (6) Ensure a stable power supply connection.
- (7) Install in a stable temperature, wind free environment for the GNSS unit to eliminate errors caused by temperature deviations.
- (8) Improper heat dissipation may increase the device temperature beyond the upper limit specifications resulting in performance degradation or failure. Install the device allowing sufficient space around the device for heat dissipation considerations.
- (9) Lightning may strike the GNSS antenna. This product does not have a lightning protector so we recommend inserting an appropriate arrester between the GNSS antenna and this product.

#### **19.2 Electronic Component**

Components in the GNSSDO such as chip resistors, capacitors, memories and TCXO are planned to be purchased from multiple manufacturers/vendors according to FURUNO's procurement policy. So it is possible that multiple components from multiple manufacturers/vendors could be used even in the same production lot.

#### 19.3 Precautions at Mounting

- (1) This product contains semi-conductor inside. While handling this, be careful about the static electrical charge (less than 100V). To avoid it, use conductive mat, ground wristband, anti-static shoes, ionizer, etc. as may be necessary.
- (2) Try to avoid mechanical shock and vibration. Try not to drop this product.



## 19.4 Precautions on Industrial Property Rights

- (1) Since this document includes our copyrights and know-how, do not use it for any purpose other than the intended use of this product. Do not make any copies of this document and disclose it to any third parties without our prior consent.
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