FDMS4D0N12C

Power MOSFET

120 V, 4.0 mΩ, 118 A, Single N−Channel, PQFN56

ON Semiconductor®

www.onsemi.com

Features

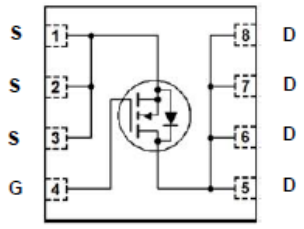
- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These are Pb−free, Halogen Free / BFR Free and are RoHS Compliant

Typical Applications

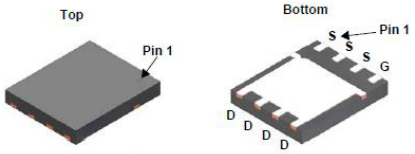
- Synchronous Rectification
- AC−DC and DC−DC Power Supplies
- AC−DC Adapters (USB PD) SR
- Load Switch

$V_{(BR)DDS}$	I_D MAX	$R_{DS(on)}$ MAX
120 V	67 A	4.0 mΩ @ 10 V
	33 A	8.0 mΩ @ 6 V

ELECTRICAL CONNECTION



N-Channel MOSFET



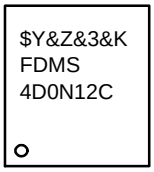
Power 56
(PQFN8 5x6)
CASE 483AF

MAXIMUM RATINGS (T_A = 25°C, Unless otherwise specified)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	120	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Note 7)	Steady State	T_C = 25°C	I_D	114	A
Power Dissipation $R_{\theta JC}$ (Note 2)			P_D	106	W
Continuous Drain Current $R_{\theta JA}$ (Note 6, 7)	Steady State	T_A = 25°C	I_D	18.5	A
Power Dissipation $R_{\theta JA}$ (Note 6, 7)			P_D	2.7	W
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	628	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to +150	°C
Source Current (Body Diode)			I_S	114	A
Single Pulse Drain−to−Source Avalanche Energy (I_{AV} = 66.7 A, L = 0.1 mH)			E_{AS}	222	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)			T_L	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDMS4D0N12C	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Device	Package	Shipping†
FDMS4D0N12C	PQFN8 (Power 56) (Pb−Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction – to – Case – Steady State (Note 7)	$R_{\theta JC}$	1.18	°C/W
Junction – to – Ambient – Steady State (Note 7)	$R_{\theta JA}$	45	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Symbol Test Conditions		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain – to – Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		120			V
Drain – to – Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}$/ T_J	I_D = 250 μA, ref to 25°C			49		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 96 V	T_J = 25°C			1	μA
			T_J = 125°C			100	μA
Gate – to – Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V				±100	nA
ON CHARACTERISTICS (Note 8)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 370 A		2.0		4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}$ /T_J	I_D = 250 μA, ref to 25°C			−8.5		mV/°C
Drain – to – Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 67 A			3.3	4.0	mΩ
		V_{GS} = 6 V, I_D = 33 A			4.7	8.0	
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 67 A			144		S
Gate−Resistance	R_G	T_A = 25°C			0.9	1.8	Ω
CHARGES & CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 60 V			4565	6460	pF
Output Capacitance	C_{OSS}				2045	3060	
Reverse Transfer Capacitance	C_{RSS}				17	24	
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 6 V, V_{DS} = 60 V, I_D = 67 A			36	51	nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 60 V, I_D = 67 A			58	82	
Gate−to−Source Charge	Q_{GS}				21		
Gate−to−Drain Charge	Q_{GD}				9		
Plateau Voltage	V_{GP}				5		V
Output Charge	Q_{OSS}	V_{DD} = 60 V, V_{GS} = 0 V			207		nC

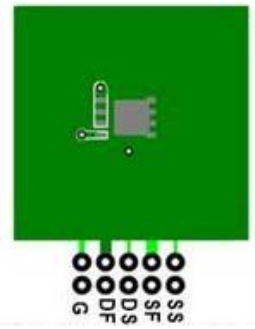
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Symbol Test Conditions		Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS (Note 8)							
Turn – On Delay Time	$td_{(ON)}$	V_{GS} = 10 V, V_{DS} = 60 V, I_D = 67 A, R_G = 6 Ω			25	41	ns
Rise Time	t_r				8	16	
Turn – Off Delay Time	$t_{D(OFF)}$				45	72	
Fall Time	t_f				12	22	
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 67 A	T_J = 25°C		0.86	1.3	V
			T_J = 125°C		0.7	1.2	
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 300 A/μs, I_S = 33 A			53	84	ns
Reverse Recovery Charge	Q_{RR}				175	280	nC
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 1000 A/μs, I_S = 33 A			36	57	ns
Reverse Recovery Charge	Q_{RR}				360	575	nC

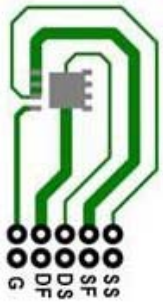
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR−4 material. $R_{\theta CA}$ is determined by the user's board design.



a) 45°C/W when mounted on a 1 in^2 pad of 2 oz copper.



b) 115°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. E_{AS} of 222 mJ is based on starting T_J = 25°C; L = 0.1 mH, I_{AS} = 66.7 A, V_{DD} = 100 V, V_{GS} = 12 V, 100% tested at L = 0.1 mH, I_{AS} = 66.7 A.
4. Pulsed I_D please refer to Fig. 11 SOA graph for more details.
5. Computed continuous current limited to max Junction Temperature only, actual continuous current will be limited by thermal & electro−mechanical application board design.
6. Surface−mounted on FR4 board using 1 in2 pad size, 2 oz Cu pad.
7. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
8. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

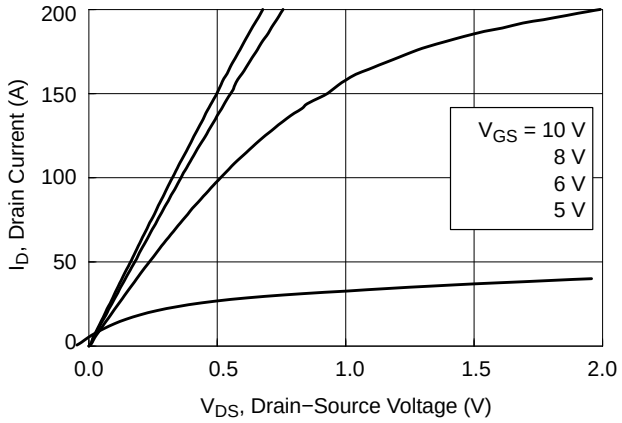


Figure 1. On-Region Characteristics

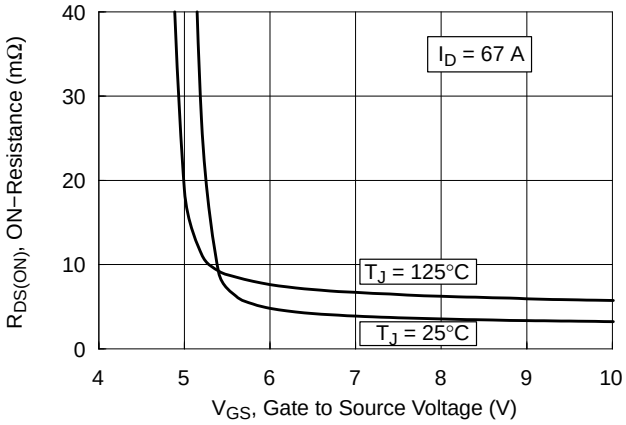


Figure 2. Transfer Characteristics

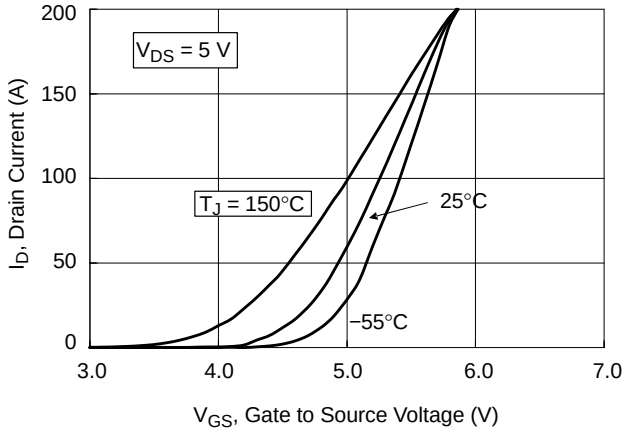


Figure 3. On−Resistance vs. Gate−to−Source Voltage

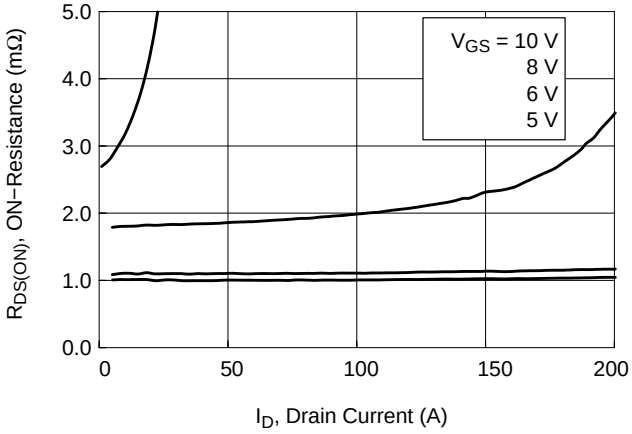


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

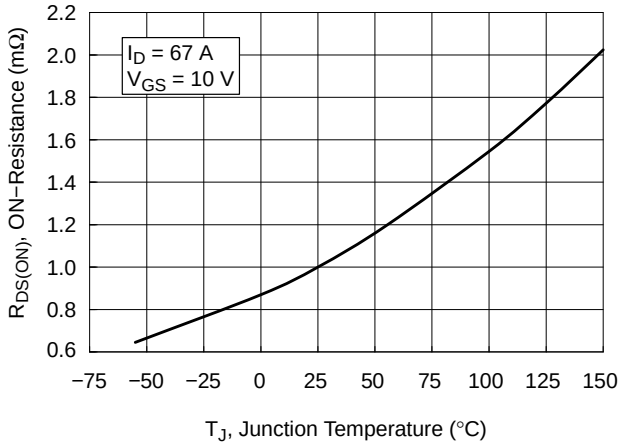


Figure 5. On−Resistance Variation with Temperature

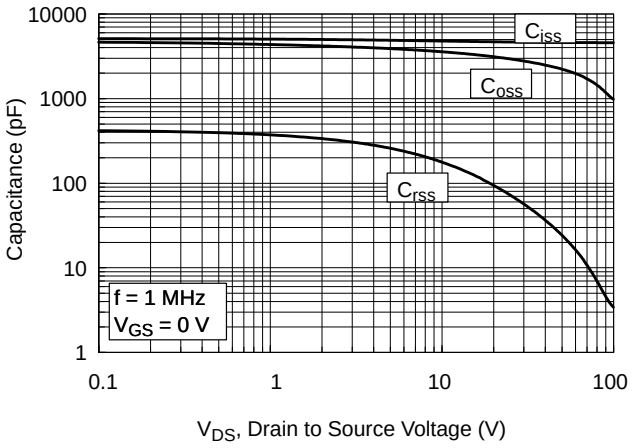


Figure 6. Capacitance Variation

TYPICAL CHARACTERISTICS (continued)

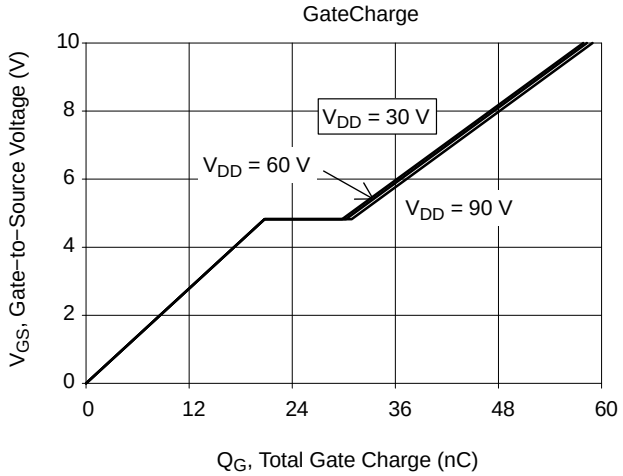


Figure 7. Gate−to−Source Voltage vs. Total Charge

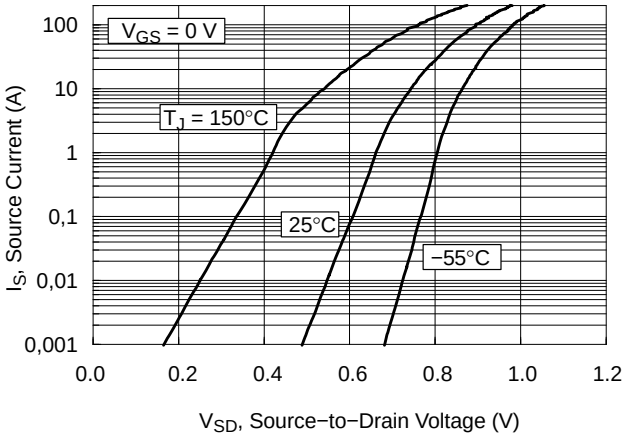


Figure 8. Diode Forward Voltage vs. Current

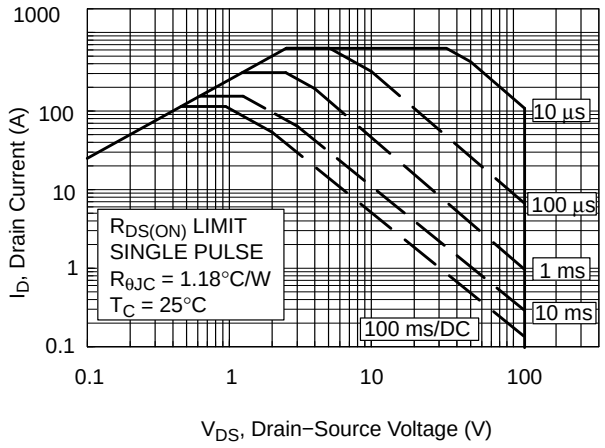


Figure 9. Safe Operating Area

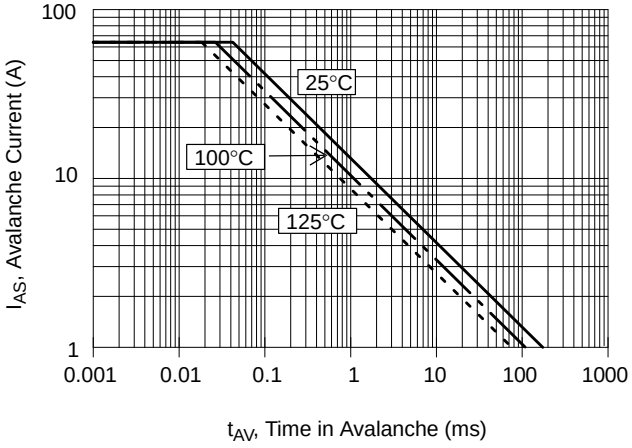
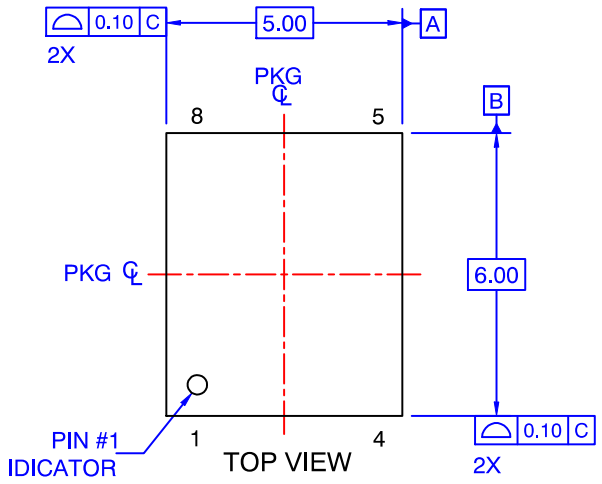
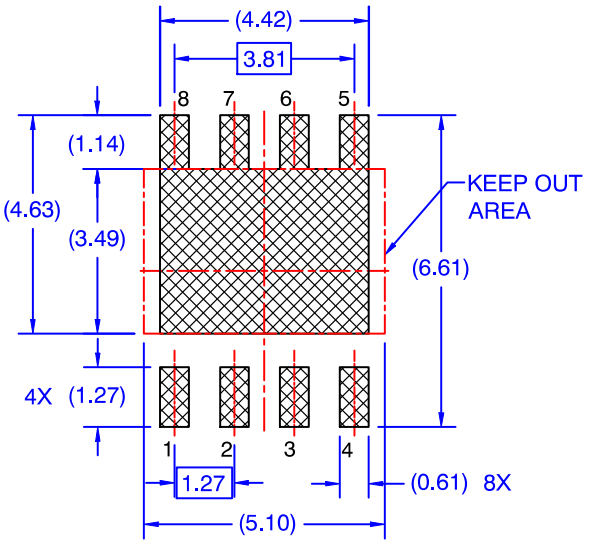


Figure 10. I_{PEAK} vs. Time in Avalanche

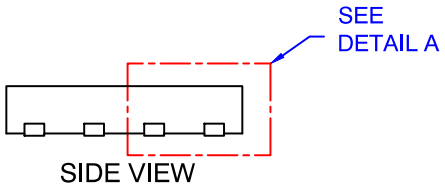
PACKAGE DIMENSIONS

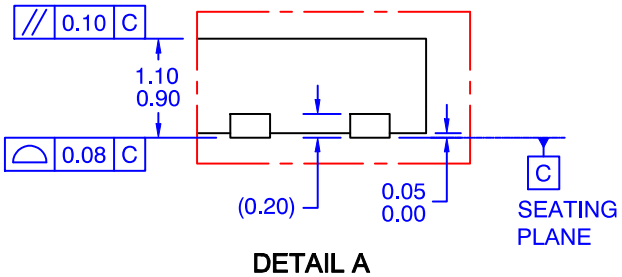
PQFN8 5X6, 1.27P
CASE 483AF
ISSUE O



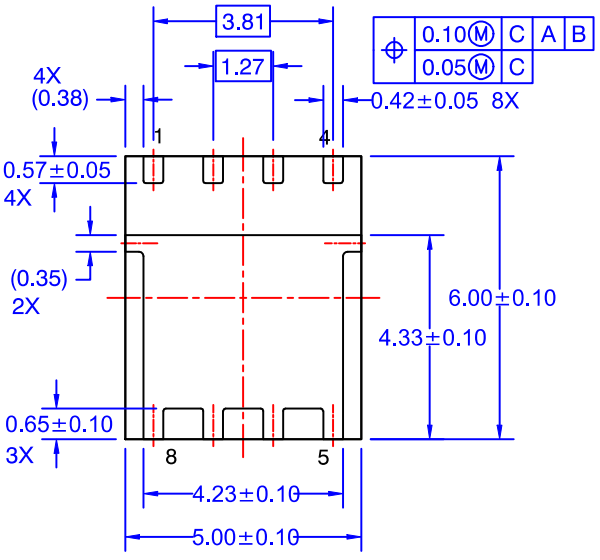


LAND PATTERN
RECOMMENDATION





DETAIL A
SCALE: 2:1



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED
A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA,
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
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