FR60 MB91460B Series, 32-bit Microcontroller Datasheet

MB91460B series is a line of general-purpose 32-bit RISC microcontrollers designed for embedded control applications which require high-speed real-time processing, such as consumer devices and on-board vehicle systems. This series uses the FR60 CPU, which is compatible with the FR family of CPUs.

This series contains the LIN-USART and CAN controllers.

Note: MB91F466BA, MB91F464BB - These devices are under development.

Features

FR60 CPU core

- 32-bit RISC, load/store architecture, five-stage pipeline

- 16-bit fixed-length instructions (basic instructions)

- Instruction execution speed: 1 instruction per cycle

- Instructions including memory-to-memory transfer, bit manipulation, and barrel shift instructions: Instructions suitable for embedded applications

- Function entry/exit instructions and register data multi-load store instructions: Instructions supporting C language

- Register interlock function: Facilitating assembly-language coding

- Built-in multiplier with instruction-level support
  Signed 32-bit multiplication: 5 cycles
  Signed 16-bit multiplication: 3 cycles

- Interrupts (save PC/PS): 6 cycles (16 priority levels)

- Harvard architecture enabling program access and data access to be performed simultaneously

- Instructions compatible with the FR family

Internal Peripheral Resources

- General-purpose ports: Maximum 108 ports

- DMAC (DMA Controller)

Maximum of 5 channels able to operate simultaneously

2 transfer sources (internal peripheral/software)
Activation source can be selected using software

Addressing mode specifies full 32-bit addresses (increment/decrement/fixed)

Transfer mode (demand transfer/burst transfer/step transfer/block transfer)
Transfer data size selectable from 8/16/32-bit
Multi-byte transfer enabled (by software)
DMAC descriptor in I/O areas (200_H to 240_H, 1000_H to 1024_H)

A/D converter (successive approximation type)
10-bit resolution: maximum 32 channels
Conversion time: minimum 1 μs

- External interrupt inputs: maximum 16 channels
  6 channels shared with CAN RX or I^2C pins

- Bit search module (for REALOS)

Function to search the first bit position of ''1'', ''0'', ''changed'' from the MSB (most significant bit) within one word

- LIN-USART (full duplex double buffer): 4 or 7 channels, depending on pin multiplexing

Clock synchronous/asynchronous selectable

Sync-break detection

Internal dedicated baud rate generator

- I^2C bus interface (supports 400 kbps): 2 channels

Master/slave transmission and reception

Arbitration function, clock synchronization function

- CAN controller (C-CAN): 3 or 6 channels (depending on the device)

Maximum transfer speed: 1 Mbps

32 transmission/reception message buffers

- Sound generator: 1 channel
  Tone frequency : PWM frequency divide-by-two (reload value + 1)

- Alarm comparator: 1 channel
  Monitor external voltage
  Generate an interrupt in case of voltage lower/higher than the defined thresholds (reference voltage)

- 16-bit PPG timer: maximum 16 channels

- 16-bit reload timer: 8 channels

- 16-bit free-run timer: 8 channels (1 channel each for ICU and OCU)

- Input capture: maximum 8 channels (operates in conjunction with the free-run timer)

- Output compare: maximum 8 channels (operates in conjunction with the free-run timer)

- Up/Down counter: 2 channels (2*8-bit or 1*16-bit)

- Watchdog timer

- Real-time clock

- Low-power consumption modes: Sleep/stop mode function

- Low voltage detection circuit

- Clock supervisor
  Monitors the sub-clock (32 kHz) and the main clock (4 MHz) ,

and switches to a recovery clock (CR oscillator, etc.) when the oscillations stop.

■ Clock modulator

■ Clock monitor

■ Sub-clock calibration
Corrects the real-time clock timer when operating with the 32 kHz or CR oscillator

Package and Technology

■ Package: QFP-144

■ CMOS 180 nm technology

■ Main oscillator stabilization timer
Generates an interrupt in sub-clock mode after the stabilization wait time has elapsed on the 23-bit stabilization wait time counter

■ Sub-oscillator stabilization timer
Generates an interrupt in main clock mode after the stabilization wait time has elapsed on the 15-bit stabilization wait time counter

■ Power supply range 3 V to 5 V (1.8 V internal logic provided by a step-down voltage converter)

■ Operating temperature range: between $-40°C$ and $+125°C$

Contents

1. Product Lineup

Feature	MB91V460	MB91F465BB/464BB	MB91F467BA/466BA
Max. core frequency (CLKB)	80 MHz	100 MHz	96 MHz
Max. resource frequency (CLKP)	40 MHz	50 MHz	48 MHz
Max. external bus frequency (CLKT)	40 MHz	50 MHz	48 MHz
Max. CAN frequency (CLKCAN)	20 MHz	50 MHz	48 MHz
Technology	0.35μm	0.18μm	0.18μm
Watchdog	yes	yes	yes
Watchdog (RC osc. based)	yes (disengageable)	yes	yes
Bit Search	yes	yes	yes
Reset input (INITX)	yes	yes	yes
Hardware standby input (HSTX)	yes	no	no
Clock Modulator	yes	yes	yes
Clock Monitor	yes	yes	yes
Low Power Mode	yes	yes	yes
DMA	5 ch	5 ch	5 ch
MMU/MPU	MPU (16 ch)[1]	MPU (8 ch)[1]	MPU (8 ch)[1]
Flash memory	Emulation SRAM 32bit read data	MB91F465BB: 544 KByte MB91F464BB: 416 KByte	MB91F467BA: 1088 KByte MB91F466BA: 832 KByte
Satellite Flash memory	-	-	-
Flash Protection	-	yes	yes
D-RAM	64 KByte	24 KByte	24 KByte
ID-RAM	64 KByte	16 KByte	16 KByte
Flash-Cache (Instruction cache)	16 KByte	8 KByte	8 KByte
Boot-ROM / BI-ROM	4 KByte fixed	4 KByte	4 KByte
RTC	1 ch	1 ch	1 ch
Free Running Timer	8 ch	8 ch[2]	8 ch[2]
ICU	8 ch	MD_3=0: 8 ch MD_3=1: 4 ch[3]	MD_3=0: 8 ch MD_3=1: 4 ch[3]
OCU	8 ch	MD_3=0: 8 ch MD_3=1: 4 ch[4]	MD_3=0: 8 ch MD_3=1: 4 ch[4]
Reload Timer	8 ch	8 ch[5]	8 ch[5]
PPG 16-bit	16 ch	MD_3=0: 16 ch MD_3=1: 8 ch[6]	MD_3=0: 16 ch MD_3=1: 8 ch[6]
PFM 16-bit	1 ch	-	-
Sound Generator	1 ch	1 ch	1 ch
Up/Down Counter (8/16 bit)	4 ch (8-bit) / 2 ch (16-bit)	MD_3=0: 2 ch (8-bit) / 1 ch (16bit) MD_3=1: NA[7]	MD_3=0: 2 ch (8-bit) / 1 ch (16bit) MD_3=1: NA[7]
C_CAN	6 ch (128msg)	3 ch (32msg)	6 ch (32msg)

Feature	MB91V460	MB91F465BB/464BB	MB91F467BA/466BA
LIN-USART	4 ch + 4 ch FIFO + 8 ch	MD_3=0: 3 ch + 4 ch FIFO[8] MD_3=1: 4 ch FIFO	MD_3=0: 3 ch + 4 ch FIFO[8] MD_3=1: 4 ch FIFO
I^2C (400K)	4 ch	2 ch	2 ch
FR external bus	yes (32bit addr, 32bit data)	MD_3=0: no MD_3=1: yes (22bit addr, 16bit data)	MD_3=0: no MD_3=1: yes (22bit addr, 16bit data)
External Interrupts	16 ch	MD_3=0: 16 ch MD_3=1: 12 ch[9]	MD_3=0: 16 ch MD_3=1: 12 ch[9]
NMI Interrupts	1 ch	1 ch	1 ch
SMC	6 ch	-	-
LCD controller (40x4)	1 ch	-	-
ADC (10-bit)	32 ch	MD_3=0: 32 ch MD_3=1: 16 ch	MD_3=0: 32 ch MD_3=1: 16 ch
Alarm Comparator	2 ch	1 ch	1 ch
Supply Supervisor (low voltage detection)	yes	yes	yes
Clock Supervisor	yes	yes	yes
Main clock oscillator	4 MHz	4 MHz	4 MHz
Sub clock oscillator	32kHz	32kHz	32kHz
RC oscillator	100kHz	100kHz / 2MHz	100kHz / 2MHz
PLL	x 20	x 25	x 25
DSU4	yes	no	no
EDSU	yes (32 BP)[1]	yes (16 BP)[1]	yes (16 BP)[1]
Supply voltage	3V/5V	3V/5V	3V/5V
Regulator	yes	yes	yes
Power consumption	n.a.	< 1.3 W	< 1.3 W
Temperature Range (Ta)	0..70 C	-40..125 C	-40..125 C
Package	BGA-660	QFP-144	QFP-144
Power on to PLL run	< 20 ms	< 20 ms	< 20 ms
Flash Download Time	n.a.	< 5 sec. typical	< 6 sec. typical

1. MPU channels use EDSU breakpoint registers (shared operation between MPU and EDSU).

2. Free Running Timer: MD3=0 : CH 1 and 0 cannot select external clock (bit7 of TCCS1,0)
        MD3=1: CH 3, 2, 1, and 0 cannot select external clock (bit7 of TCCS3,2,1,0)

3. ICU: MD3=1: Do not set PFR = 1 & EPFR = 1 (for LIN Synch Field detect).

4. OCU: MD3=1: You cannot use external out-port (but, OCU-function is active.)

5. Reload Timer: MD3=1: CH 7, 6, 5, and 4 cannot select external event

6. PPG: MD3=1: You can use CH15 to 8 of PPG. CH15 to12 cannot select external trigger.

7. Up/Down Counter: MD3=1: You can use Timer-mode only.

8. LIN-USART CH 0 (shared with external bus) can be used for asynchronous mode only.

9. External Interrupts: INT7 to INT4(shared with external bus) can be used for MD3=0 mode only. INT0 (shared with external bus) can be used for MD3=0 mode only.

2. Pin Assignment

2.1 MB91F467BA/466BA with MD_3=1

(TOP VIEW)

LQFP-144

Top side pins (144 down to 109):

VDD35, P07_5/A5, P07_4/A4, P07_3/A3, P07_2/A2, P07_1/A1, P07_0/A0, P15_3/OCU3/TOT3, P15_2/OCU2/TOT2, P15_1/OCU1/TOT1, P15_0/OCU0/TOT0, P14_3/ICU3/TIN3/TTG3/11, P14_2/ICU2/TIN2/TTG2/10, P14_1/ICU1/TIN1/TTG1/9, P14_0/ICU0/TIN0/TTG0/8, P24_3/INT3, P24_2/INT2, VSS5, VDD5, P28_7/AN15, P28_6/AN14, P28_5/AN13, P28_4/AN12, P28_3/AN11, P28_2/AN10, P28_1/AN9, P28_0/AN8, P29_7/AN7, P29_6/AN6, P29_5/AN5, P29_4/AN4, P29_3/AN3, P29_2/AN2, P29_1/AN1, P29_0/AN0, VSS5

(pins 144,143,142,141,140,139,138,137,136,135,134,133,132,131,130,129,128,127,126,125,124,123,122,121,120,119,118,117,116,115,114,113,112,111,110,109)

Left side pins (1 to 36):

Pin	Name
1	VSS5
2	P07_6/A6
3	P07_7/A7
4	P06_0/A8
5	P06_1/A9
6	P06_2/A10
7	P06_3/A11
8	P06_4/A12
9	P06_5/A13
10	P06_6/A14
11	P06_7/A15
12	P05_0/A16
13	P05_1/A17
14	P05_2/A18
15	P05_3/A19
16	P05_4/A20
17	P05_5/A21
18	VDD35
19	VSS5
20	P01_0/D16
21	P01_1/D17
22	P01_2/D18
23	P01_3/D19
24	P01_4/D20
25	P01_5/D21
26	P01_6/D22
27	P01_7/D23
28	P00_0/D24
29	P00_1/D25
30	P00_2/D26
31	P00_3/D27
32	P00_4/D28
33	P00_5/D29
34	P00_6/D30
35	P00_7/D31
36	VDD35

Right side pins (108 to 73):

Pin	Name
108	VDD5
107	AVCC5
106	AVRH5
105	AVSS5
104	ALARM_0
103	P18_6/SCK7/CK7
102	P18_5/SOT7
101	P18_4/SIN7
100	P18_2/SCK6/CK6
99	P18_1/SOT6
98	P18_0/SIN6
97	P19_6/SCK5/CK5
96	P19_5/SOT5
95	P19_4/SIN5
94	P19_2/SCK4/CK4
93	P19_1/SOT4
92	P19_0/SIN4
91	VSS5
90	VDD5
89	VDD5R
88	VDD5R
87	VCC18C
86	VSS5
85	NMIX
84	INITX
83	X1A
82	X0A
81	VSS5
80	X0
79	X1
78	MD_3
77	MONCLK
76	MD_2
75	MD_1
74	MD_0
73	VSS5

Bottom side pins (37 to 72):

VSS5, P10_0/SYSCLK, P09_0/CSX0, P09_1/CSX1, P08_0/WRX0, P08_4/RDX, P08_7/RDY, WRX1, P24_1/INT1, P23_0/RX0/INT8, P23_1/TX0, P23_2/RX1/INT9, P23_3/TX1, P23_4/RX2/INT10, P23_5/TX2, P23_6/RX3/INT11, P23_7/TX3, VSS5, VDD5, P22_0/RX4/INT12, P22_1/TX4, P22_2/RX5/INT13, P22_3/TX5, P22_4/SDA0/INT14, P22_5/SCL0, P22_6/SDA1/INT15, P22_7/SCL1, P16_0/PPG8, P16_1/PPG9, P16_2/PPG10, P16_3/PPG11, P16_4/PPG12/SGA, P16_5/PPG13/SGO, P16_6/PPG14, P16_7/PPG15/ATGX, VDD5

(pins 37,38,39,40,41,42,43,44,45,46,47,48,49,50,51,52,53,54,55,56,57,58,59,60,61,62,63,64,65,66,67,68,69,70,71,72)

2.2　MB91F467BA/466BA with MD_3=0

(TOP VIEW)

LQFP-144

Pin	Signal		Pin	Signal
1	VSS5		108	VDD5
2	P27_6/AN22		107	AVCC5
3	P27_7/AN23		106	AVRH5
4	P26_0/AN24		105	AVSS5
5	P26_1/AN25		104	ALARM_0
6	P26_2/AN26		103	P18_6/SCK7/CK7
7	P26_3/AN27		102	P18_5/SOT7
8	P26_4/AN28		101	P18_4/SIN7
9	P26_5/AN29		100	P18_2/SCK6/CK6
10	P26_6/AN30		99	P18_1/SOT6
11	P26_7/AN31		98	P18_0/SIN6
12	P24_4/INT4		97	P19_6/SCK5/CK5
13	P24_5/INT5		96	P19_5/SOT5
14	P24_6/INT6		95	P19_4/SIN5
15	P24_7/INT7		94	P19_2/SCK4/CK4
16	P21_0/SIN0		93	P19_1/SOT4
17	P21_1/SOT0		92	P19_0/SIN4
18	VDD35		91	VSS5
19	VSS5		90	VDD5
20	P14_4/ICU4/TIN4/TTG12/4		89	VDD5R
21	P14_5/ICU5/TIN5/TTG13/5		88	VDD5R
22	P14_6/ICU6/TIN6/TTG14/6		87	VCC18C
23	P14_7/ICU7/TIN7/TTG15/7		86	VSS5
24	P15_4/OCU4/TOT4		85	NMIX
25	P15_5/OCU5/TOT5		84	INITX
26	P15_6/OCU6/TOT6		83	X1A
27	P15_7/OCU7/TOT7		82	X0A
28	P17_0/PPG0		81	VSS5
29	P17_1/PPG1		80	X0
30	P17_2/PPG2		79	X1
31	P17_3/PPG3		78	MD_3
32	P17_4/PPG4		77	MONCLK
33	P17_5/PPG5		76	MD_2
34	P17_6/PPG6		75	MD_1
35	P17_7/PPG7		74	MD_0
36	VDD35		73	VSS5

Top pins (144–109):
VDD35, P27_5/AN21, P27_4/AN20, P27_3/AN19, P27_2/AN18, P27_1/AN17, P27_0/AN16, P15_3/OCU3/TOT3, P15_2/OCU2/TOT2, P15_1/OCU1/TOT1, P15_0/OCU0/TOT0, P14_3/ICU3/TIN3/TTG3/11, P14_2/ICU2/TIN2/TTG2/10, P14_1/ICU1/TIN1/TTG1/9, P14_0/ICU0/TIN0/TTG3/8, P24_3/INT3, P24_2/INT2, VSS5, VDD5, P28_7/AN15, P28_6/AN14, P28_5/AN13, P28_4/AN12, P28_3/AN11, P28_2/AN10, P28_1/AN9, P28_0/AN8, P29_7/AN7, P29_6/AN6, P29_5/AN5, P29_4/AN4, P29_3/AN3, P29_2/AN2, P29_1/AN1, P29_0/AN0, VSS5

Bottom pins (37–72):
VSS5, P20_0/SIN2/AIN0, P20_1/SOT2/BIN0, P20_2/SCK2/ZIN0/CK2, P20_4/SIN3/AIN1, P20_5/SOT3/BIN1, P20_6/SCK3/ZIN1/CK3, P24_0/INT0, P24_1/INT1, P23_0/RX0/INT8, P23_1/TX0, P23_2/RX1/INT9, P23_3/TX1, P23_4/RX2/INT10, P23_5/TX2, P23_6/RX3/INT11, P23_7/TX3, VDD5, VSS5, P22_0/RX4/INT12, P22_1/TX4, P22_2/RX5/INT13, P22_3/TX5, P22_4/SDA0/INT14, P22_5/SCL0, P22_6/SDA1/INT15, P22_7/SCL1, P16_0/PPG8, P16_1/PPG9, P16_2/PPG10, P16_3/PPG11, P16_4/PPG12/SGA, P16_5/PPG13/SGO, P16_6/PPG14, P16_7/PPG15/ATGX, VDD5

2.3   MB91F465BB/464BB with MD_3=1

(TOP VIEW)

LQFP-144

Left side pins (top to bottom):

Pin	Name
1	VSS5
2	P07_6/A6
3	P07_7/A7
4	P06_0/A8
5	P06_1/A9
6	P06_2/A10
7	P06_3/A11
8	P06_4/A12
9	P06_5/A13
10	P06_6/A14
11	P06_7/A15
12	P05_0/A16
13	P05_1/A17
14	P05_2/A18
15	P05_3/A19
16	P05_4/A20
17	P05_5/A21
18	VDD35
19	VSS5
20	P01_0/D16
21	P01_1/D17
22	P01_2/D18
23	P01_3/D19
24	P01_4/D20
25	P01_5/D21
26	P01_6/D22
27	P01_7/D23
28	P00_0/D24
29	P00_1/D25
30	P00_2/D26
31	P00_3/D27
32	P00_4/D28
33	P00_5/D29
34	P00_6/D30
35	P00_7/D31
36	VDD35

Right side pins (top to bottom):

Pin	Name
108	VDD5
107	AVCC5
106	AVRH5
105	AVSS5
104	ALARM_0
103	P18_6/SCK7/CK7
102	P18_5/SOT7
101	P18_4/SIN7
100	P18_2/SCK6/CK6
99	P18_1/SOT6
98	P18_0/SIN6
97	P19_6/SCK5/CK5
96	P19_5/SOT5
95	P19_4/SIN5
94	P19_2/SCK4/CK4
93	P19_1/SOT4
92	P19_0/SIN4
91	VSS5
90	VDD5
89	VDD5R
88	VDD5R
87	VCC18C
86	VSS5
85	NMIX
84	INITX
83	X1A
82	X0A
81	VSS5
80	X0
79	X1
78	MD_3
77	MONCLK
76	MD_2
75	MD_1
74	MD_0
73	VSS5

Top side pins (left to right, pins 144 to 109):

Pin	Name
144	VDD35
143	P07_5/A5
142	P07_4/A4
141	P07_3/A3
140	P07_2/A2
139	P07_1/A1
138	P07_0/A0
137	P15_3/OCU3/TOT3
136	P15_2/OCU2/TOT2
135	P15_1/OCU1/TOT1
134	P15_0/OCU0/TOT0
133	P14_3/ICU3/TIN3/TTG3/11
132	P14_2/ICU2/TIN2/TTG2/10
131	P14_1/ICU1/TIN1/TTG1/9
130	P14_0/ICU0/TIN0/TTG0/8
129	P24_3/INT3
128	P24_2/INT2
127	VSS5
126	VDD5
125	P28_7/AN15
124	P28_6/AN14
123	P28_5/AN13
122	P28_4/AN12
121	P28_3/AN11
120	P28_2/AN10
119	P28_1/AN9
118	P28_0/AN8
117	P29_7/AN7
116	P29_6/AN6
115	P29_5/AN5
114	P29_4/AN4
113	P29_3/AN3
112	P29_2/AN2
111	P29_1/AN1
110	P29_0/AN0
109	VSS5

Bottom side pins (left to right, pins 37 to 72):

Pin	Name
37	VSS5
38	P10_0/SYSCLK
39	P09_0/CSX0
40	P09_1/CSX1
41	P08_0/WRX0
42	P08_4/RDX
43	P08_7/RDY
44	P08_1/WRX1
45	P24_1/INT1
46	P23_0/RX0/INT8
47	P23_1/TX0
48	P23_2/RX1/INT9
49	P23_3/TX1
50	P23_4/RX2/INT10
51	P23_5/TX2
52	P23_6/INT11
53	P23_7
54	VDD5
55	P22_1
56	VSS5
57	P22_0/INT12
58	P22_2/INT13
59	P22_3
60	P22_4/SDA0/INT14
61	P22_5/SCL0
62	P22_6/SDA1/INT15
63	P22_7/SCL1
64	P16_0/PPG8
65	P16_1/PPG9
66	P16_2/PPG10
67	P16_3/PPG11
68	P16_4/PPG12/SGA
69	P16_5/PPG13/SGO
70	P16_6/PPG14
71	P16_7/PPG15/ATGX
72	VDD5

2.4 MB91F465BB/464BB with MD_3=0

(TOP VIEW)

LQFP-144

Left side pins (1-36):
- 1 VSS5
- 2 P27_6/AN22
- 3 P27_7/AN23
- 4 P26_0/AN24
- 5 P26_1/AN25
- 6 P26_2/AN26
- 7 P26_3/AN27
- 8 P26_4/AN28
- 9 P26_5/AN29
- 10 P26_6/AN30
- 11 P26_7/AN31
- 12 P24_4/INT4
- 13 P24_5/INT5
- 14 P24_6/INT6
- 15 P24_7/INT7
- 16 P21_0/SIN0
- 17 P21_1/SOT0
- 18 VDD35
- 19 VSS5
- 20 P14_4/ICU4/TIN4/TTG12/4
- 21 P14_5/ICU5/TIN5/TTG13/5
- 22 P14_6/ICU6/TIN6/TTG14/6
- 23 P14_7/ICU7/TIN7/TTG15/7
- 24 P15_4/OCU4/TOT4
- 25 P15_5/OCU5/TOT5
- 26 P15_6/OCU6/TOT6
- 27 P15_7/OCU7/TOT7
- 28 P17_0/PPG0
- 29 P17_1/PPG1
- 30 P17_2/PPG2
- 31 P17_3/PPG3
- 32 P17_4/PPG4
- 33 P17_5/PPG5
- 34 P17_6/PPG6
- 35 P17_7/PPG7
- 36 VDD35

Right side pins (73-108):
- 108 VDD5
- 107 AVCC5
- 106 AVRH5
- 105 AVSS5
- 104 ALARM_0
- 103 P18_6/SCK7/CK7
- 102 P18_5/SOT7
- 101 P18_4/SIN7
- 100 P18_2/SCK6/CK6
- 99 P18_1/SOT6
- 98 P18_0/SIN6
- 97 P19_6/SCK5/CK5
- 96 P19_5/SOT5
- 95 P19_4/SIN5
- 94 P19_2/SCK4/CK4
- 93 P19_1/SOT4
- 92 P19_0/SIN4
- 91 VSS5
- 90 VDD5
- 89 VDD5R
- 88 VDD5R
- 87 VCC18C
- 86 VSS5
- 85 NMIX
- 84 INITX
- 83 X1A
- 82 X0A
- 81 VSS5
- 80 X0
- 79 X1
- 78 MD_3
- 77 MONCLK
- 76 MD_2
- 75 MD_1
- 74 MD_0
- 73 VSS5

Top side pins (109-144):
- 144 VDD35
- 143 P27_5/AN21
- 142 P27_4/AN20
- 141 P27_3/AN19
- 140 P27_2/AN18
- 139 P27_1/AN17
- 138 P27_0/AN16
- 137 P15_3/OCU3/TOT3
- 136 P15_2/OCU2/TOT2
- 135 P15_1/OCU1/TOT1
- 134 P15_0/OCU0/TOT0
- 133 P14_3/ICU3/TIN3/TTG3/11
- 132 P14_2/ICU2/TIN2/TTG2/10
- 131 P14_1/ICU1/TIN1/TTG1/9
- 130 P14_0/ICU0/TIN0/TTG0/8
- 129 P24_3/INT3
- 128 P24_2/INT2
- 127 VSS5
- 126 VDD5
- 125 P28_7/AN15
- 124 P28_6/AN14
- 123 P28_5/AN13
- 122 P28_4/AN12
- 121 P28_3/AN11
- 120 P28_2/AN10
- 119 P28_1/AN9
- 118 P28_0/AN8
- 117 P29_7/AN7
- 116 P29_6/AN6
- 115 P29_5/AN5
- 114 P29_4/AN4
- 113 P29_3/AN3
- 112 P29_2/AN2
- 111 P29_1/AN1
- 110 P29_0/AN0
- 109 VSS5

Bottom side pins (37-72):
- 37 VSS5
- 38 P20_0/SIN2/AIN0
- 39 P20_1/SOT2/BIN0
- 40 P20_2/SCK2/ZIN0/CK2
- 41 P20_4/SIN3/AIN1
- 42 P20_5/SOT3/BIN1
- 43 P20_6/SCK3/ZIN1/CK3
- 44 P24_0/INT0
- 45 P24_1/INT1
- 46 P23_0/RX0/INT8
- 47 P23_1/TX0
- 48 P23_2/RX1/INT9
- 49 P23_3/TX1
- 50 P23_4/RX2/INT10
- 51 P23_5/TX2
- 52 P23_6/INT11
- 53 P23_7
- 54 VDD5
- 55 VSS5
- 56 P22_0/INT12
- 57 P22_1
- 58 P22_2/INT13
- 59 P22_3
- 60 P22_4/SDA0/INT14
- 61 P22_5/SCL0
- 62 P22_6/SDA1/INT15
- 63 P22_7/SCL1
- 64 P16_0/PPG8
- 65 P16_1/PPG9
- 66 P16_2/PPG10
- 67 P16_3/PPG11
- 68 P16_4/PPG12/SGA
- 69 P16_5/PPG13/SGO
- 70 P16_6/PPG14
- 71 P16_7/PPG15/ATGX
- 72 VDD5

3. Pin Description

3.1 MB91F467BA/466BA AND MB91F465BB/464BB with MD_3=1

Pin no.	Pin name	I/O	I/O circuit type[1]	Function
2, 3	P07_6, P07_7	I/O	B	General-purpose input/output port
	A6, A7			Signal pins of external address bus (bit6 to bit7)
4 to 11	P06_0 to P06_7	I/O	B	General-purpose input/output port
	A8 to A15			Signal pins of external address bus (bit8 to bit15)
12 to 17	P05_0 to P05_5	I/O	A	General-purpose input/output port
	A16 to A21			Signal pins of external address bus (bit16 to bit21)
20 to 27	P01_0 to P01_7	I/O	A	General-purpose input/output port
	D16 to D23			Signal pins of external data bus (bit16 to bit23)
28 to 35	P00_0 to P00_7	I/O	A	General-purpose input/output port
	D24 to D31			Signal pins of external data bus (bit24 to bit31)
38	P10_0	I/O	A	General-purpose input/output port
	SYSCLK			External bus clock output pin
39	P09_0	I/O	A	General-purpose input/output port
	CSX0			Chip select output pins
40	P09_1	I/O	A	General-purpose input/output port
	CSX1			Chip select output pins
41	P08_0	I/O	A	General-purpose input/output port
	WRX0			External write strobe output pins
42	P08_4	I/O	A	General-purpose input/output port
	RDX			External read strobe output pin
43	P08_7	I/O	A	General-purpose input/output port
	RDY			External ready input pin
44	P08_1 Not on MB91F467BA/MB91F466BA	I/O	A	General-purpose input/output port
	WRX1			External write strobe output pins
	INT0 Not on MB91F467BA/MB91F466BA			External interrupt input, can only be used in general-purpose IO port mode
45	P24_1	I/O	A	General-purpose input/output port
	INT1			External interrupt input pins
46	P23_0	I/O	A	General-purpose input/output port
	RX0			RX input pin of CAN0
	INT8			External interrupt input pins
47	P23_1	I/O	A	General-purpose input/output port
	TX0			TX output pin of CAN0

Pin no.	Pin name	I/O	I/O circuit type[1]	Function
48	P23_2	I/O	A	General-purpose input/output port
	RX1			RX input pin of CAN1
	INT9			External interrupt input pins
49	P23_3	I/O	A	General-purpose input/output port
	TX1			TX output pin of CAN1
50	P23_4	I/O	A	General-purpose input/output port
	RX2			RX input pin of CAN2
	INT10			External interrupt input pin
51	P23_5	I/O	A	General-purpose input/output port
	TX2			TX output pin of CAN2
52	P23_6	I/O	A	General-purpose input/output port
	INT11			External interrupt input pin
	MB91F467BA/MB91F466BA: RX3			RX input pin of CAN3
53	P23_7	I/O	A	General-purpose input/output port
	MB91F467BA/MB91F466BA: TX3			TX output pin of CAN3
56	P22_0	I/O	A	General-purpose input/output port
	INT12			External interrupt input pin
	MB91F467BA/MB91F466BA: RX4			RX input pin of CAN4
57	P22_1	I/O	A	General-purpose input/output port
	MB91F467BA/MB91F466BA: TX4			TX output pin of CAN4
58	P22_2	I/O	A	General-purpose input/output port
	INT13			External interrupt input pin
	MB91F467BA/MB91F466BA: RX5			RX input pin of CAN5
59	P22_3	I/O	A	General-purpose input/output port
	MB91F467BA/MB91F466BA: TX5			TX output pin of CAN5
60	P22_4	I/O	C	General-purpose input/output port
	SDA0			I^{2}C bus DATA input/output pin (open drain)
	INT14			External interrupt input pin
61	P22_5	I/O	C	General-purpose input/output port
	SCL0			I^{2}C bus clock input/output pin (open drain)
62	P22_6	I/O	C	General-purpose input/output port
	SDA1			I^{2}C bus DATA input/output pin (open drain)
	INT15			External interrupt input pin
63	P22_7	I/O	C	General-purpose input/output port
	SCL1			I^{2}C bus clock input/output pin (open drain)

Pin no.	Pin name	I/O	I/O circuit type[1]	Function
64	P16_0	I/O	A	General-purpose input/output port
	PPG8			Output pins of PPG timer
65	P16_1	I/O	A	General-purpose input/output port
	PPG9			Output pins of PPG timer
66	P16_2	I/O	A	General-purpose input/output port
	PPG10			Output pins of PPG timer
67	P16_3	I/O	A	General-purpose input/output port
	PPG11			Output pins of PPG timer
68	P16_4	I/O	A	General-purpose input/output port
	PPG12			Output pins of PPG timer
	SGA			SGA output pin of sound generator
69	P16_5	I/O	A	General-purpose input/output port
	PPG13			Output pins of PPG timer
	SGO			SG0 output pin of sound generator
70	P16_6	I/O	A	General-purpose input/output port
	PPG14			Output pins of PPG timer
71	P16_7	I/O	A	General-purpose input/output port
	PPG15			Output pins of PPG timer
	ATGX			A/D converter external trigger input pin
74 to 76	MD_0 to MD_2	I	G	Mode setting pins
77	MONCLK	O	M	Clock monitor pin
78	MD_3	I	H	Mode setting pin
79	X1	—	J1	Clock (oscillation) output
80	X0	—	J1	Clock (oscillation) input
82	X0A	—	J2	Sub clock (oscillation) input
83	X1A	—	J2	Sub clock (oscillation) output
84	INITX	I	H	External reset input pin
85	NMIX	I	H	Non-maskable interrupt input pin
92	P19_0	I/O	A	General-purpose input/output port
	SIN4			Data input pin of USART4
93	P19_1	I/O	A	General-purpose input/output port
	SOT4			Data output pin of USART4
94	P19_2	I/O	A	General-purpose input/output port
	SCK4			Clock input/output pin of USART4
	CK4			External clock input pin of free-run timer 4
95	P19_4	I/O	A	General-purpose input/output port
	SIN5			Data input pin of USART5
96	P19_5	I/O	A	General-purpose input/output port
	SOT5			Data output pin of USART5

Pin no.	Pin name	I/O	I/O circuit type[1]	Function
97	P19_6	I/O	A	General-purpose input/output port
	SCK5			Clock input/output pin of USART5
	CK5			External clock input pin of free-run timer 5
98	P18_0	I/O	A	General-purpose input/output port
	SIN6			Data input pin of USART6
99	P18_1	I/O	A	General-purpose input/output port
	SOT6			Data output pin of USART6
100	P18_2	I/O	A	General-purpose input/output port
	SCK6			Clock input/output pin of USART6
	CK6			External clock input pin of free-run timer 6
101	P18_4	I/O	A	General-purpose input/output port
	SIN7			Data input pin of USART7
102	P18_5	I/O	A	General-purpose input/output port
	SOT7			Data output pin of USART7
103	P18_6	I/O	A	General-purpose input/output port
	SCK7			Clock input/output pin of USART7
	CK7			External clock input pin of free-run timer 7
104	ALARM_0	O	N	Alarm comparator input pin
110 to 117	P29_0 to P29_7	I/O	B	General-purpose input/output port
	AN0 to AN7			Analog input pins of A/D converter
118 to 125	P28_0 to P28_7	I/O	B	General-purpose input/output port
	AN8 to AN15			Analog input pins of A/D converter
128	P24_2	I/O	A	General-purpose input/output port
	INT2			External interrupt input pin
129	P24_3	I/O	A	General-purpose input/output port
	INT3			External interrupt input pin
130 to 133	P14_0 to P14_3	I/O	A	General-purpose input/output port
	ICU0 to ICU3			Input capture input pins
	TIN0 to TIN3			External trigger input pins of reload timer
	TTG0/8 to TTG3/11			External trigger input pins of PPG timer
134 to 137	P15_0 to P15_3	I/O	A	General-purpose input/output port
	OCU0 to OCU3			Output compare output pins
	TOT0 to TOT3			Reload timer output pins
138 to 143	P07_0 to P07_5	I/O	B	General-purpose input/output port
	A0 to A5			Signal pins of external address bus (bit0 to bit5)

3.1.1 Power supply/Ground pins

Pin no.	Pin name	I/O	Function
1, 19, 37, 55, 73, 81, 86, 91, 109, 127	VSS5	Supply	Ground pins
54, 72, 90, 108, 126	VDD5		Power supply pins
88, 89	VDD5R		Power supply pins for internal regulator
105	AVSS5		Analog ground pin for A/D converter
107	AVCC5		Power supply pin for A/D converter
106	AVRH5		Reference power supply pin for A/D converter
87	VCC18C		Capacitor connection pin for internal regulator
18, 36, 144	VDD35		Power supply pins for external bus part of I/O ring

3.2 MB91F467BA/466BA AND MB91F465BB/464BB with MD_3=0

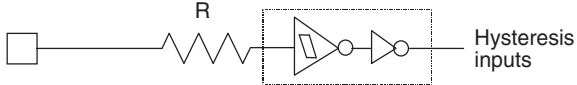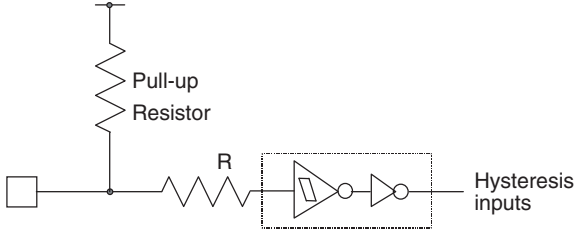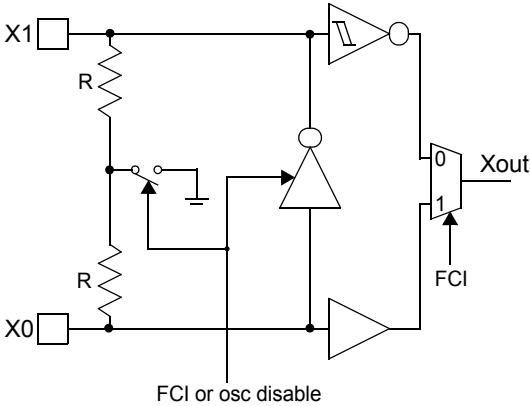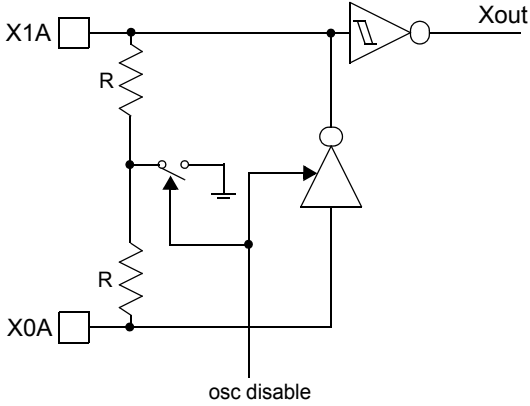| Pin no.	Pin name	I/O	I/O circuit type[1]	Function
2 to 3	P27_6 to P27_7	I/O	B	General-purpose input/output ports
	AN22 to AN23			Analog input pins of A/D converter
4 to 11	P26_0 to P26_7	I/O	B	General-purpose input/output ports
	AN24 to AN31			Analog input pins of A/D converter
12 to 15	P24_4 to P24_7	I/O	A	General-purpose input/output ports
	INT4 to INT7			External interrupt input pins
16	P21_0	I/O	A	General-purpose input/output ports
	SIN0			Data input pin of USART0
17	P21_1	I/O	A	General-purpose input/output ports
	SOT0			Data output pin of USART0
20 to 23	P14_4 to P14_7	I/O	A	General-purpose input/output ports
	ICU4 to ICU7			Input capture input pins
	TIN4 to TIN7			External trigger input pins of reload timer
	TTG4/12 to TTG7/15			External trigger input pins of PPG timer
24 to 27	P15_4 to P15_7	I/O	A	General-purpose input/output ports
	OCU4 to OCU7			Output compare output pins
	TOT4 to TOT7			Reload timer output pins
28 to 35	P17_0 to P17_7	I/O	A	General-purpose input/output ports
	PPG0 to PPG7			Output pins of PPG timer
38	P20_0	I/O	A	General-purpose input/output ports
	SIN2			Data input pin of USART2
	AIN0			Up/down counter input pin
39	P20_1	I/O	A	General-purpose input/output ports
	SOT2			Data output pin of USART2
	BIN0			Up/down counter input pin
40	P20_2	I/O	A	General-purpose input/output ports
	SCK2			Clock input/output pin of USART2
	ZIN0			Up/down counter input pin
	CK2			External clock input pin of free-run timer 2
41	P20_4	I/O	A	General-purpose input/output ports
	SIN3			Data input pin of USART3
	AIN1			Up/down counter input pin
42	P20_5	I/O	A	General-purpose input/output ports
	SOT3			Data output pin of USART3
	BIN1			Up/down counter input pin
43	P20_6	I/O	A	General-purpose input/output ports
	SCK3			Clock input/output pin of USART3
	ZIN1			Up/down counter input pin
	CK3			External clock input pin of free-run timer 3

Pin no.	Pin name	I/O	I/O circuit type[1]	Function
44	P24_0	I/O	A	General-purpose input/output ports
	INT0			External interrupt input pin
45	P24_1	I/O	A	General-purpose input/output ports
	INT1			External interrupt input pin
46	P23_0	I/O	A	General-purpose input/output ports
	RX0			RX input pin of CAN0
	INT8			External interrupt input pin
47	P23_1	I/O	A	General-purpose input/output ports
	TX0			TX output pin of CAN0
48	P23_2	I/O	A	General-purpose input/output ports
	RX1			RX input pin of CAN1
	INT9			External interrupt input pin
49	P23_3	I/O	A	General-purpose input/output ports
	TX1			TX output pin of CAN1
50	P23_4	I/O	A	General-purpose input/output ports
	RX2			RX input pin of CAN2
	INT10			External interrupt input pin
51	P23_5	I/O	A	General-purpose input/output ports
	TX2			TX output pin of CAN2
52	P23_6	I/O	A	General-purpose input/output ports
	MB91F467BA/MB91F466BA: RX3			RX input pin of CAN3
	INT11			External interrupt input pin
53	P23_7 MB91F467BA/MB91F466BA: TX3	I/O	A	General-purpose input/output ports
				TX output pin of CAN3
56	P22_0	I/O	A	General-purpose input/output port
	MB91F467BA/MB91F466BA: RX4			RX input pin of CAN4
	INT12			External interrupt input pin
57	P22_1	I/O	A	General-purpose input/output port
	MB91F467BA/MB91F466BA: TX4			TX output pin of CAN4
58	P22_2	I/O	A	General-purpose input/output port
	INT13			External interrupt input pin
	MB91F467BA/MB91F466BA: RX5			RX input pin of CAN5
59	P22_3	I/O	A	General-purpose input/output port
	MB91F467BA/MB91F466BA: TX5			TX output pin of CAN5

Pin no.	Pin name	I/O	I/O circuit type[1]	Function
60	P22_4	I/O	C	General-purpose input/output ports
	SDA0			I^2C bus DATA input/output pin (open drain)
	INT14			External interrupt input pin
61	P22_5	I/O	C	General-purpose input/output ports
	SCL0			I^2C bus clock input/output pin (open drain)
62	P22_6	I/O	C	General-purpose input/output ports
	SDA1			I^2C bus DATA input/output pin (open drain)
	INT15			External interrupt input pin
63	P22_7	I/O	C	General-purpose input/output ports
	SCL1			I^2C bus clock input/output pin (open drain)
64 to 67	P16_0 to P16_3	I/O	A	General-purpose input/output ports
	PPG8 to PPG11			Output pins of PPG timer
68	P16_4	I/O	A	General-purpose input/output ports
	PPG12			Output pins of PPG timer
	SGA			SGA output pin of sound generator
69	P16_5	I/O	A	General-purpose input/output ports
	PPG13			Output pins of PPG timer
	SGO			SG0 output pin of sound generator
70	P16_6	I/O	A	General-purpose input/output ports
	PPG14			Output pins of PPG timer
71	P16_7	I/O	A	General-purpose input/output ports
	PPG15			Output pins of PPG timer
	ATGX			A/D converter external trigger input pin
74 to 76	MD_0 to MD_2	I	G	Mode setting pins
77	MONCLK	O	M	Clock monitor pin
78	MD_3	I	H	Mode setting pins
79	X1	—	J1	Clock (oscillation) output
80	X0	—	J1	Clock (oscillation) input
82	X0A	—	J2	Sub clock (oscillation) input
83	X1A	—	J2	Sub clock (oscillation) output
84	INITX	I	H	External reset input pin
85	NMIX	I	H	Non-maskable interrupt input pin
92	P19_0	I/O	A	General-purpose input/output ports
	SIN4			Data input pin of USART4
93	P19_1	I/O	A	General-purpose input/output ports
	SOT4			Data output pin of USART4
94	P19_2	I/O	A	General-purpose input/output ports
	SCK4			Clock input/output pin of USART4
	CK4			External clock input pin of free-run timer 4

Pin no.	Pin name	I/O	I/O circuit type[1]	Function
95	P19_4	I/O	A	General-purpose input/output ports
	SIN5			Data input pin of USART5
96	P19_5	I/O	A	General-purpose input/output ports
	SOT5			Data output pin of USART5
97	P19_6	I/O	A	General-purpose input/output ports
	SCK5			Clock input/output pin of USART5
	CK5			External clock input pin of free-run timer 5
98	P18_0	I/O	A	General-purpose input/output ports
	SIN6			Data input pin of USART6
99	P18_1	I/O	A	General-purpose input/output ports
	SOT6			Data output pin of USART6
100	P18_2	I/O	A	General-purpose input/output ports
	SCK6			Clock input/output pin of USART6
	CK6			External clock input pin of free-run timer 6
101	P18_4	I/O	A	General-purpose input/output ports
	SIN7			Data input pin of USART7
102	P18_5	I/O	A	General-purpose input/output ports
	SOT7			Data output pin of USART7
103	P18_6	I/O	A	General-purpose input/output ports
	SCK7			Clock input/output pin of USART7
	CK7			External clock input pin of free-run timer 7
104	ALARM_0	I	N	Alarm comparator input pin
110 to 117	P29_0 to P29_7	I/O	B	General-purpose input/output ports
	AN0 to AN7			Analog input pins of A/D converter
118 to 125	P28_0 to P28_7	I/O	B	General-purpose input/output ports
	AN8 to AN15			Analog input pins of A/D converter
128	P24_2	I/O	A	General-purpose input/output ports
	INT2			External interrupt input pin
129	P24_3	I/O	A	General-purpose input/output ports
	INT3			External interrupt input pin
130 to 133	P14_0 to P14_3	I/O	A	General-purpose input/output ports
	ICU0 to ICU3			Input capture input pins
	TIN0 to TIN3			External trigger input pins of reload timer
	TTG0/8 to TTG3/11			External trigger input pins of PPG timer
134 to 137	P15_0 to P15_3	I/O	A	General-purpose input/output ports
	OCU0 to OCU3			Output compare output pins
	TOT0 to TOT3			Reload timer output pins
138 to 143	P27_0 to P27_5	I/O	B	General-purpose input/output ports
	AN16 to AN21			Analog input pins of A/D converter
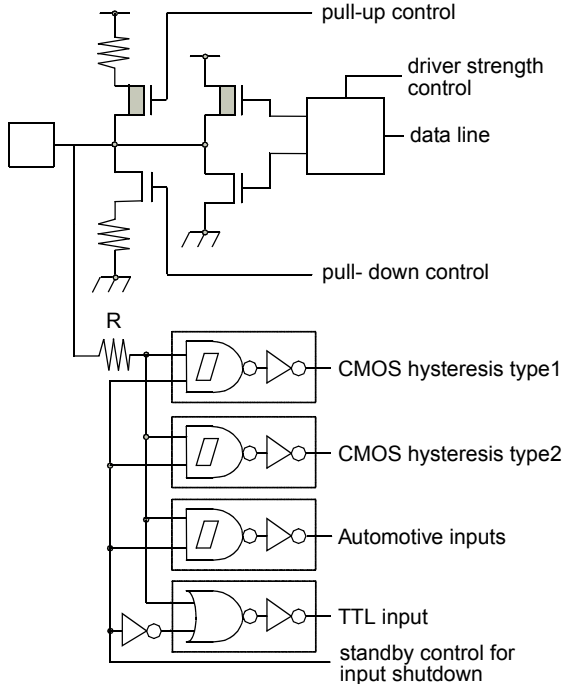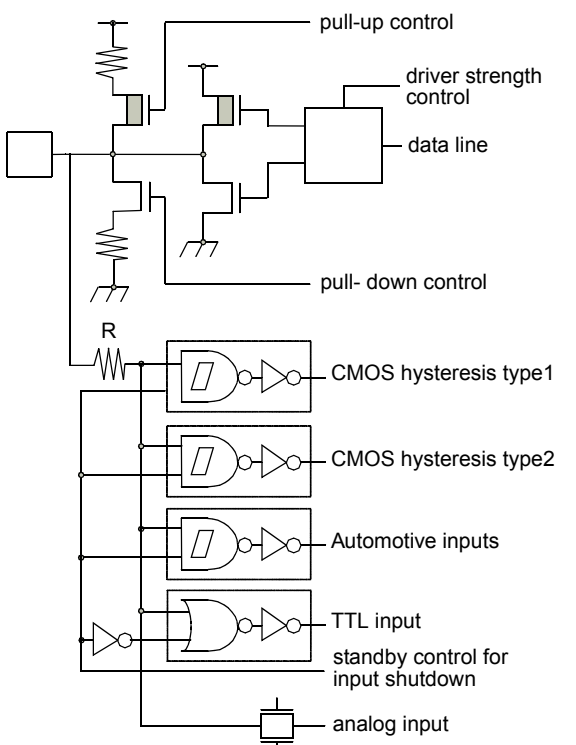
1. For information about the I/O circuit type, refer to "I/O Circuit Types".
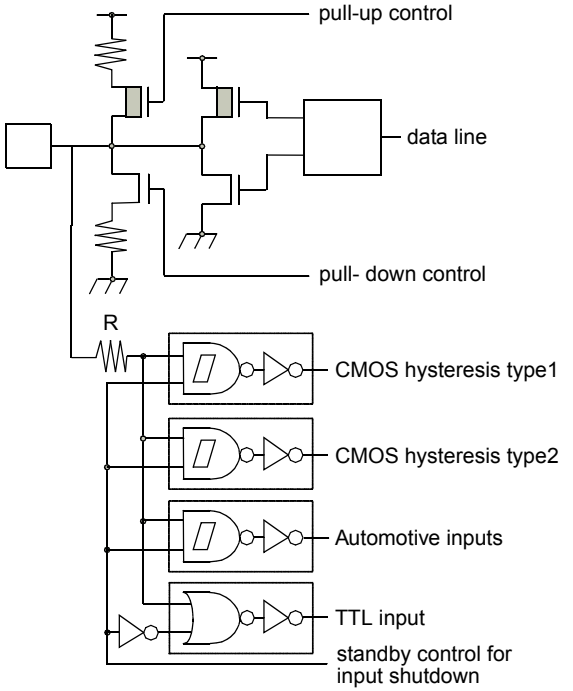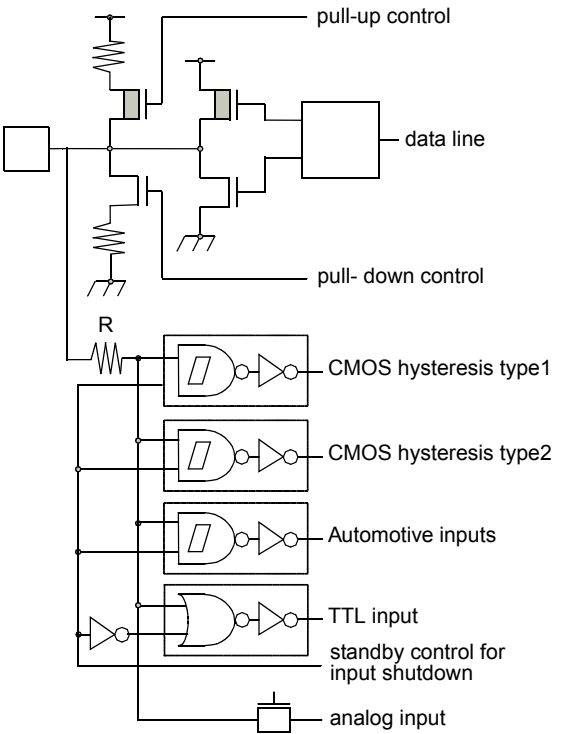
3.2.1   Power supply/Ground pins
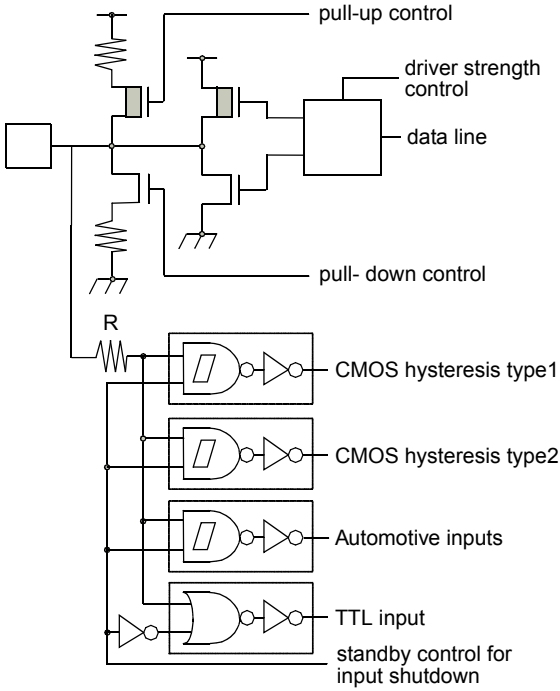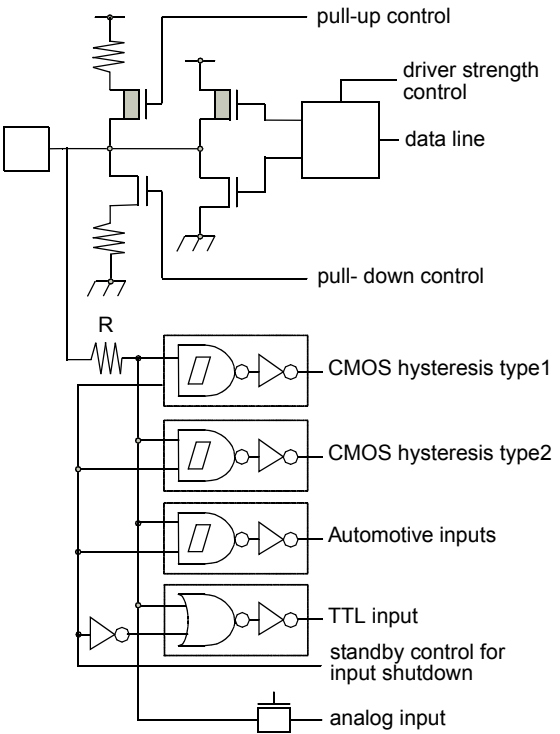
Pin no.	Pin name	I/O	Function
1, 19, 37, 55, 73, 81, 86, 91, 109, 127	VSS5	Supply	Ground pins
54, 72, 90, 108, 126	VDD5		Power supply pins
88, 89	VDD5R		Power supply pins for internal regulator
105	AVSS5		Analog ground pin for A/D converter
107	AVCC5		Power supply pin for A/D converter
106	AVRH5		Reference power supply pin for A/D converter
87	VCC18C		Capacitor connection pin for internal regulator
18, 36, 144	VDD35		Power supply pins for external bus part of I/O ring

1. For information about the I/O circuit type, refer to "I/O Circuit Types".

4. I/O Circuit Types
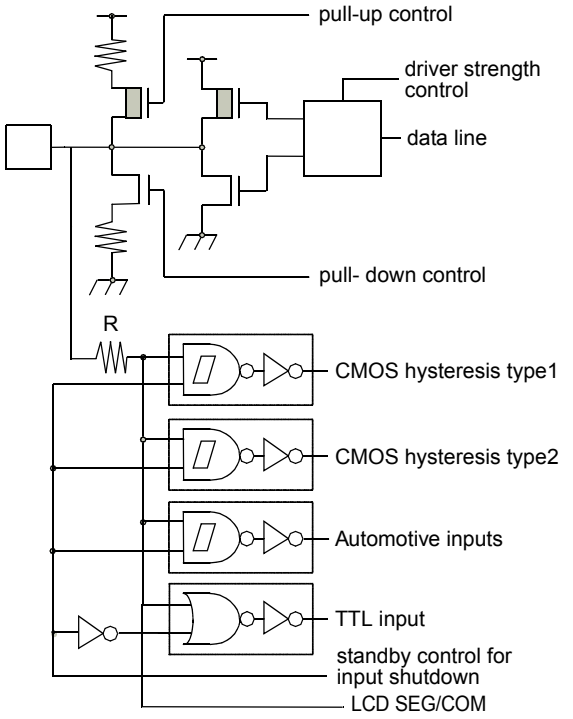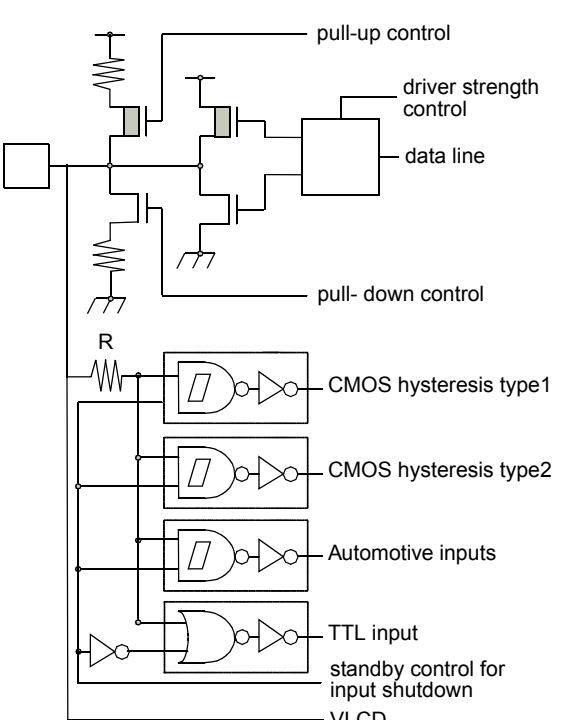
Type	Circuit	Remarks
A		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx.
B		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input

Type	Circuit	Remarks
C		CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx.
D		CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input
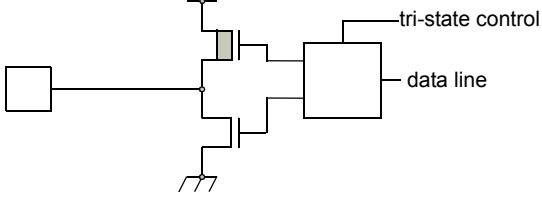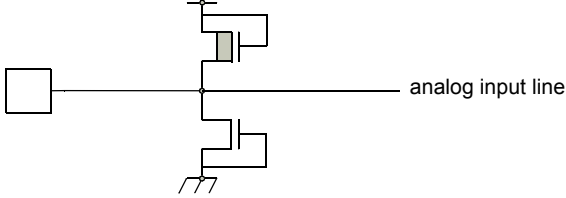
Type	Circuit	Remarks
E	pull-up control driver strength control data line pull-down control R CMOS hysteresis type1 CMOS hysteresis type2 Automotive inputs TTL input standby control for input shutdown	CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA, and I_{OL} = 30mA, I_{OH} = -30mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx.
F	pull-up control driver strength control data line pull-down control R CMOS hysteresis type1 CMOS hysteresis type2 Automotive inputs TTL input standby control for input shutdown analog input	CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA, and I_{OL} = 30mA, I_{OH} = -30mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input

Type	Circuit	Remarks

G	R — Hysteresis inputs	Mask ROM and EVA device:
		  CMOS Hysteresis input pin
		Flash device:
		  CMOS input pin
		  12 V withstand (for MD [2:0])

H	Pull-up Resistor — R — Hysteresis inputs	CMOS Hysteresis input pin Pull-up resistor value: 50 kΩ approx.
J1	X1, R, X0, R, FCI or osc disable, Xout, 0, 1, FCI	High-speed oscillation circuit: ■ Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) ■ Feedback resistor = approx. 2 * 0.5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode.
J2	X1A, R, X0A, R, osc disable, Xout	Low-speed oscillation circuit: ■ Feedback resistor = approx. 2 * 5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled.

Type	Circuit	Remarks
K
pull-up control
driver strength control
data line
pull-down control
R
CMOS hysteresis type1
CMOS hysteresis type2
Automotive inputs
TTL input
standby control for input shutdown
LCD SEG/COM | CMOS level output
(programmable I_{OL} = 5mA, I_{OH} = -5mA
and I_{OL} = 2mA, I_{OH} = -2mA)
2 different CMOS hysteresis inputs with input shutdown function
Automotive input with input shutdown function
TTL input with input shutdown function
Programmable pull-up resistor: 50kΩ approx.
LCD SEG/COM output |
| L |
pull-up control
driver strength control
data line
pull-down control
R
CMOS hysteresis type1
CMOS hysteresis type2
Automotive inputs
TTL input
standby control for input shutdown
VLCD | CMOS level output
(programmable I_{OL} = 5mA, I_{OH} = -5mA
and I_{OL} = 2mA, I_{OH} = -2mA)
2 different CMOS hysteresis inputs with input shutdown function
Automotive input with input shutdown function)
TTL input with input shutdown function
Programmable pull-up resistor: 50kΩ approx.
Analog input
LCD Voltage input |

Type	Circuit	Remarks
M	tri-state control data line	CMOS level tri-state output (I_{OL} = 5mA, I_{OH} = -5mA)
N	analog input line	Analog input pin with protection

5. Handling Devices

5.1 Preventing Latch-up

Latch-up may occur in a CMOS IC if a voltage higher than ($V_{DD}5$, $V_{DD}35$ or $HV_{DD}5$ [1]) or less than ($V_{SS}5$ or $HV_{SS}5$ [1]) is applied to an input or output pin or if a voltage exceeding the rating is applied between the power supply pins and ground pins. If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Therefore, be very careful not to apply voltages in excess of the absolute maximum ratings.

Note: 1. $HV_{DD}5$, $HV_{SS}5$ are available only on devices having Stepper Motor Controller.

5.2 Handling of Unused Input Pins

If unused input pins are left open, abnormal operation may result. Any unused input pins should be connected to pull-up or pull-down resistor (2KΩ to 10KΩ) or enable internal pullup or pulldown resisters (PPER/PPCR) before the input enable (PORTEN) is activated by software. The mode pins MD_x can be connected to $V_{SS}5$ or $V_{DD}5$ directly. Unused ALARM input pins can be connected to $AV_{SS}5$ directly.

5.3 Power Supply Pins

In MB91460 series, devices including multiple power supply pins and ground pins are designed as follows; pins necessary to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. All of the power supply pins and ground pins must be externally connected to the power supply and ground respectively in order to reduce unnecessary radiation, to prevent strobe signal malfunctions due to the ground level rising and to follow the total output current ratings. Furthermore, the power supply pins and ground pins of the MB91460 series must be connected to the current supply source via a low impedance. It is also recommended to connect a ceramic capacitor of approximately 0.1 μF as a bypass capacitor between power supply pin and ground pin near this device. This series has a built-in step-down regulator. Connect a bypass capacitor of 4.7 μF (use a X7R ceramic capacitator) to VCC18C pin for the regulator.

5.4 Crystal Oscillator Circuit

Noise in proximity to the X0 (X0A) and X1 (X1A) pins can cause the device to operate abnormally. Printed circuit boards should be designed so that the X0 (X0A) and X1 (X1A) pins, and crystal oscillator, as well as bypass capacitors connected to ground, are located near the device and ground.
It is recommended that the printed circuit board layout be designed such that the X0 and X1 pins or X0A and X1A pins are surrounded by ground plane for the stable operation. Please request the oscillator manufacturer to evaluate the oscillational characteristics of the crystal and this device.

5.5 Notes on using External Clock

When using the external clock, it is necessary to simultaneously supply the X0 (X0A) and the X1 (X1A) pins. In the described combination, X1 (X1A) should be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins. At X0 and X1, a frequency up to 16 MHz is possible.

Figure 1. Example of using opposite phase supply
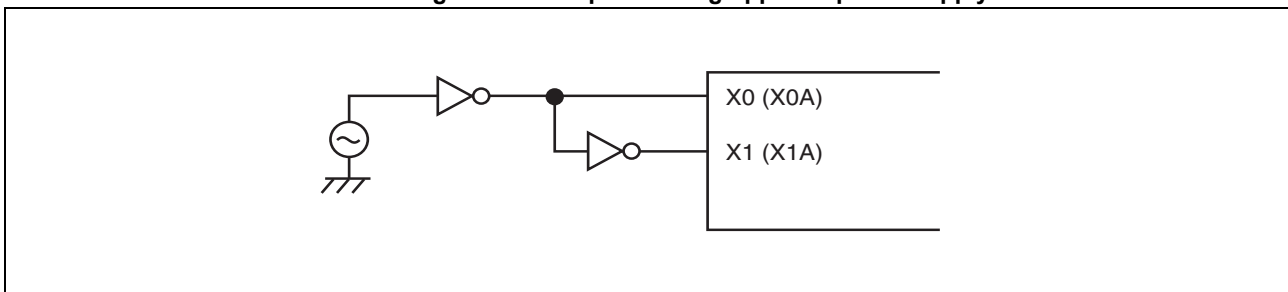
5.6   Mode Pins (MD_x)

These pins should be connected directly to the power supply or ground pins. To prevent the device from entering test mode accidentally due to noise, minimize the lengths of the patterns between each mode pin and power supply pin or ground pin on the printed circuit board as possible and connect them with low impedance.

5.7   Notes on Operating in PLL Clock Mode

If the oscillator is disconnected or the clock input stops when the PLL clock is selected, the microcontroller may continue to operate at the free-running frequency of the self-oscillating circuit of the PLL. However, this self-running operation cannot be guaranteed.

5.8   Pull-up Control

The AC standard is not guaranteed in case a pull-up resistor is connected to the pin serving as an external bus pin.

6. Notes on Debugger

6.1 Execution of the RETI Command

If single-step execution is used in an environment where an interrupt occurs frequently, the corresponding interrupt handling routine will be executed repeatedly to the exclusion of other processing. This will prevent the main routine and the handlers for low priority level interrupts from being executed (For example, if the time-base timer interrupt is enabled, stepping over the RETI instruction will always break on the first line of the time-base timer interrupt handler).

Disable the corresponding interrupts when the corresponding interrupt handling routine no longer needs debugging.

6.2 Break Function

If the range of addresses that cause a hardware break (including event breaks) is set to the address of the current system stack pointer or to an area that contains the stack pointer, execution will break after each instruction regardless of whether the user program actually contains data access instructions.

To prevent this, do not set (word) access to the area containing the address of the system stack pointer as the target of the hardware break (including an event breaks).

6.3 Operand Break

It may cause malfunctions if a stack pointer exists in the area which is set as the DSU operand break. Do not set the access to the areas containing the address of system stack pointer as a target of data event break.

6.4 Notes on PS Register

As the PS register is processed in advance by some instructions, when the debugger is being used, the exception handling may result in execution breaking in an interrupt handling routine or the displayed values of the flags in the PS register being updated. As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event,the operation before and after the EIT always proceeds according to specification.

■ **The following behavior may occur if any of the following occurs in the instruction immediately after a DIV0U/DIV0S instruction:**
(a) a user interrupt or NMI is accepted;
(b) single-step execution is performed;
(c) execution breaks due to a data event or from the emulator menu.
    1. D0 and D1 flags are updated in advance.
    2. An EIT handling routine (user interrupt/NMI or emulator) is executed.
    3. Upon returning from the EIT, the DIV0U/DIV0S instruction is executed and the D0 and D1 flags are updated to the same values as those in 1.

■ **The following behavior occurs when an ORCCR, STILM, MOV Ri,PS instruction is executed to enable a user interrupt or NMI source while that interrupt is in the active state.**
    1. The PS register is updated in advance.
    2. An EIT handling routine (user interrupt/NMI or emulator) is executed.
    3. Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as in 1.

7. Block Diagram

7.1 MB91F467BA/466BA with MD_3=1
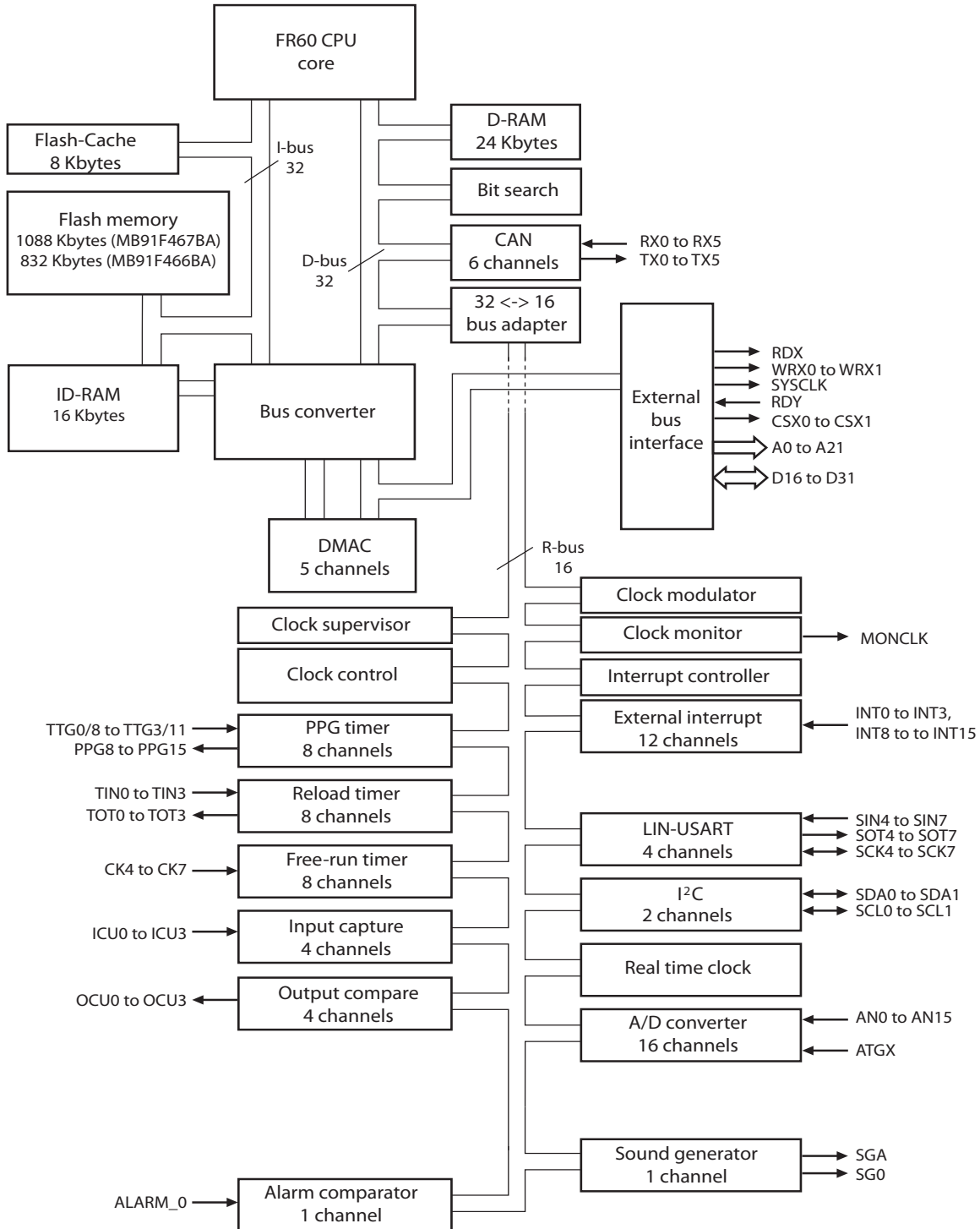
7.2   MB91F467BA/466BA with MD_3=0
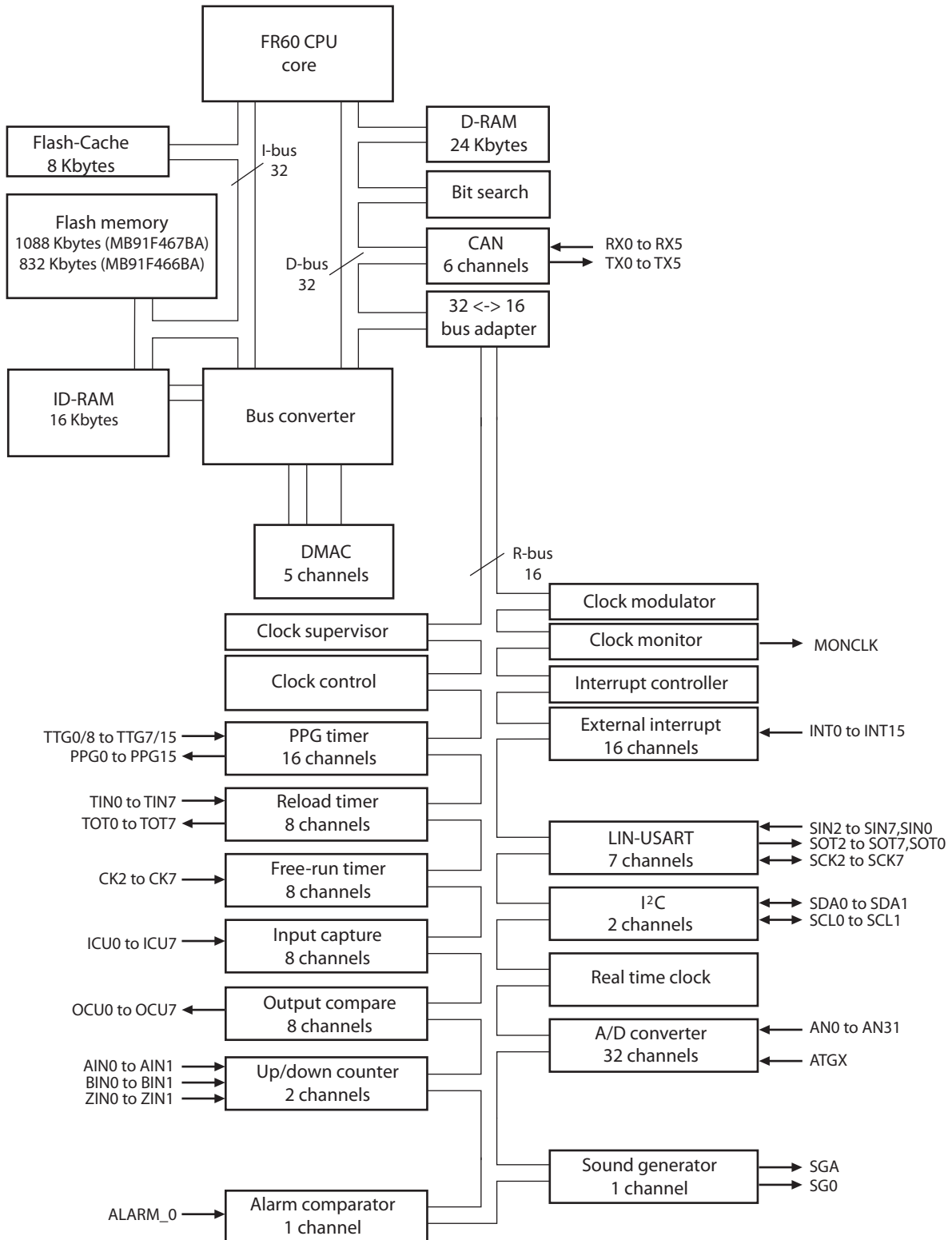
7.3   MB91F465BB/464BB with MD_3=1
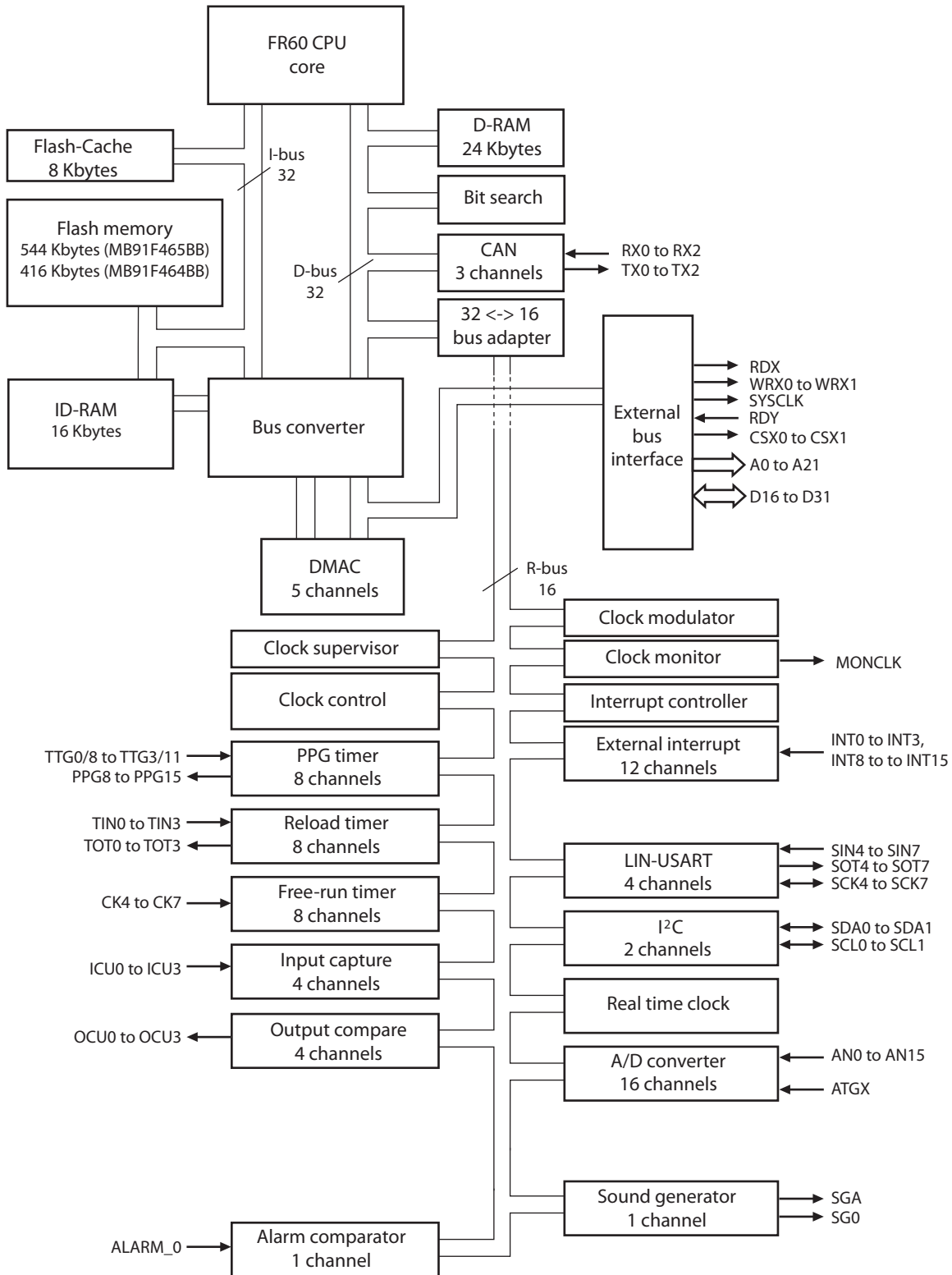
7.4   MB91F465BB/464BB with MD_3=0
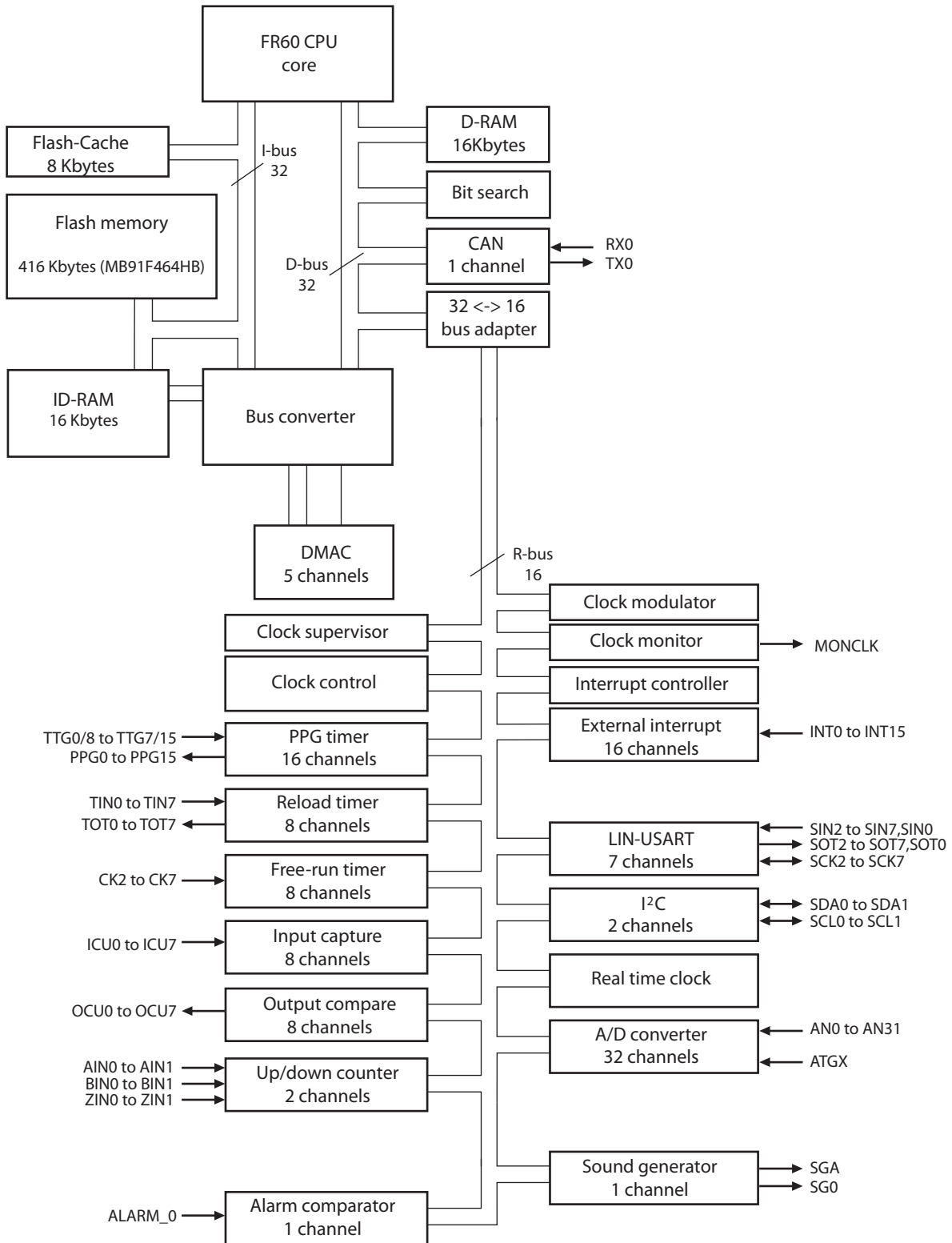
8. CPU and Control Unit

The FR family CPU is a high performance core that is designed based on the RISC architecture with advanced instructions for embedded applications.

8.1 Features

- Adoption of RISC architecture
  Basic instruction: 1 instruction per cycle

- General-purpose registers: 32-bit × 16 registers

- 4 Gbytes linear memory space

- Multiplier installed
  32-bit × 32-bit multiplication: 5 cycles
  16-bit × 16-bit multiplication: 3 cycles

- Enhanced interrupt processing function
  Quick response speed (6 cycles)
  Multiple-interrupt support
  Level mask function (16 levels)

- Enhanced instructions for I/O operation
  Memory-to-memory transfer instruction
  Bit processing instruction
  Basic instruction word length: 16 bits

- Low-power consumption
  Sleep mode/stop mode

8.2 Internal Architecture

- The FR family CPU uses the Harvard architecture in which the instruction bus and data bus are independent of each other.

- A 32-bit ↔ 16-bit buffer is connected to the 32-bit bus (D-bus) to provide an interface between the CPU and peripheral resources.

- A Harvard ↔ Princeton bus converter is connected to both the I-bus and D-bus to provide an interface between the CPU and the bus controller.

8.3 Programming Model

8.3.1 Basic Programming Model

8.4 Registers

8.4.1 General-Purpose Register

Registers R0 to R15 are general-purpose registers. These registers can be used as accumulators for computation operations and as pointers for memory access.

Of the 16 registers, enhanced commands are provided for the following registers to enable their use for particular applications.

R13 : Virtual accumulator

R14 : Frame pointer

R15 : Stack pointer

Initial values at reset are undefined for R0 to R14. The value for R15 is 00000000_H (SSP value).

8.4.2 PS (Program Status)

This register holds the program status, and is divided into three parts, ILM, SCR, and CCR.

All undefined bits (-) in the diagram are reserved bits. The read values are always "0". Write access to these bits is invalid.

8.4.3　CCR (Condition Code Register)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
—	SV	S	I	N	Z	V	C

Initial value

- 000XXXX$_B$
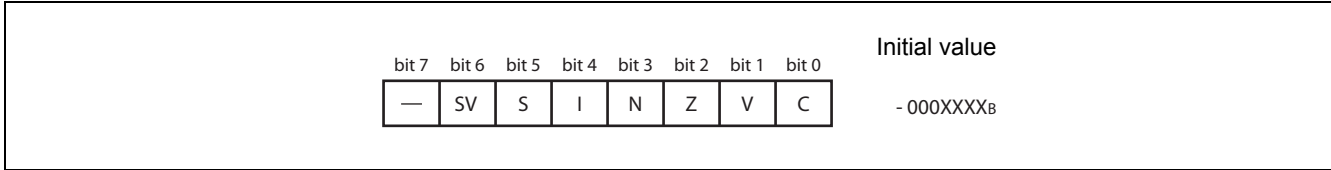
SV: Supervisor flag

S: Stack flag

I: Interrupt enable flag

N: Negative enable flag

Z: Zero flag

V: Overflow flag

C: Carry flag

8.4.4　SCR (System Condition Register)

bit 10	bit 9	bit 8
D1	D0	T

Initial value

XX0$_B$
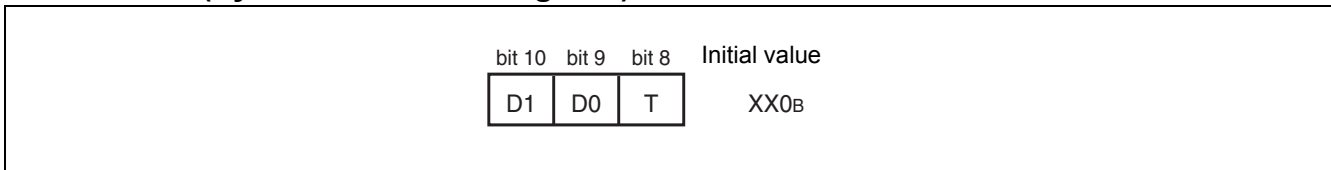
Flag for step division (D1, D0)
This flag stores interim data during execution of step division.

Step trace trap flag (T)
This flag indicates whether the step trace trap is enabled or disabled.
The step trace trap function is used by emulators. When an emulator is in use, it cannot be used in execution of user programs.

8.4.5　ILM (Interrupt Level Mask Register)

bit 20	bit 19	bit 18	bit 17	bit 16
ILM4	ILM3	ILM2	ILM1	ILM0

Initial value
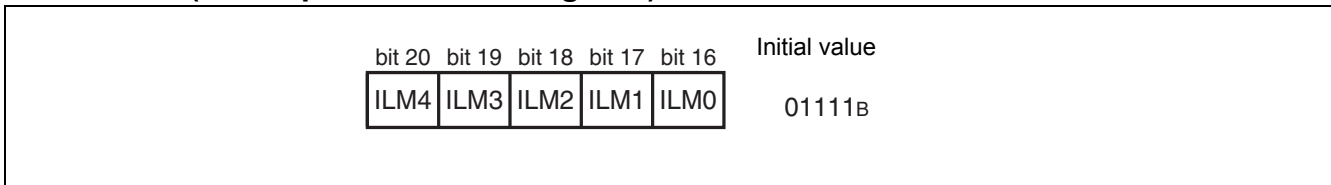
01111$_B$

This register stores interrupt level mask values, and the values stored in ILM4 to ILM0 are used for level masking.

The register is initialized to value "01111$_B$" at reset.

8.4.6　PC (Program Counter)

bit 31　　　　　　　　　　　　　　　　　　　　　　bit 0

Initial value

XXXXXXXX$_H$
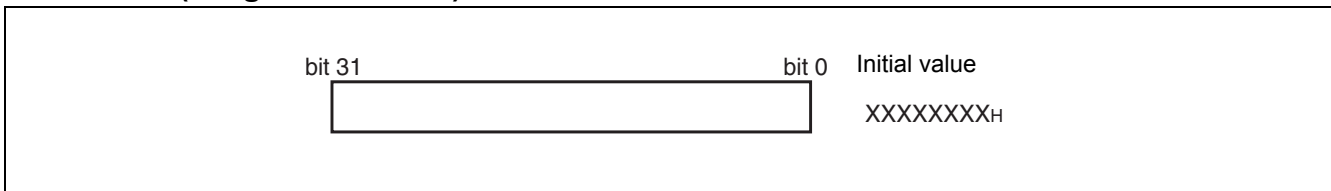
The program counter indicates the address of the instruction that is being executed.

The initial value at reset is undefined.

8.4.7 TBR (Table Base Register)

bit 31   bit 0   Initial value

000FFC00$_H$

The table base register stores the starting address of the vector table used in EIT processing.

The initial value at reset is 000FFC00$_H$.

8.4.8 RP (Return Pointer)

bit 31   bit 0   Initial value

XXXXXXXX$_H$
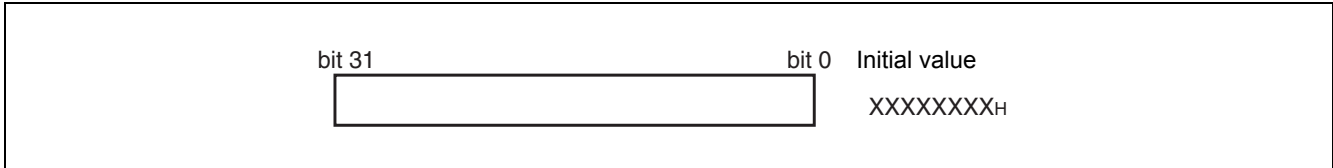
The return pointer stores the address for return from subroutines.

During execution of a CALL instruction, the PC value is transferred to this RP register.

During execution of a RET instruction, the contents of the RP register are transferred to PC.

The initial value at reset is undefined.

8.4.9 USP (User Stack Pointer)

bit 31   bit 0   Initial value

XXXXXXXX$_H$
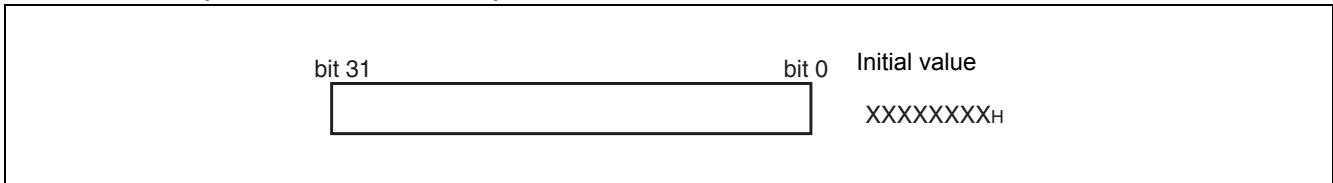
The user stack pointer, when the S flag is "1", this register functions as the R15 register.

■ The USP register can also be explicitly specified.
The initial value at reset is undefined.

■ This register cannot be used with RETI instructions.

8.4.10 Multiply & Divide Registers

bit 31   bit 0

MDH

MDL
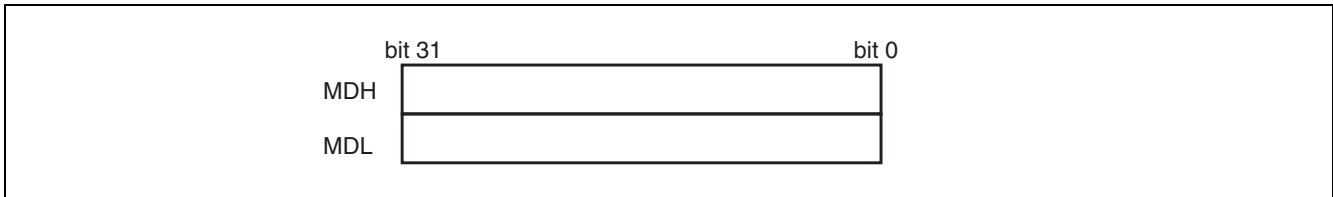
These registers are for multiplication and division, and are each 32 bits in length.

The initial value at reset is undefined.

9. Embedded Program/Data Memory (Flash)

9.1 Flash features

■ MB91F467BA: 1088 Kbytes (16 × 64 Kbytes + 8 × 8 Kbytes = 8.5 Mbits)

■ MB91F466BA: 832 Kbytes (12 × 64 Kbytes + 8 × 8 Kbytes = 6.5 Mbits)

■ MB91F465BB: 544 Kbytes (8 × 64 Kbytes + 4 × 8 Kbytes = 4.25 Mbits)

■ MB91F464BB: 416 Kbytes (6 × 64 Kbytes + 4 × 8 Kbytes = 3.25 Mbits)

■ Programmable wait states for read/write access

■ Flash and Boot security with security vector at 0x0014:8000 - 0x0014:800F

■ Boot security

■ Basic specification: Same as MBM29LV400TC (except size and part of sector configuration)

9.2 Operation Modes

9.2.1 64-bit CPU mode (available on MB91F467BA/466BA only) :

■ CPU reads and executes programs in word (32-bit) length units.

■ Flash writing is not possible.

■ Actual Flash Memory access is performed in d-word (64-bit) length units.

9.2.2 32-bit CPU mode:

■ CPU reads and executes programs in word (32-bit) length units.

■ Actual Flash Memory access is performed in word (32-bit) length units.

9.2.3 16-bit CPU mode:

■ CPU reads and writes in half-word (16-bit) length units.

■ Program execution from the Flash is not possible.

■ Actual Flash Memory access is performed in word (16-bit) length units.

9.2.4 Flash Memory Mode (External Access to Flash Memory Enabled)

Note: The operation mode of the flash memory can be selected using a Boot-ROM function. The function start address is 0xBF60. The parameter description is given in the Hardware Manual in chapter 54.6 "Flash Access Mode Switching".

9.3 Flash Access in CPU mode

9.3.1 Flash Configuration

9.3.1.1 Flash Memory Map MB91F467BA

Address			
0014:FFFFh 0014:C000h	SA6 (8KB)	SA7 (8KB)	ROMS7
0014:BFFFh 0014:8000h	SA4 (8KB)	SA5 (8KB)	
0014:7FFFh 0014:4000h	SA2 (8KB)	SA3 (8KB)	
0014:3FFFh 0014:0000h	SA0 (8KB)	SA1 (8KB)	
0013:FFFFh 0012:0000h	SA22 (64KB)	SA23 (64KB)	ROMS6
0011:FFFFh 0010:0000h	SA20 (64KB)	SA21 (64KB)	
000F:FFFFh 000E:0000h	SA18 (64KB)	SA19 (64KB)	ROMS5
000D:FFFFh 000C:0000h	SA16 (64KB)	SA17 (64KB)	ROMS4
000B:FFFFh 000A:0000h	SA14 (64KB)	SA15 (64KB)	ROMS3
0009:FFFFh 0008:0000h	SA12 (64KB)	SA13 (64KB)	ROMS2
0007:FFFFh 0006:0000h	SA10 (64KB)	SA11 (64KB)	ROMS1
0005:FFFFh 0004:0000h	SA8 (64KB)	SA9 (64KB)	ROMS0

	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]	
32bit read/write	dat[31:0]				dat[31:0]			
64bit read	dat[63:0]							

9.3.1.2 Flash Memory Map MB91F466BA

Addr			
0014:FFFFh 0014:C000h	SA6 (8KB)	SA7 (8KB)	
0014:BFFFh 0014:8000h	SA4 (8KB)	SA5 (8KB)	ROMS7
0014:7FFFh 0014:4000h	SA2 (8KB)	SA3 (8KB)	
0014:3FFFh 0014:0000h	SA0 (8KB)	SA1 (8KB)	
0013:FFFFh 0012:0000h	SA22 (64KB)	SA23 (64KB)	ROMS6
0011:FFFFh 0010:0000h	SA20 (64KB)	SA21 (64KB)	
000F:FFFFh 000E:0000h	SA18 (64KB)	SA19 (64KB)	ROMS5
000D:FFFFh 000C:0000h	SA16 (64KB)	SA17 (64KB)	ROMS4
000B:FFFFh 000A:0000h	SA14 (64KB)	SA15 (64KB)	ROMS3
0009:FFFFh 0008:0000h	SA12 (64KB)	SA13 (64KB)	ROMS2
0007:FFFFh 0006:0000h	SA10 (64KB)	SA11 (64KB)	ROMS1
0005:FFFFh 0004:0000h	SA8 (64KB)	SA9 (64KB)	ROMS0

	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]	
32bit read	dat[31:0]				dat[31:0]			
64bit read	dat[63:0]							

Legend	Memory not available in this area	Memory available in this area

9.3.1.3 Flash Memory Map MB91F465BB

Addr			
0014:FFFFh 0014:C000h	SA6 (8KB)	SA7 (8KB)	ROMS7
0014:BFFFh 0014:8000h	SA4 (8KB)	SA5 (8KB)	
0014:7FFFh 0014:4000h	SA2 (8KB)	SA3 (8KB)	
0014:3FFFh 0014:0000h	SA0 (8KB)	SA1 (8KB)	
0013:FFFFh 0012:0000h	SA22 (64KB)	SA23 (64KB)	ROMS6
0011:FFFFh 0010:0000h	SA20 (64KB)	SA21 (64KB)	
000F:FFFFh 000E:0000h	SA18 (64KB)	SA19 (64KB)	ROMS5
000D:FFFFh 000C:0000h	SA16 (64KB)	SA17 (64KB)	ROMS4
000B:FFFFh 000A:0000h	SA14 (64KB)	SA15 (64KB)	ROMS3
0009:FFFFh 0008:0000h	SA12 (64KB)	SA13 (64KB)	ROMS2
0007:FFFFh 0006:0000h	SA10 (64KB)	SA11 (64KB)	ROMS1
0005:FFFFh 0004:0000h	SA8 (64KB)	SA9 (64KB)	ROMS0

	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]	
32bit read	dat[31:0]				dat[31:0]			

Legend	Memory not available in this area	Memory available in this area

9.3.1.4 Flash Memory Map MB91F464BB

Address			
0014:FFFFh 0014:C000h	SA6 (8KB)	SA7 (8KB)	ROMS7
0014:BFFFh 0014:8000h	SA4 (8KB)	SA5 (8KB)	
0014:7FFFh 0014:4000h	SA2 (8KB)	SA3 (8KB)	
0014:3FFFh 0014:0000h	SA0 (8KB)	SA1 (8KB)	
0013:FFFFh 0012:0000h	SA22 (64KB)	SA23 (64KB)	ROMS6
0011:FFFFh 0010:0000h	SA20 (64KB)	SA21 (64KB)	
000F:FFFFh 000E:0000h	SA18 (64KB)	SA19 (64KB)	ROMS5
000D:FFFFh 000C:0000h	SA16 (64KB)	SA17 (64KB)	ROMS4
000B:FFFFh 000A:0000h	SA14 (64KB)	SA15 (64KB)	ROMS3
0009:FFFFh 0008:0000h	SA12 (64KB)	SA13 (64KB)	ROMS2
0007:FFFFh 0006:0000h	SA10 (64KB)	SA11 (64KB)	ROMS1
0005:FFFFh 0004:0000h	SA8 (64KB)	SA9 (64KB)	ROMS0

	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]	
32bit read	dat[31:0]				dat[31:0]			

Legend	Memory not available in this area	Memory available in this area

9.3.2 Flash Access Timing Settings in CPU mode

The following tables list all settings for a given maximum Core Frequency (through the setting of CLKB or maximum clock modulation) for Flash read and write access.

9.3.2.1 Flash Read Timing Settings (Synchronous Read)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 24 MHz	0	0	0	-	1	
to 48 MHz	0	0	1	-	2	
to 96 MHz	1	1	3	-	4	
to 100 MHz	1	1	3	-	4	not available on MB91F467BA/MB91F466BA

9.3.2.2 Flash Write Timing Settings (Synchronous Write)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 16 MHz	0	-	-	0	3	
to 32 MHz	0	-	-	0	4	
to 48 MHz	0	-	-	0	5	
to 64 MHz	1	-	-	0	6	
to 96 MHz	1	-	-	0	7	
to 100 MHz	1	-	-	0	7	not available on MB91F467BA/MB91F466BA

9.3.3 Address Mapping from CPU to Parallel Programming Mode

The following tables show the calculation from CPU addresses to flash macro addresses which are used in parallel programming.

9.3.3.1 Address Mapping MB91F467BA

CPU Address (addr)	Condition	Flash sectors	FA (Flash address) Calculation
14:0000h to 14:FFFFh	addr[2]==0	SA0, SA2, SA4, SA6 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 - (addr/2)%4 + addr%4 - 05:0000h
14:0000h to 14:FFFFh	addr[2]==1	SA1, SA3, SA5, SA7 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 + 00:2000h - (addr/2)%4 + addr%4 - 05:0000h
04:0000h to 13:FFFFh	addr[2]==0	SA8, SA10, SA12, SA14, SA16, SA18, SA20, SA22 (64 Kbyte)	FA := addr - addr%02:0000 + (addr%02:0000h)/2 - (addr/2)%4 + addr%4 + 0C:0000h
04:0000h to 13:FFFFh	addr[2]==1	SA9, SA11, SA13, SA15, SA17, SA19, SA21, SA23 (64 Kbyte)	FA := addr - addr%02:0000h + (addr%02:0000h)/2 + 01:0000h - (addr/2)%4 + addr%4 + 0C:0000h

Note: FA result is without 20:0000h offset for parallel Flash programming . Set offset by keeping FA[21] = 1 as described in section "Parallel Flash programming mode".

9.3.3.2 Address Mapping MB91F466BA

CPU Address (addr)	Condition	Flash sectors	FA (Flash address) Calculation
14:0000h to 14:FFFFh	addr[2]==0	SA0, SA2, SA4, SA6 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 - (addr/2)%4 + addr%4 - 05:0000h
14:0000h to 14:FFFFh	addr[2]==1	SA1, SA3, SA5, SA7 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 + 00:2000h - (addr/2)%4 + addr%4 - 05:0000h
04:0000h to 0F:FFFFh	addr[2]==0	SA8, SA10, SA12, SA14, SA16, SA18 (64 Kbyte)	FA := addr - addr%02:0000 + (addr%02:0000h)/2 - (addr/2)%4 + addr%4 + 0C:0000h
04:0000h to 0F:FFFFh	addr[2]==1	SA9, SA11, SA13, SA15, SA17, SA19 (64 Kbyte)	FA := addr - addr%02:0000h + (addr%02:0000h)/2 + 01:0000h - (addr/2)%4 + addr%4 + 0C:0000h

Note: FA result is without 20:0000h offset for parallel Flash programming . Set offset by keeping FA[21] = 1 as described in section "Parallel Flash programming mode".

9.3.3.3   Address Mapping MB91F465BB

CPU Address (addr)	Condition	Flash sectors	FA (Flash address) Calculation
14:8000h to 14:FFFFh	addr[2]==0	SA4, SA6 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 - (addr/2)%4 + addr%4 - 0D:0000h
14:8000h to 14:FFFFh	addr[2]==1	SA5, SA7 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 + 00:2000h - (addr/2)%4 + addr%4 - 0D:0000h
08:0000h to 0F:FFFFh	addr[2]==0	SA12, SA14, SA16, SA18 (64 Kbyte)	FA := addr - addr%02:0000 + (addr%02:0000h)/2 - (addr/2)%4 + addr%4
08:0000h to 0F:FFFFh	addr[2]==1	SA13, SA15, SA17, SA19 (64 Kbyte)	FA := addr - addr%02:0000h + (addr%02:0000h)/2 + 01:0000h - (addr/2)%4 + addr%4

Note: FA result is without 20:0000h offset for parallel Flash programming . Set offset by keeping FA[21] = 1 as described in section "Parallel Flash programming mode".

9.3.3.4   Address Mapping MB91F464BB

CPU Address (addr)	Condition	Flash sectors	FA (Flash address) Calculation
14:8000h to 14:FFFFh	addr[2]==0	SA4, SA6 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 - (addr/2)%4 + addr%4 - 0D:0000h
14:8000h to 14:FFFFh	addr[2]==1	SA5, SA7 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 + 00:2000h - (addr/2)%4 + addr%4 - 0D:0000h
0A:0000h to 0F:FFFFh	addr[2]==0	SA14, SA16, SA18 (64 Kbyte)	FA := addr - addr%02:0000 + (addr%02:0000h)/2 - (addr/2)%4 + addr%4
0A:0000h to 0F:FFFFh	addr[2]==1	SA15, SA17, SA19 (64 Kbyte)	FA := addr - addr%02:0000h + (addr%02:0000h)/2 + 01:0000h - (addr/2)%4 + addr%4

Note: FA result is without 20:0000h offset for parallel Flash programming . Set offset by keeping FA[21] = 1 as described in section "Parallel Flash programming mode".

9.4   Parallel Flash Programming Mode

9.4.1   Flash Configuration in Parallel Flash Programming Mode

9.4.1.1   Parallel Flash programming mode (MD[2:0] = 111):

MB91F467BA

FA[21:0]

Address	Sector
003F:FFFFh / 003F:0000h	SA23 (64KB)
003E:FFFFh / 003E:0000h	SA22 (64KB)
003D:FFFFh / 003D:0000h	SA21 (64KB)
003C:FFFFh / 003C:0000h	SA20 (64KB)
003B:FFFFh / 003B:0000h	SA19 (64KB)
003A:FFFFh / 003A:0000h	SA18 (64KB)
0039:FFFFh / 0039:0000h	SA17 (64KB)
0038:FFFFh / 0038:0000h	SA16 (64KB)
0037:FFFFh / 0037:0000h	SA15 (64KB)
0036:FFFFh / 0036:0000h	SA14 (64KB)
0035:FFFFh / 0035:0000h	SA13 (64KB)
0034:FFFFh / 0034:0000h	SA12 (64KB)
0033:FFFFh / 0033:0000h	SA11 (64KB)
0032:FFFFh / 0032:0000h	SA10 (64KB)
0031:FFFFh / 0031:0000h	SA9 (64KB)
0030:FFFFh / 0030:0000h	SA8 (64KB)
002F:FFFFh / 002F:E000h	SA7 (8KB)
002F:DFFFh / 002F:C000h	SA6 (8KB)
002F:BFFFh / 002F:A000h	SA5 (8KB)
002F:9FFFh / 002F:8000h	SA4 (8KB)
002F:7FFFh / 002F:6000h	SA3 (8KB)
002F:5FFFh / 002F:4000h	SA2 (8KB)
002F:3FFFh / 002F:2000h	SA1 (8KB)
002F:1FFFh / 002F:0000h	SA0 (8KB)

	FA[1:0]=00	FA[1:0]=10
16bit write mode	DQ[15:0]	DQ[15:0]

MB91F466BA

FA[21:0]

Address	Sector
	SA23 (64KB)
	SA22 (64KB)
	SA21 (64KB)
	SA20 (64KB)
003B:FFFFh / 003B:0000h	SA19 (64KB)
003A:FFFFh / 003A:0000h	SA18 (64KB)
0039:FFFFh / 0039:0000h	SA17 (64KB)
0038:FFFFh / 0038:0000h	SA16 (64KB)
0037:FFFFh / 0037:0000h	SA15 (64KB)
0036:FFFFh / 0036:0000h	SA14 (64KB)
0035:FFFFh / 0035:0000h	SA13 (64KB)
0034:FFFFh / 0034:0000h	SA12 (64KB)
0033:FFFFh / 0033:0000h	SA11 (64KB)
0032:FFFFh / 0032:0000h	SA10 (64KB)
0031:FFFFh / 0031:0000h	SA9 (64KB)
0030:FFFFh / 0030:0000h	SA8 (64KB)
002F:FFFFh / 002F:E000h	SA7 (8KB)
002F:DFFFh / 002F:C000h	SA6 (8KB)
002F:BFFFh / 002F:A000h	SA5 (8KB)
002F:9FFFh / 002F:8000h	SA4 (8KB)
002F:7FFFh / 002F:6000h	SA3 (8KB)
002F:5FFFh / 002F:4000h	SA2 (8KB)
002F:3FFFh / 002F:2000h	SA1 (8KB)
002F:1FFFh / 002F:0000h	SA0 (8KB)

	FA[1:0]=00	FA[1:0]=10
16bit write mode	DQ[15:0]	DQ[15:0]

Remark: Always keep FA[0] = 0 and FA[21] = 1

MB91F465BB

FA[20:0]

Address	Block
001F:FFFFh 001F:0000h	SA19 (64KB)
001E:FFFFh 001E:0000h	SA18 (64KB)
001D:FFFFh 001D:0000h	SA17 (64KB)
001C:FFFFh 001C:0000h	SA16 (64KB)
001B:FFFFh 001B:0000h	SA15 (64KB)
001A:FFFFh 001A:0000h	SA14 (64KB)
0019:FFFFh 0019:0000h	SA13 (64KB)
0018:FFFFh 0018:0000h	SA12 (64KB)
	SA11 (64KB)
	SA10 (64KB)
	SA9 (64KB)
	SA8 (64KB)
0017:FFFFh 0017:E000h	SA7 (8KB)
0017:DFFFh 0017:C000h	SA6 (8KB)
0017:BFFFh 0017:A000h	SA5 (8KB)
0017:9FFFh 0017:8000h	SA4 (8KB)
	SA3 (8KB)
	SA2 (8KB)
	SA1 (8KB)
	SA0 (8KB)

FA[1:0]=00	FA[1:0]=10
DQ[15:0]	DQ[15:0]

16bit write mode

Remark: Always keep FA[0] = 0 and FA[20] = 1

Legend

Memory available in this area
Memory not available in this area

MB91F464BB

FA[20:0]

Address	Block
001F:FFFFh 001F:0000h	SA19 (64KB)
001E:FFFFh 001E:0000h	SA18 (64KB)
001D:FFFFh 001D:0000h	SA17 (64KB)
001C:FFFFh 001C:0000h	SA16 (64KB)
001B:FFFFh 001B:0000h	SA15 (64KB)
001A:FFFFh 001A:0000h	SA14 (64KB)
	SA13 (64KB)
	SA12 (64KB)
	SA11 (64KB)
	SA10 (64KB)
	SA9 (64KB)
	SA8 (64KB)
0017:FFFFh 0017:E000h	SA7 (8KB)
0017:DFFFh 0017:C000h	SA6 (8KB)
0017:BFFFh 0017:A000h	SA5 (8KB)
0017:9FFFh 0017:8000h	SA4 (8KB)
	SA3 (8KB)
	SA2 (8KB)
	SA1 (8KB)
	SA0 (8KB)

FA[1:0]=00	FA[1:0]=10
DQ[15:0]	DQ[15:0]

16bit write mode

Remark: Always keep FA[0] = 0 and FA[20] = 1

Legend

Memory available in this area
Memory not available in this area

9.4.2   Pin Connections in Parallel Programming Mode

Resetting after setting the MD[2:0] pins to [111] will halt CPU functioning. At this time, the Flash memory's interface circuit enables direct control of the Flash memory unit from external pins by directly linking some of the signals to GP-Ports. Please see table below for signal mapping.

In this mode, the Flash memory appears to the external pins as a stand-alone unit. This mode is generally set when writing/erasing using the parallel Flash programmer. In this mode, all operations of the 8.5 Mbits Flash memory's Auto Algorithms are available.

Table 1. Correspondence between MBM29LV400TC and Flash Memory Control Signals

MBM29LV400TCE xternal pins	FR-CPU mode	MB91F467BA/466BA/F465BB/F464BB External Pins			Comment
		Flash memory mode	Normal function	Pin number	
-	INITX	-	INITX	84	
RESET	-	FRSTX	GP16_6	70	
-	-	MD2	MD2	76	Set to '1'
-	-	MD1	MD1	75	Set to '1'
-	-	MD0	MD0	74	Set to '1'
RY/BY	FMCS:RDY bit	RY/BYX	GP18_2	100	
BYTE	Internally fixed to 'H'	BYTEX	GP16_4	68	
WE	Internal control signal + control via interface circuit	WEX	GP16_7	71	
OE		OEX	GP07_7	3	
CE		CEX	GP07_6	2	
-		ATDIN	GP18_6	103	Set to '0'
-		EQIN	GP18_5	102	Set to '0'
-		TESTX	GP16_5	69	Set to '1'
-		RDYI	GP18_4	101	Set to '0'
A-1	Internal address bus	FA0	GP05_5	17	Set to '0'
A0 to A3		FA1 to FA4	GP19_0 to GP19_2, GP19_4	92 to 95	
A4 to A7		FA5 to FA8	GP19_5 to GP19_6, GP18_0 to GP18_1	96 to 99	
A8 to A11		FA9 to FA12	GP06_0 to GP06_3	4 to 7	
A12 to A15		FA13 to FA16	GP06_4 to GP06_7	8 to 11	
A16 to A18		FA17 to FA19	GP05_0 to GP05_2	12 to 14	
A19		FA20	GP05_3	15	See note [1]
-		FA21	GP05_4	16	See note [2]
DQ0 to DQ7	Internal data bus	DQ0 to DQ7	GP00_0 to GP00_7	28 to 35	
DQ8 to DQ15		DQ8 to DQ15	GP01_0 to GP01_7	20 to 27	

1.   A19 is used as address bit on MB91F467BA/F466BA. For MB91F465BB/F464BB, set this pin to '1'.
2.   For MB91F467BA/F466BA, set this pin to '1'. For MB91F465BB/F464BB, this pin can be left open.

9.5   Poweron Sequence in Parallel Programming Mode

The flash memory can be accessed in programming mode after a certain wait time, which is needed for Security Vector fetch:

■ Minimum wait time after VDD5/VDD5R power on: 2.76 ms

■ Minimum wait time after INITX rising: 1.0 ms

9.6   Flash Security

9.6.1   Vector Addresses

Two Flash Security Vectors (FSV1, FSV2) are located parallel to the Boot Security Vectors (BSV1, BSV2) controlling the protection functions of the Flash Security Module:

FSV1: 0x14:8000   BSV1: 0x14:8004
FSV2: 0x14:8008   BSV2: 0x14:800C

9.6.2   Security Vector FSV1

The setting of the Flash Security Vector FSV1 is responsible for the read and write protection modes and the individual write protection of the 8 KBytes sectors.

9.6.2.1   FSV1 (bit31 to bit16)

The setting of the Flash Security Vector FSV1 bits [31:16] is responsible for the read and write protection modes.

Table 2. Explanation of the bits in the Flash Security Vector FSV1[31:16]

FSV1[31:19]	FSV1[18] Write Protection Level	FSV1[17] Write Protection	FSV1[16] Read Protection	Flash Security Mode
set all to '0'	set to '0'	set to '0'	set to '1'	Read Protection (all device modes, except INTVEC mode MD[2:0]="000")
set all to '0'	set to '0'	set to '1'	set to '0'	Write Protection (all device modes, without exception)
set all to '0'	set to '0'	set to '1'	set to '1'	Read Protection (all device modes, except INTVEC mode MD[2:0]="000") and Write Protection (all device modes)
set all to '0'	set to '1'	set to '0'	set to '1'	Read Protection (all device modes, except INTVEC mode MD[2:0]="000")
set all to '0'	set to '1'	set to '1'	set to '0'	Write Protection (all device modes, except INTVEC mode MD[2:0]="000")
set all to '0'	set to '1'	set to '1'	set to '1'	Read Protection (all device modes, except INTVEC mode MD[2:0]="000") and Write Protection (all device modes except INTVEC mode MD[2:0]="000")

9.6.2.2 FSV1 (bit15 to bit0) MB91F467BA/466BA

The setting of the Flash Security Vector FSV1 bits [15:0] is responsible for the individual write protection of the 8 KBytes sectors. It is only evaluated if write protection bit FSV1[17] is set.

Table 3. Explanation of the bits in the Flash Security Vector FSV1[15:0]

FSV1 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV1[0]	SA0	set to "0"	set to "1"	
FSV1[1]	SA1	set to "0"	set to "1"	
FSV1[2]	SA2	set to "0"	set to "1"	
FSV1[3]	SA3	set to "0"	set to "1"	
FSV1[4]	SA4	set to "0"	–	Write protection is manda-tory!
FSV1[5]	SA5	set to "0"	set to "1"	
FSV1[6]	SA6	set to "0"	set to "1"	
FSV1[7]	SA7	set to "0"	set to "1"	
FSV1[15:8]	–	–	–	not available

Note: It is mandatory to always set the sector where the Flash Security Vectors FSV1 and FSV2 are located to write protected (here sector SA4). Otherwise it is possible to overwrite the Security Vector to a setting where it is possible to either read out the Flash content or manipulate data by writing. See section "Flash access in CPU mode" for an overview about the sector organisation of the Flash Memory.

9.6.2.3 FSV1 (bit15 to bit0) MB91F465BB/464BB

The setting of the Flash Security Vector FSV1 bits [15:0] is responsible for the individual write protection of the 8 KBytes sectors. It is only evaluated if write protection bit FSV1[17] is set.

Table 4. Explanation of the bits in the Flash Security Vector FSV1[15:0]

FSV1 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV1[3:0]	–	–	–	not available
FSV1[4]	SA4	set to "0"	—	Write protection is manda-tory!
FSV1[5]	SA5	set to "0"	set to "1"	
FSV1[6]	SA6	set to "0"	set to "1"	
FSV1[7]	SA7	set to "0"	set to "1"	
FSV1[15:8]	–	–	–	not available

Note: It is mandatory to always set the sector where the Flash Security Vectors FSV1 and FSV2 are located to write protected (here sector SA4). Otherwise it is possible to overwrite the Security Vector to a setting where it is possible to either read out the Flash content or manipulate data by writing. See section "Flash access in CPU mode" for an overview about the sector organisation of the Flash Memory.

9.6.3   Security Vector FSV2 MB91F467BA/466BA

The setting of the Flash Security Vector FSV2 bits [31:0] is responsible for the individual write protection of the 64 KByte sectors. It is only evaluated if write protection bit FSV1[17] is set.

Table 5. Explanation of the bits in the Flash Security Vector FSV2[31:0]

FSV2 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV2[0]	SA8	set to "0"	set to "1"	
FSV2[1]	SA9	set to "0"	set to "1"	
FSV2[2]	SA10	set to "0"	set to "1"	
FSV2[3]	SA11	set to "0"	set to "1"	
FSV2[4]	SA12	set to "0"	set to "1"	
FSV2[5]	SA13	set to "0"	set to "1"	
FSV2[6]	SA14	set to "0"	set to "1"	
FSV2[7]	SA15	set to "0"	set to "1"	
FSV2[8]	SA16	set to "0"	set to "1"	
FSV2[9]	SA17	set to "0"	set to "1"	
FSV2[10]	SA18	set to "0"	set to "1"	
FSV2[11]	SA19	set to "0"	set to "1"	
FSV2[12]	SA20 (MB91F467BA)	set to "0"	set to "1"	
FSV2[13]	SA21 (MB91F467BA)	set to "0"	set to "1"	
FSV2[14]	SA22 (MB91F467BA)	set to "0"	set to "1"	
FSV2[15]	SA23 (MB91F467BA)	set to "0"	set to "1"	
FSV2[31:16]	–	set to "0"	set to "1"	not available

Note: See section "Flash access in CPU mode" for an overview about the sector organisation of the Flash Memory.

9.6.4   Security Vector FSV2 MB91F465BB/464BB

The setting of the Flash Security Vector FSV2 bits [31:0] is responsible for the individual write protection of the 64 KByte sectors. It is only evaluated if write protection bit FSV1[17] is set.

Table 6. Explanation of the bits in the Flash Security Vector FSV2[31:0]

FSV2 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV2[3:0]	–	–	–	not available
FSV2[4]	SA12 (MB91F465BB)	set to "0"	set to "1"	
FSV2[5]	SA13 (MB91F465BB)	set to "0"	set to "1"	
FSV2[6]	SA14	set to "0"	set to "1"	
FSV2[7]	SA15	set to "0"	set to "1"	
FSV2[8]	SA16	set to "0"	set to "1"	
FSV2[9]	SA17	set to "0"	set to "1"	
FSV2[10]	SA18	set to "0"	set to "1"	
FSV2[11]	SA19	set to "0"	set to "1"	
FSV2[31:12]	–	–	–	not available

Note: See section "Flash access in CPU mode" for an overview about the sector organisation of the Flash Memory.

10. Memory Space

The FR family has 4 Gbytes of logical address space (2^{32} addresses) available to the CPU by linear access.

■ Direct addressing area
The following address space area is used for I/O.

This area is called direct addressing area, and the address of an operand can be specified directly in an instruction.

The size of directly addressable area depends on the length of the data being accessed as shown below.

Byte data access: 000_H to $0FF_H$

Half word access: 000_H to $1FF_H$

Word data access: 000_H to $3FF_H$

11. Memory Maps

11.1 MB91F467BA, MB91F466BA

MB91F467BA

00000000H	I/O (direct addressing area)
00000400H	I/O
00001000H	DMA
00002000H	
00004000H	Flash-Cache (8 KBytes)
00006000H	
00007000H	Flash memory control
00008000H	
0000B000H	Boot ROM (4 Kbytes)
0000C000H	CAN
0000D000H	
0002A000H	D-RAM (0 wait, 24 Kbytes)
00030000H	ID-RAM (16 Kbytes)
00034000H	
00040000H	Flash memory (1088 Kbytes)
00150000H	
00180000H	External bus area
00500000H	External data bus
FFFFFFFFH	

MB91F466BA

00000000H	I/O (direct addressing area)
00000400H	I/O
00001000H	DMA
00002000H	
00004000H	Flash-Cache (8 KBytes)
00006000H	
00007000H	Flash memory control
00008000H	
0000B000H	Boot ROM (4 Kbytes)
0000C000H	CAN
0000D000H	
0002A000H	D-RAM (0 wait, 24 Kbytes)
00030000H	ID-RAM (16 Kbytes)
00034000H	
00040000H	External bus area
00080000H	Flash memory (768 Kbytes)
00100000H	
00140000H	Flash memory (64 Kbytes)
00150000H	
00180000H	External bus area
00500000H	External data bus
FFFFFFFFH	

Note: [Access prohibited areas]

Note: [Access prohibited areas]

11.2   MB91F465BB, MB91F464BB

MB91F465BB

Address	Region
00000000H	I/O (direct addressing area)
00000400H	I/O
00001000H	DMA
00002000H	
00004000H	Flash-Cache (8 KBytes)
00006000H	
00007000H	Flash memory control
00008000H	
0000B000H	Boot ROM (4 Kbytes)
0000C000H	CAN
0000D000H	
0002A000H	D-RAM (0 wait, 24 Kbytes)
00030000H	ID-RAM (16 Kbytes)
00034000H	
00040000H	External bus area
00080000H	Flash memory (512 Kbytes)
00100000H	External bus area
00148000H	Flash memory (32 Kbytes)
00150000H	
00180000H	External bus area
00500000H	External data bus
FFFFFFFFH	

MB91F464BB

Address	Region
00000000H	I/O (direct addressing area)
00000400H	I/O
00001000H	DMA
00002000H	
00004000H	Flash-Cache (8 KBytes)
00006000H	
00007000H	Flash memory control
00008000H	
0000B000H	Boot ROM (4 Kbytes)
0000C000H	CAN
0000D000H	
0002A000H	D-RAM (0 wait, 24 Kbytes)
00030000H	ID-RAM (16 Kbytes)
00034000H	
00040000H	External bus area
00080000H	
000A0000H	Flash memory (384 Kbytes)
00100000H	External bus area
00148000H	Flash memory (32 Kbytes)
00150000H	
00180000H	External bus area
00500000H	External data bus
FFFFFFFFH	

Note: Access prohibited areas

12. I/O Map

12.1 MB91F467BA/466BA, MB91F465BB/464BB

Address	Register				Block
	+ 0	**+ 1**	**+ 2**	**+ 3**	**Block**
000000$_H$	PDR0 [R/W] XXXXXXXX	PDR1 [R/W] XXXXXXXX	PDR2 [R/W] XXXXXXXX	PDR3 [R/W] XXXXXXXX	T-unit port data register

Read/write attribute

Register initial value after reset

Register name (column 1 register at address 4n, column 2 register at address 4n + 1...)

Leftmost register address (for word access, the register in column 1 becomes the MSB side of the data.)
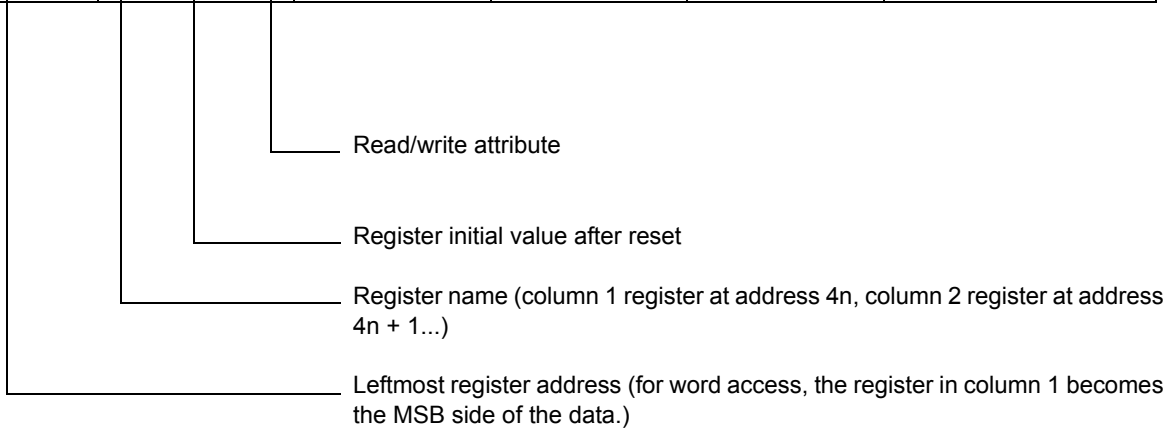
Note: Initial values of register bits are represented as follows:
" 1 ": Initial value " 1 "
" 0 ": Initial value " 0 "
" X ": Initial value " undefined "
" - ": No physical register at this location
Access is barred with an undefined data access attribute.

Address	Register				Block
	+0	**+1**	**+2**	**+3**	
000000$_H$	PDR00 [R/W] XXXXXXXX	PDR01 [R/W] XXXXXXXX	Reserved	Reserved	R-bus Port Data Register
000004$_H$	Reserved	PDR05 [R/W] - - XXXXXX	PDR06 [R/W] XXXXXXXX	PDR07 [R/W] XXXXXXXX	
000008$_H$	PDR08 [R/W] X - - X - - - X	PDR09 [R/W] - - - - - - XX	PDR10 [R/W] - - - - - - - X	Reserved	
00000C$_H$	Reserved	Reserved	PDR14 [R/W] XXXXXXXX	PDR15 [R/W] XXXXXXXX	
000010$_H$	PDR16 [R/W] XXXXXXXX	PDR17 [R/W] XXXXXXXX	PDR18 [R/W] - XXX - XXX	PDR19 [R/W] - XXX - XXX	
000014$_H$	PDR20 [R/W] - XXX - XXX	PDR21 [R/W] - - - - - - XX	PDR22 [R/W] XXXXXXXX	PDR23 [R/W] XXXXXXXX	
000018$_H$	PDR24 [R/W] XXXXXXXX	Reserved	PDR26 [R/W] XXXXXXXX	PDR27 [R/W] XXXXXXXX	
00001C$_H$	PDR28 [R/W] XXXXXXXX	PDR29 [R/W] XXXXXXXX	Reserved	Reserved	
000020$_H$ to 00002C$_H$	Reserved				
000030$_H$	EIRR0 [R/W] MB91F467BA: 00000000:MD3=0 11110000:MD3=1 MB91F465BB: XXXXXXXX	ENIR0 [R/W] 00000000	ELVR0 [R/W] 00000000 00000000		External interrupt (INT 0 to INT 7)
000034$_H$	EIRR1 [R/W] MB91F467BA: 00000000 MB91F465BB: XXXXXXXX	ENIR1 [R/W] 00000000	ELVR1 [R/W] 00000000 00000000		External interrupt (INT 8 to INT 15)
000038$_H$	DICR [R/W] - - - - - - - 0	HRCL [R/W] 0 - - 11111	RBSYNC		Delay interrupt
00003C$_H$	Reserved				Reserved
000040$_H$	SCR00 [R/W,W] 00000000	SMR00 [R/W,W] 00000000	SSR00 [R/W,R] 00001000	RDR00/TDR00 [R/W] 00000000	LIN-USART 0
000044$_H$	ESCR00 [R/W] 00000X00	ECCR00 [R/W,R,W] -00000XX	Reserved		
000048$_H$ 00004C$_H$	Reserved				Reserved
000050$_H$	SCR02 [R/W,W] 00000000	SMR02 [R/W,W] 00000000	SSR02 [R/W,R] 00001000	RDR02/TDR02 [R/W] 00000000	LIN-USART 2
000054$_H$	ESCR02 [R/W] 00000X00	ECCR02 [R/W,R,W] -00000XX	Reserved		

Address	Register				Block
	+0	+1	+2	+3	
000058H	SCR03 [R/W,W] 00000000	SMR03 [R/W,W] 00000000	SSR03 [R/W,R] 00001000	RDR03/TDR03 [R/W] 00000000	LIN-USART 3
00005CH	ESCR03 [R/W] 00000X00	ECCR03 [R/W,R,W] -00000XX	Reserved		
000060H	SCR04 [R/W,W] 00000000	SMR04 [R/W,W] 00000000	SSR04 [R/W,R] 00001000	RDR04/TDR04 [R/W] 00000000	LIN-USART 4 with FIFO
000064H	ESCR04 [R/W] 00000X00	ECCR04 [R/W,R,W] -00000XX	FSR04 [R] - - - 00000	FCR04 [R/W] 0001 - 000	
000068H	SCR05 [R/W,W] 00000000	SMR05 [R/W,W] 00000000	SSR05 [R/W,R] 00001000	RDR05/TDR05 [R/W] 00000000	LIN-USART 5 with FIFO
00006CH	ESCR05 [R/W] 00000X00	ECCR05 [R/W,R,W] -00000XX	FSR05 [R] - - - 00000	FCR05 [R/W] 0001 - 000	
000070H	SCR06 [R/W,W] 00000000	SMR06 [R/W,W] 00000000	SSR06 [R/W,R] 00001000	RDR06/TDR06 [R/W] 00000000	LIN-USART 6 with FIFO
000074H	ESCR06 [R/W] 00000X00	ECCR06 [R/W,R,W] -00000XX	FSR06 [R] - - - 00000	FCR06 [R/W] 0001 - 000	
000078H	SCR07 [R/W,W] 00000000	SMR07 [R/W,W] 00000000	SSR07 [R/W,R] 00001000	RDR07/TDR07 [R/W] 00000000	LIN-USART 7 with FIFO
00007CH	ESCR07 [R/W] 00000X00	ECCR07 [R/W,R,W] -00000XX	FSR07 [R] - - - 00000	FCR07 [R/W] 0001 - 000	
000080H	BGR100 [R/W] 00000000	BGR000 [R/W] 00000000	Reserved	Reserved	Baud rate Generator LIN-USART 0 to 7
000084H	BGR102 [R/W] 00000000	BGR002 [R/W] 00000000	BGR103 [R/W] 00000000	BGR003 [R/W] 00000000	
000088H	BGR104 [R/W] 00000000	BGR004 [R/W] 00000000	BGR105 [R/W] 00000000	BGR005 [R/W] 00000000	
00008CH	BGR106 [R/W] 00000000	BGR006 [R/W] 00000000	BGR107 [R/W] 00000000	BGR007 [R/W] 00000000	
000090H to 0000CCH	Reserved				Reserved
0000D0H	IBCR0 [R/W] 00000000	IBSR0 [R] 00000000	ITBAH0 [R/W] - - - - - - 00	ITBAL0 [R/W] 00000000	I^2C 0
0000D4H	ITMKH0 [R/W] 00 - - - - 11	ITMKL0 [R/W] 11111111	ISMK0 [R/W] 01111111	ISBA0 [R/W] - 0000000	
0000D8H	Reserved	IDAR0 [R/W] 00000000	ICCR0 [R/W] - 0011111	Reserved	
0000DCH	IBCR1 [R/W] 00000000	IBSR1 [R] 00000000	ITBAH1 [R/W] - - - - - - 00	ITBAL1 [R/W] 00000000	I^2C 1
0000E0H	ITMKH1 [R/W] 00 - - - - 11	ITMKL1 [R/W] 11111111	ISMK1 [R/W] 01111111	ISBA1 [R/W] - 0000000	
0000E4H	Reserved	IDAR1 [R/W] 00000000	ICCR1 [R/W] - 0011111	Reserved	

Address	Register				Block
	+0	**+1**	**+2**	**+3**	
0000E8_H to 0000FC_H	Reserved				Reserved
000100_H	GCN10 [R/W] 00110010 00010000		Reserved	GCN20 [R/W] - - - - 0000	PPG Control 0 to 3
000104_H	GCN11 [R/W] 00110010 00010000		Reserved	GCN21 [R/W] - - - - 0000	PPG Control 4 to 7
000108_H	GCN12 [R/W] 00110010 00010000		Reserved	GCN22 [R/W] - - - - 0000	PPG Control 8 to 11
000110_H	PTMR00 [R] 11111111 11111111		PCSR00 [W] XXXXXXXX XXXXXXXX		PPG 0
000114_H	PDUT00 [W] XXXXXXXX XXXXXXXX		PCNH00 [R/W] 0000000 -	PCNL00 [R/W] 000000 - 0	
000118_H	PTMR01 [R] 11111111 11111111		PCSR01 [W] XXXXXXXX XXXXXXXX		PPG 1
00011C_H	PDUT01 [W] XXXXXXXX XXXXXXXX		PCNH01 [R/W] 0000000 -	PCNL01 [R/W] 000000 - 0	
000120_H	PTMR02 [R] 11111111 11111111		PCSR02 [W] XXXXXXXX XXXXXXXX		PPG 2
000124_H	PDUT02 [W] XXXXXXXX XXXXXXXX		PCNH02 [R/W] 0000000 -	PCNL02 [R/W] 000000 - 0	
000128_H	PTMR03 [R] 11111111 11111111		PCSR03 [W] XXXXXXXX XXXXXXXX		PPG 3
00012C_H	PDUT03 [W] XXXXXXXX XXXXXXXX		PCNH03 [R/W] 0000000 -	PCNL03 [R/W] 000000 - 0	
000130_H	PTMR04 [R] 11111111 11111111		PCSR04 [W] XXXXXXXX XXXXXXXX		PPG 4
000134_H	PDUT04 [W] XXXXXXXX XXXXXXXX		PCNH04 [R/W] 0000000 -	PCNL04 [R/W] 000000 - 0	
000138_H	PTMR05 [R] 11111111 11111111		PCSR05 [W] XXXXXXXX XXXXXXXX		PPG 5
00013C_H	PDUT05 [W] XXXXXXXX XXXXXXXX		PCNH05 [R/W] 0000000 -	PCNL05 [R/W] 000000 - 0	
000140_H	PTMR06 [R] 11111111 11111111		PCSR06 [W] XXXXXXXX XXXXXXXX		PPG 6
000144_H	PDUT06 [W] XXXXXXXX XXXXXXXX		PCNH06 [R/W] 0000000 -	PCNL06 [R/W] 000000 - 0	
000148_H	PTMR07 [R] 11111111 11111111		PCSR07 [W] XXXXXXXX XXXXXXXX		PPG 7
00014C_H	PDUT07 [W] XXXXXXXX XXXXXXXX		PCNH07 [R/W] 0000000 -	PCNL07 [R/W] 000000 - 0	
000150_H	PTMR08 [R] 11111111 11111111		PCSR08 [W] XXXXXXXX XXXXXXXX		PPG 8
000154_H	PDUT08 [W] XXXXXXXX XXXXXXXX		PCNH08 [R/W] 0000000 -	PCNL08 [R/W] 000000 - 0	

Address	Register				Block
	+0	+1	+2	+3	
000158$_H$	PTMR09 [R] 11111111 11111111		PCSR09 [W] XXXXXXXX XXXXXXXX		PPG 9
00015C$_H$	PDUT09 [W] XXXXXXXX XXXXXXXX		PCNH09 [R/W] 0000000 -	PCNL09 [R/W] 000000 - 0	
000160$_H$	PTMR10 [R] 11111111 11111111		PCSR10 [W] XXXXXXXX XXXXXXXX		PPG 10
000164$_H$	PDUT10 [W] XXXXXXXX XXXXXXXX		PCNH10 [R/W] 0000000 -	PCNL10 [R/W] 000000 - 0	
000168$_H$	PTMR11 [R] 11111111 11111111		PCSR11 [W] XXXXXXXX XXXXXXXX		PPG 11
00016C$_H$	PDUT11 [W] XXXXXXXX XXXXXXXX		PCNH11 [R/W] 0000000 -	PCNL11 [R/W] 000000 - 0	
000170$_H$ to 00017C$_H$	Reserved				Reserved
000180$_H$	Reserved	ICS01 [R/W] 00000000	Reserved	ICS23 [R/W] 00000000	Input Capture 0 to 3
000184$_H$	IPCP0 [R] XXXXXXXX XXXXXXXX		IPCP1 [R] XXXXXXXX XXXXXXXX		
000188$_H$	IPCP2 [R] XXXXXXXX XXXXXXXX		IPCP3 [R] XXXXXXXX XXXXXXXX		
00018C$_H$	OCS01 [R/W] - - - 0 - - 00 0000 - - 00		OCS23 [R/W] - - - 0 - - 00 0000 - - 00		Output Compare 0 to 3
000190$_H$	OCCP0 [R/W] XXXXXXXX XXXXXXXX		OCCP1 [R/W] XXXXXXXX XXXXXXXX		
000194$_H$	OCCP2 [R/W] XXXXXXXX XXXXXXXX		OCCP3 [R/W] XXXXXXXX XXXXXXXX		
000198$_H$	SGCRH [R/W] 0000 - - 00	SGCRL [R/W] - - 0 - - 000	SGFR [R/W, R] XXXXXXXX XXXXXXXX		Sound Generator
00019C$_H$	SGAR [R/W] 00000000	Reserved	SGTR [R/W] XXXXXXXX	SGDR [R/W] XXXXXXXX	
0001A0$_H$	ADERH [R/W] 00000000 00000000		ADERL [R/W] 00000000 00000000		A/D Converter
0001A4	ADCS1 [R/W] 00000000	ADCS0 [R/W] 00000000	ADCR1 [R] 000000XX	ADCR0 [R] XXXXXXXX	
0001A8$_H$	ADCT1 [R/W] 00010000	ADCT0 [R/W] 00101100	ADSCH [R/W] - - - 00000	ADECH [R/W] - - - 00000	
0001AC$_H$	Reserved	ACSR0 [R/W] -11XXX00	Reserved	Reserved	Alarm Comparator 0 to 1
0001B0$_H$	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0 (PPG 0, PPG 1)
0001B4$_H$	Reserved		TMCSRH0 [R/W] - - - 00000	TMCSRL0 [R/W] 0 - 000000	
0001B8$_H$	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1 (PPG 2, PPG 3)
0001BC$_H$	Reserved		TMCSRH1 [R/W] - - - 00000	TMCSRL1 [R/W] 0 - 000000	

Address	Register				Block
	+0	+1	+2	+3	
0001C0$_H$	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		Reload Timer 2 (PPG 4, PPG 5)
0001C4$_H$	Reserved		TMCSRH2 [R/W] - - - 00000	TMCSRL2 [R/W] 0 - 000000	
0001C8$_H$	TMRLR3 [W] XXXXXXXX XXXXXXXX		TMR3 [R] XXXXXXXX XXXXXXXX		Reload Timer 3 (PPG 6, PPG 7)
0001CC$_H$	Reserved		TMCSRH3 [R/W] - - - 00000	TMCSRL3 [R/W] 0 - 000000	
0001D0$_H$	TMRLR4 [W] XXXXXXXX XXXXXXXX		TMR4 [R] XXXXXXXX XXXXXXXX		Reload Timer 4 (PPG 8, PPG 9)
0001D4$_H$	Reserved		TMCSRH4 [R/W] - - - 00000	TMCSRL4 [R/W] 0 - 000000	
0001D8$_H$	TMRLR5 [W] XXXXXXXX XXXXXXXX		TMR5 [R] XXXXXXXX XXXXXXXX		Reload Timer 5 (PPG 10, PPG 11)
0001DC$_H$	Reserved		TMCSRH5 [R/W] - - - 00000	TMCSRL5 [R/W] 0 - 000000	
0001E0$_H$	TMRLR6 [W] XXXXXXXX XXXXXXXX		TMR6 [R] XXXXXXXX XXXXXXXX		Reload Timer 6 (PPG 12, PPG 13)
0001E4$_H$	Reserved		TMCSRH6 [R/W] - - - 00000	TMCSRL6 [R/W] 0 - 000000	
0001E8$_H$	TMRLR7 [W] XXXXXXXX XXXXXXXX		TMR7 [R] XXXXXXXX XXXXXXXX		Reload Timer 7 (PPG 14, PPG 15) (A/D Converter)
0001EC$_H$	Reserved		TMCSRH7 [R/W] - - - 00000	TMCSRL7 [R/W] 0 - 000000	
0001F0$_H$	TCDT0 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS0 [R/W] 00000000	Free Running Timer 0 (ICU 0, ICU 1)
0001F4$_H$	TCDT1 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS1 [R/W] 00000000	Free Running Timer 1 (ICU 2, ICU 3)
0001F8$_H$	TCDT2 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS2 [R/W] 00000000	Free Running Timer 2 (OCU 0, OCU 1)
0001FC$_H$	TCDT3 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS3 [R/W] 00000000	Free Running Timer 3 (OCU 2, OCU 3)

Address	Register				Block
	+0	**+1**	**+2**	**+3**	
000200$_H$	DMACA0　[R/W]　00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204$_H$	DMACB0　[R/W]　00000000 00000000 XXXXXXXX XXXXXXXX				
000208$_H$	DMACA1　[R/W]　00000000 0000XXXX XXXXXXXX XXXXXXXX				
00020C$_H$	DMACB1　[R/W]　00000000 00000000 XXXXXXXX XXXXXXXX				
000210$_H$	DMACA2　[R/W]　00000000 0000XXXX XXXXXXXX XXXXXXXX				
000214$_H$	DMACB2　[R/W]　00000000 00000000 XXXXXXXX XXXXXXXX				
000218$_H$	DMACA3　[R/W]　00000000 0000XXXX XXXXXXXX XXXXXXXX				
00021C$_H$	DMACB3　[R/W]　00000000 00000000 XXXXXXXX XXXXXXXX				
000220$_H$	DMACA4　[R/W]　00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000224$_H$	DMACB4　[R/W]　00000000 00000000 XXXXXXXX XXXXXXXX				
000228$_H$ to 00023C$_H$	Reserved				
000240$_H$	DMACR　[R/W]　00 - - 0000	Reserved			
000244$_H$ to 0002CC$_H$	Reserved				Reserved
0002D0$_H$	Reserved	ICS045 [R/W]　00000000	Reserved	ICS67 [R/W]　00000000	Input Capture 4 to 7
0002D4$_H$	IPCP4　[R]　XXXXXXXX　XXXXXXXX		IPCP5　[R]　XXXXXXXX　XXXXXXXX		
0002D8$_H$	IPCP6　[R]　XXXXXXXX　XXXXXXXX		IPCP7　[R]　XXXXXXXX　XXXXXXXX		
0002DC$_H$	OCS45 [R/W]　- - - 0 - - 00　0000 - - 00		OCS67 [R/W]　- - - 0 - - 00　0000 - - 00		Output Compare 4 to 7
0002E0$_H$	OCCP4 [R/W]　XXXXXXXX　XXXXXXXX		OCCP5 [R/W]　XXXXXXXX　XXXXXXXX		
0002E4$_H$	OCCP6 [R/W]　XXXXXXXX　XXXXXXXX		OCCP7 [R/W]　XXXXXXXX　XXXXXXXX		
0002E8$_H$ to 0002EC$_H$	Reserved				Reserved
0002F0$_H$	TCDT4　[R/W]　XXXXXXXX　XXXXXXXX		Reserved	TCCS4　[R/W]　00000000	Free Running Timer 4 (ICU 4, ICU 5)
0002F4$_H$	TCDT5　[R/W]　XXXXXXXX　XXXXXXXX		Reserved	TCCS5　[R/W]　00000000	Free Running Timer 5 (ICU 6, ICU 7)
0002F8$_H$	TCDT6　[R/W]　XXXXXXXX　XXXXXXXX		Reserved	TCCS6　[R/W]　00000000	Free Running Timer 6 (OCU 4, OCU 5)
0002FC$_H$	TCDT7　[R/W]　XXXXXXXX　XXXXXXXX		Reserved	TCCS7　[R/W]　00000000	Free Running Timer 7 (OCU 6, OCU 7)

Address	Register				Block
	+0	+1	+2	+3	
000300H	UDRC1 [W] 00000000	UDRC0 [W] 00000000	UDCR1 [R] 00000000	UDCR0 [R] 00000000	Up/Down Counter 0 to 1
000304H	UDCCH0 [R/W] 00000000	UDCCL0 [R/W] 00001000	Reserved	UDCS0 [R/W] 00000000	
000308H	UDCCH1 [R/W] 00000000	UDCCL1 [R/W] 00001000	Reserved	UDCS1 [R/W] 00000000	
00030CH to 00031CH	Reserved				Reserved
000320H	GCN13 [R/W] 00110010 00010000		Reserved	GCN23 [R/W] - - - - 0000	PPG Control 12 to 15
000324H to 00032CH	Reserved				Reserved
000330H	PTMR12 [R] 11111111 11111111		PCSR12 [W] XXXXXXXX XXXXXXXX		PPG 12
000334H	PDUT12 [W] XXXXXXXX XXXXXXXX		PCNH12 [R/W] 0000000 -	PCNL12 [R/W] 000000 - 0	
000338H	PTMR13 [R] 11111111 11111111		PCSR13 [W] XXXXXXXX XXXXXXXX		PPG 13
00033CH	PDUT13 [W] XXXXXXXX XXXXXXXX		PCNH13 [R/W] 0000000 -	PCNL13 [R/W] 000000 - 0	
000340H	PTMR14 [R] 11111111 11111111		PCSR14 [W] XXXXXXXX XXXXXXXX		PPG 14
000344H	PDUT14 [W] XXXXXXXX XXXXXXXX		PCNH14 [R/W] 0000000 -	PCNL14 [R/W] 000000 - 0	
000348H	PTMR15 [R] 11111111 11111111		PCSR15 [W] XXXXXXXX XXXXXXXX		PPG 15
00034CH	PDUT15 [W] XXXXXXXX XXXXXXXX		PCNH15 [R/W] 0000000 -	PCNL15 [R/W] 000000 - 0	
000350H to 00038CH	Reserved				Reserved
000390H	ROMS [R] 11111111 00000000 (MB91F467BA/466BA) 11111111 01000011 (MB91F465BB/464BB)		Reserved		ROM Select Register
000394H to 0003ECH	Reserved				Reserved
0003F0H	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
0003F4H	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8H	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FCH	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400H to 00043CH	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
000440_H	ICR00 [R/W] ---11111	ICR01 [R/W] ---11111	ICR02 [R/W] ---11111	ICR03 [R/W] ---11111	Interrupt Controller
000444_H	ICR04 [R/W] ---11111	ICR05 [R/W] ---11111	ICR06 [R/W] ---11111	ICR07 [R/W] ---11111	
000448_H	ICR08 [R/W] ---11111	ICR09 [R/W] ---11111	ICR10 [R/W] ---11111	ICR11 [R/W] ---11111	
00044C_H	ICR12 [R/W] ---11111	ICR13 [R/W] ---11111	ICR14 [R/W] ---11111	ICR15 [R/W] ---11111	
000450_H	ICR16 [R/W] ---11111	ICR17 [R/W] ---11111	ICR18 [R/W] ---11111	ICR19 [R/W] ---11111	
000454_H	ICR20 [R/W] ---11111	ICR21 [R/W] ---11111	ICR22 [R/W] ---11111	ICR23 [R/W] ---11111	
000458_H	ICR24 [R/W] ---11111	ICR25 [R/W] ---11111	ICR26 [R/W] ---11111	ICR27 [R/W] ---11111	
00045C_H	ICR28 [R/W] ---11111	ICR29 [R/W] ---11111	ICR30 [R/W] ---11111	ICR31 [R/W] ---11111	
000460_H	ICR32 [R/W] ---11111	ICR33 [R/W] ---11111	ICR34[R/W] ---11111	ICR35 [R/W] ---11111	
000464_H	ICR36 [R/W] ---11111	ICR37 [R/W] ---11111	ICR38 [R/W] ---11111	ICR39 [R/W] ---11111	
000468_H	ICR40 [R/W] ---11111	ICR41 [R/W] ---11111	ICR42 [R/W] ---11111	ICR43 [R/W] ---11111	
00046C_H	ICR44 [R/W] ---11111	ICR45 [R/W] ---11111	ICR46 [R/W] ---11111	ICR47 [R/W] ---11111	
000470_H	ICR48 [R/W] ---11111	ICR49 [R/W] ---11111	ICR50 [R/W] ---11111	ICR51 [R/W] ---11111	
000474_H	ICR52 [R/W] ---11111	ICR53 [R/W] ---11111	ICR54 [R/W] ---11111	ICR55 [R/W] ---11111	
000478_H	ICR56 [R/W] ---11111	ICR57 [R/W] ---11111	ICR58 [R/W] ---11111	ICR59 [R/W] ---11111	
00047C_H	ICR60 [R/W] ---11111	ICR61 [R/W] ---11111	ICR62 [R/W] ---11111	ICR63 [R/W] ---11111	Interrupt Controller
000480_H	RSRR [R/W] 10000000	STCR [R/W] 00110011	TBCR [R/W] 00XXXX00	CTBR [W] XXXXXXXX	Clock Control
000484_H	CLKR [R/W] - - - - 0000	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011	DIVR1 [R/W] 00000000	
000488_H	Reserved				Reserved
00048C_H	PLLDIVM [R/W] - - - - 0000	PLLDIVN [R/W] - - 000000	PLLDIVG [R/W] - - - - 0000	PLLMULG [R/W] 00000000	PLL Interface
000490_H	PLLCTRL [R/W] - - - - 0000	Reserved			
000494_H	OSCC1 [R/W] - - - - - 010	OSCS1 [R/W] 00001111	OSCC2 [R/W] - - - - - 010	OSCS2 [R/W] 00001111	Main/Sub Oscillator Control (Reserved)
000498_H	PORTEN [R/W] - - - - - - 00	Reserved			Port Input Enable Control

Address	Register				Block
	+0	**+1**	**+2**	**+3**	
0004A0_H	Reserved	WTCER [R/W] - - - - - - 00	WTCR [R/W] 00000000 000 - 00 - 0		Real Time Clock (Watch Timer)
0004A4_H	Reserved	WTBR [R/W] - - - XXXXX XXXXXXXX XXXXXXXX			
0004A8_H	WTHR [R/W] - - - 00000	WTMR [R/W] - - 000000	WTSR [R/W] - - 000000	Reserved	
0004AC_H	CSVTR [R/W] - - - 00010	CSVCR [R/W] **-** 011100	CSCFG [R/W] 0X000000	CMCFG [R/W] 00000000	Clock- Supervisor / Selector/ Monitor
0004B0_H	CUCR [R/W] - - - - - - - - - - - 0 - - 00		CUTD [R/W] 10000000 00000000		Calibration of Sub Clock
0004B4_H	CUTR1 [R] - - - - - - - - 00000000		CUTR2 [R] 00000000 00000000		
0004B8_H	CMPR [R/W] - - 000010 11111101		Reserved	CMCR [R/W] - 001 - - 00	Clock Modulator
0004BC_H	CMT1 [R/W] 00000000 1 - - - 0000		CMT2 [R/W] - - 000000 - - 000000		
0004C0_H	CANPRE [R/W] 0 - - - 0000	CANCKD [R/W] - - 000000	Reserved		CAN Clock Control
0004C4_H	LVSEL [R/W] 00000111	LVDET [R/W] 00000 - 00	HWWDE [R/W] - - - - - - 00	HWWD [R/W,W] 00011000	Low Voltage Detection/ Hardware Watchdog
0004C8_H	OSCRH [R/W] 000 - - 001	OSCRL [R/W] - - - - - 000	WPCRH [R/W] 000 - - 001	WPCRL [R/W] - - - - - - 00	Main-/Sub-Oscillation Sta- bilisation Timer
0004CC_H	OSCCR [R/W] - - - - - - 00	Reserved	REGSEL [R/W] - - 000110	REGCTR [R/W] - - - 0 - - 00	Main- Oscillation Standby Control / Main/ Sub Regulator Control
0004D0_H to 00063C_H	Reserved				Reserved

Address	Register				Block
	+0	**+1**	**+2**	**+3**	
000640H	ASR0 [R/W] 00000000 00000000		ACR0 [R/W] 1111**00 00000000[2]		External Bus Unit
000644H	ASR1 [R/W] XXXXXXXX XXXXXXXX		ACR1 [R/W] XXXXXXXX XXXXXXXX		
000648H	ASR2 [R/W] XXXXXXXX XXXXXXXX		ACR2 [R/W] XXXXXXXX XXXXXXXX		
00064CH	ASR3 [R/W] XXXXXXXX XXXXXXXX		ACR3 [R/W] XXXXXXXX XXXXXXXX		
000650H	ASR4 [R/W] XXXXXXXX XXXXXXXX		ACR4 [R/W] XXXXXXXX XXXXXXXX		
000654H	ASR5 [R/W] XXXXXXXX XXXXXXXX		ACR5 [R/W] XXXXXXXX XXXXXXXX		
000658H	ASR6 [R/W] XXXXXXXX XXXXXXXX		ACR6 [R/W] XXXXXXXX XXXXXXXX		
00065CH	ASR7 [R/W] XXXXXXXX XXXXXXXX		ACR7 [R/W] XXXXXXXX XXXXXXXX		
000660H	AWR0 [R/W] 01111111 11111*11		AWR1 [R/W] XXXXXXXX XXXXXXXX		
000664H	AWR2 [R/W] XXXXXXXX XXXXXXXX		AWR3 [R/W] XXXXXXXX XXXXXXXX		
000668H	AWR4 [R/W] XXXXXXXX XXXXXXXX		AWR5 [R/W] XXXXXXXX XXXXXXXX		
00066CH	AWR6 [R/W] XXXXXXXX XXXXXXXX		AWR7 [R/W] XXXXXXXX XXXXXXXX		
000670H	MCRA [R/W] XXXXXXXX	MCRB [R/W] XXXXXXXX	Reserved		
000674H	Reserved				
000678H	IOWR0 [R/W] XXXXXXXX	IOWR1 [R/W] XXXXXXXX	IOWR2 [R/W] XXXXXXXX	IOWR3 [R/W] XXXXXXXX	
00067CH	Reserved				
000680H	CSER [R/W] 00000001	CHER [R/W] 11111111	Reserved	TCR [R/W] 0000**** [3]	
000684H	RCRH [R/W] 00XXXXXX	RCRL [R/W] XXXX0XXX	Reserved		
000688H to 0007F8H	Reserved				External Bus Unit
0007FCH	Reserved	MODR [W] XXXXXXXX	Reserved		Mode Register
000800H to 000CFCH	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
000D00H	PDRD00 [R] XXXXXXXX	PDRD01 [R] XXXXXXXX	Reserved		R-bus Port Data Direct Read Register
000D04H	Reserved	PDRD05 [R] - - XXXXXX	PDRD06 [R] XXXXXXXX	PDRD07 [R] XXXXXXXX	
000D08H	PDRD08 [R] X - - X - - -X	PDRD09 [R] - - - - - - XX	PDRD10 [R] - - - - - - - X	Reserved	
000D0CH	Reserved		PDRD14 [R] XXXXXXXX	PDRD15 [R] XXXXXXXX	
000D10H	PDRD16 [R] XXXXXXXX	PDRD17 [R] XXXXXXXX	PDRD18 [R] - XXX - XXX	PDRD19 [R] - XXX - XXX	
000D14H	PDRD20 [R] - XXX - XXX	PDRD21 [R] - - - - - - X	PDRD22 [R] XXXXXXXX	PDRD23 [R] XXXXXXXX	
000D18H	PDRD24 [R] XXXXXXXX	Reserved	PDRD26 [R] XXXXXXXX	PDRD27 [R] XXXXXXXX	
000D1CH	PDRD28 [R] XXXXXXXX	PDRD29 [R] XXXXXXXX	Reserved		
000D20H to 000D3CH	Reserved				
000D40H	DDR00 [R/W] 00000000	DDR01 [R/W] 00000000	Reserved		R-bus Port Direction Register
000D44H	Reserved	DDR05 [R/W] - - 000000	DDR06 [R/W] 00000000	DDR07 [R/W] 00000000	
000D48H	DDR08 [R/W] 0 - - 0 - - -0	DDR09 [R/W] - - - - - - 00	DDR10 [R/W] - - - - - - -0	Reserved	
000D4CH	Reserved		DDR14 [R/W] 00000000	DDR15 [R/W] 00000000	
000D50H	DDR16 [R/W] 00000000	DDR17 [R/W] 00000000	DDR18 [R/W] - 000 - 000	DDR19 [R/W] - 000 - 000	
000D54H	DDR20 [R/W] - 000 - 000	DDR21 [R/W] - - - - - - 00	DDR22 [R/W] 00000000	DDR23 [R/W] 00000000	
000D58H	DDR24 [R/W] 00000000	Reserved	DDR26 [R/W] 00000000	DDR27 [R/W] 00000000	
000D5CH	DDR28 [R/W] 00000000	DDR29 [R/W] 00000000	Reserved		
000D60H to 000D7CH	Reserved				Reserved

Address	Register				Block
	+0	**+1**	**+2**	**+3**	
000D80$_H$	PFR00 [R/W] 11111111	PFR01 [R/W] 11111111	Reserved		R-bus Port Function Register
000D84$_H$	Reserved	PFR05 [R/W] - - 111111	PFR06 [R/W] 11111111	PFR07 [R/W] 11111111	
000D88$_H$	PFR08 [R/W] 1 - - 1 - - 11	PFR09 [R/W] - - - - - - 11	PFR10 [R/W] - - - - - - -1	Reserved	
000D8C$_H$	Reserved		PFR14 [R/W] 00000000	PFR15 [R/W] 00000000	
000D90$_H$	PFR16 [R/W] 00000000	PFR17 [R/W] 00000000	PFR18 [R/W] - 000 - 000	PFR19 [R/W] - 000 - 000	
000D94$_H$	PFR20 [R/W] - 000 - 000	PFR21 [R/W] - - - - - - 00	PFR22 [R/W] 0000-0-0	PFR23 [R/W] -0000000	
000D98$_H$	PFR24 [R/W] 00000000	Reserved	PFR26 [R/W] 00000000	PFR27 [R/W] 00000000	
000D9C$_H$	PFR28 [R/W] 00000000	PFR29 [R/W] 00000000	Reserved		
000DA0$_H$ to 000DC4$_H$	Reserved				
000DC8$_H$	Reserved		EPFR10 [R/W] - - - - - - - 0	Reserved	R-bus Port Extra Function Register
000DCC$_H$	Reserved		EPFR14 [R/W] 00000000	EPFR15 [R/W] 00000000	
000DD0$_H$	EPFR16 [R/W] 0 - 00 - - - -	Reserved	EPFR18 [R/W] - 000 - 000	EPFR19 [R/W] - 0- - - 0- -	
000DD4$_H$	EPFR20 [R/W] - 000 - 000	EPFR21 [R/W] - - - - - - - -	Reserved		
000DD8$_H$	Reserved		EPFR26 [R/W] 00000000	EPFR27 [R/W] 00000000	
000DDC$_H$ to 000DFC$_H$	Reserved				Reserved
000E00$_H$	PODR00 [R/W] 00000000	PODR01 [R/W] 00000000	Reserved		R-bus Port Output Drive Select Register
000E04$_H$	Reserved	PODR05 [R/W] - - 000000	PODR06 [R/W] 00000000	PODR07 [R/W] 00000000	
000E08$_H$	PODR08 [R/W] 0 - - 0 - - - 0	PODR09 [R/W] - - - - - - 00	PODR10 [R/W] - - - - - - - 0	Reserved	
000E0C$_H$	Reserved		PODR14 [R/W] 00000000	PODR15 [R/W] 00000000	
000E10$_H$	PODR16 [R/W] 00000000	PODR17 [R/W] 00000000	PODR18 [R/W] - 000 - 000	PODR19 [R/W] - 000 - 000	
000E14$_H$	PODR20 [R/W] - 000 - 000	PODR21 [R/W] - - - - - - 00	PODR22 [R/W] 00000000	PODR23 [R/W] 00000000	
000E18$_H$	PODR24 [R/W] 00000000	Reserved	PODR26 [R/W] 00000000	PODR27 [R/W] 00000000	
000E1C$_H$	PODR28 [R/W] 00000000	PODR29 [R/W] 00000000	Reserved		
000E20$_H$ to 000E3C$_H$	Reserved				Reserved

Address	Register				Block
	+0	**+1**	**+2**	**+3**	
000E40$_H$	PILR00 [R/W] 00000000	PILR01 [R/W] 00000000	Reserved		R-bus Port Input Level Select Register
000E44$_H$	Reserved	PILR05 [R/W] - - 000000	PILR06 [R/W] 00000000	PILR07 [R/W] 00000000	
000E48$_H$	PILR08 [R/W] 0 - - 0 - - - 0	PILR09 [R/W] - - - - - - 00	PILR10 [R/W] - - - - - - - 0	Reserved	
000E4C$_H$	Reserved		PILR14 [R/W] 00000000	PILR15 [R/W] 00000000	
000E50$_H$	PILR16 [R/W] 00000000	PILR17 [R/W] 00000000	PILR18 [R/W] - - - - - 000	PILR19 [R/W] - 000 - 000	
000E54$_H$	PILR20 [R/W] - 000 - 000	PILR21 [R/W] - - - - - - 00	PILR22 [R/W] 00000000	PILR23 [R/W] 00000000	
000E58$_H$	PILR24 [R/W] 00000000	Reserved	PILR26 [R/W] 00000000	PILR27 [R/W] 00000000	
000E5C$_H$	PILR28 [R/W] 00000000	PILR29 [R/W] 00000000	Reserved		
000E60$_H$ to 000E7C$_H$	Reserved				Reserved
000E80$_H$	EPILR00 [R/W] 00000000	EPILR01 [R/W] 00000000	Reserved		R-bus Port Extra Input Level Select Register
000E84$_H$	Reserved	EPILR05 [R/W] - - 000000	EPILR06 [R/W] 00000000	EPILR07 [R/W] 00000000	
000E88$_H$	EPILR08 [R/W] 0 - - 0- - - 0	EPILR09 [R/W] - - - - - - 00	EPILR10 [R/W] - - - - - - - 0	Reserved	
000E8C$_H$	Reserved		EPILR14 [R/W] 00000000	EPILR15 [R/W] 00000000	
000E90$_H$	EPILR16 [R/W] 00000000	EPILR17 [R/W] 00000000	EPILR18 [R/W] - - - - - 000	EPILR19 [R/W] - 000 - 000	
000E94$_H$	EPILR20 [R/W] - 000 - 000	EPILR21 [R/W] - - - - - - 00	EPILR22 [R/W] 00000000	EPILR23 [R/W] 00000000	
000E98$_H$	EPILR24 [R/W] 00000000	Reserved	EPILR26 [R/W] 00000000	EPILR27 [R/W] 00000000	
000E9C$_H$	EPILR28 [R/W] 00000000	EPILR29 [R/W] 00000000	Reserved		
000EA0$_H$ to 000EBC$_H$	Reserved				Reserved

Address	Register				Block
	+0	**+1**	**+2**	**+3**	
000EC0$_H$	PPER00 [R/W] 00000000	PPER01 [R/W] 00000000	Reserved		R-bus Port Pull-Up/Down Enable Register
000EC4$_H$	Reserved	PPER05 [R/W] - - 000000	PPER06 [R/W] 00000000	PPER07 [R/W] 00000000	
000EC8$_H$	PPER08 [R/W] 0 - - 0 - - - 0	PPER09 [R/W] - - - - - - 00	PPER10 [R/W] - - - - - - - 0	Reserved	
000ECC$_H$	Reserved		PPER14 [R/W] 00000000	PPER15 [R/W] 00000000	
000ED0$_H$	PPER16 [R/W] 00000000	PPER17 [R/W] 00000000	PPER18 [R/W] - 000 - 000	PPER19 [R/W] - 000 - 000	
000ED4$_H$	PPER20 [R/W] - 000 - 000	PPER21 [R/W] - - - - - - 00	PPER22 [R/W] 00000000	PPER23 [R/W] 00000000	
000ED8$_H$	PPER24 [R/W] 00000000	Reserved	PPER26 [R/W] 00000000	PPER27 [R/W] 00000000	
000EDC$_H$	PPER28 [R/W] 00000000	PPER29 [R/W] 00000000	Reserved		
000EE0$_H$ to 000EFC$_H$	Reserved				Reserved
000F00$_H$	PPCR00 [R/W] 11111111	PPCR01 [R/W] 11111111	Reserved		R-bus Port Pull-Up/Down Control Register
000F04$_H$	Reserved	PPCR05 [R/W] - - 111111	PPCR06 [R/W] 11111111	PPCR07 [R/W] 11111111	
000F08$_H$	PPCR08 [R/W] 1 - - 1 - - - 1	PPCR09 [R/W] - - - - - - 11	PPCR10 [R/W] - - - - - - - 1	Reserved	
000F0C$_H$	Reserved		PPCR14 [R/W] 00000000	PPCR15 [R/W] 11111111	
000F10$_H$	PPCR16 [R/W] 00000000	PPCR17 [R/W] 00000000	PPCR18 [R/W] - 111- 111	PPCR19 [R/W] - 111- 111	
000F14$_H$	PPCR20 [R/W] - 111- 111	PPCR21 [R/W] - - - - - - 11	PPCR22 [R/W] 11111111	PPCR23 [R/W] 11111111	
000F18$_H$	PPCR24 [R/W] 11111111	Reserved	PPCR26 [R/W] 11111111	PPCR27 [R/W] 11111111	
000F1C$_H$	PPCR28 [R/W] 11111111	PPCR29 [R/W] 11111111	Reserved		
000F20$_H$ to 000F3C$_H$	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
001000H	DMASA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004H	DMADA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008H	DMASA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00100CH	DMADA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010H	DMASA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014H	DMADA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018H	DMASA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00101CH	DMADA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020H	DMASA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024H	DMADA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001028H to 003FFCH	Reserved				Reserved
002000H to 006FFCH	Flash-cache size is 8 Kbytes : 004000H to 005FFCH				Flash-cache / I-RAM area
007000H	FMCS [R/W] 01101000	FMCR [R/W] - - - - 0000	FCHCR [R/W] - - - - - - 00 10000011		Flash Memory/ I-Cache Control Register
007004H	FMWT [R/W] 11111111 11111111		Reserved	FMPS [R/W] - - - - - 000	
007008H	FMAC [R] 00000000 00000000 00000000 00000000				
00700CH	FCHA0 [R/W] - - - - - - - - - - 000000 00000000 00000000				I-Cache Non-cacheable area setting Register
007010H	FCHA1 [R/W] - - - - - - - - - - 000000 00000000 00000000				
007014H to 007FFCH	Reserved				Reserved
008000H to 00BFFCH	Boot-ROM size is 4 Kbytes : 00B000H to 00BFFCH (instruction access is 1 wait cycle, data access is 1 wait cycle)				Boot ROM area
00C000H	CTRLR0 [R/W] 00000000 00000001		STATR0 [R/W] 00000000 00000000		CAN 0 Control Register
00C004H	ERRCNT0 [R] 00000000 00000000		BTR0 [R/W] 00100011 00000001		
00C008H	INTR0 [R] 00000000 00000000		TESTR0 [R/W] 00000000 X0000000		
00C00CH	BRPE0 [R/W] 00000000 00000000		CBSYNC0		

Address	Register				Block
	+0	**+1**	**+2**	**+3**	
00C010_H	IF1CREQ0 [R/W] 00000000 00000001		IF1CMSK0 [R/W] 00000000 00000000		CAN 0 IF 1 Register
00C014_H	IF1MSK20 [R/W] 11111111 11111111		IF1MSK10 [R/W] 11111111 11111111		
00C018_H	IF1ARB20 [R/W] 00000000 00000000		IF1ARB10 [R/W] 00000000 00000000		
00C01C_H	IF1MCTR0 [R/W] 00000000 00000000		Reserved		
00C020_H	IF1DTA10 [R/W] 00000000 00000000		IF1DTA20 [R/W] 00000000 00000000		
00C024_H	IF1DTB10 [R/W] 00000000 00000000		IF1DTB20 [R/W] 00000000 00000000		
00C028_H to 00C02C_H	Reserved				
00C030_H	IF1DTA20 [R/W] 00000000 00000000		IF1DTA10 [R/W] 00000000 00000000		
00C034_H	IF1DTB20 [R/W] 00000000 00000000		IF1DTB10 [R/W] 00000000 00000000		
00C038_H to 00C03C_H	Reserved				
00C040_H	IF2CREQ0 [R/W] 00000000 00000001		IF2CMSK0 [R/W] 00000000 00000000		CAN 0 IF 2 Register
00C044_H	IF2MSK20 [R/W] 11111111 11111111		IF2MSK10 [R/W] 11111111 11111111		
00C048_H	IF2ARB20 [R/W] 00000000 00000000		IF2ARB10 [R/W] 00000000 00000000		
00C04C_H	IF2MCTR0 [R/W] 00000000 00000000		Reserved		
00C050_H	IF2DTA10 [R/W] 00000000 00000000		IF2DTA20 [R/W] 00000000 00000000		
00C054_H	IF2DTB10 [R/W] 00000000 00000000		IF2DTB20 [R/W] 00000000 00000000		
00C058_H to 00C05C_H	Reserved				
00C060_H	IF2DTA20 [R/W] 00000000 00000000		IF2DTA10 [R/W] 00000000 00000000		
00C064_H	IF2DTB20 [R/W] 00000000 00000000		IF2DTB10 [R/W] 00000000 00000000		
00C068_H to 00C07C_H	Reserved				

Address	Register				Block
	+0	**+1**	**+2**	**+3**	
00C080$_H$	TREQR20 [R] 00000000 00000000		TREQR10 [R] 00000000 00000000		CAN 0 Status Flags
00C084$_H$ to 00C08C$_H$	Reserved		Reserved		
00C090$_H$	NEWDT20 [R] 00000000 00000000		NEWDT10 [R] 00000000 00000000		
00C094$_H$ to 00C09C$_H$	Reserved		Reserved		
00C0A0$_H$	INTPND20 [R] 00000000 00000000		INTPND10 [R] 00000000 00000000		
00C0A4$_H$ to 00C0AC$_H$	Reserved		Reserved		
00C0B0$_H$	MSGVAL20 [R] 00000000 00000000		MSGVAL10 [R] 00000000 00000000		
00C0B4$_H$ to 00C0FC$_H$	Reserved		Reserved		
00C100$_H$	CTRLR1 [R/W] 00000000 00000001		STATR1 [R/W] 00000000 00000000		CAN 1 Control Register
00C104$_H$	ERRCNT1 [R] 00000000 00000000		BTR1 [R/W] 00100011 00000001		
00C108$_H$	INTR1 [R] 00000000 00000000		TESTR1 [R/W] 00000000 X0000000		
00C10C$_H$	BRPE1 [R/W] 00000000 00000000		CBSYNC1		
00C110$_H$	IF1CREQ1 [R/W] 00000000 00000001		IF1CMSK1 [R/W] 00000000 00000000		CAN 1 IF 1 Register
00C114$_H$	IF1MSK21 [R/W] 11111111 11111111		IF1MSK11 [R/W] 11111111 11111111		
00C118$_H$	IF1ARB21 [R/W] 00000000 00000000		IF1ARB11 [R/W] 00000000 00000000		
00C11C$_H$	IF1MCTR1 [R/W] 00000000 00000000		Reserved		
00C120$_H$	IF1DTA11 [R/W] 00000000 00000000		IF1DTA21 [R/W] 00000000 00000000		
00C124$_H$	IF1DTB11 [R/W] 00000000 00000000		IF1DTB21 [R/W] 00000000 00000000		
00C128$_H$ to 00C12C$_H$	Reserved				
00C130$_H$	IF1DTA21 [R/W] 00000000 00000000		IF1DTA11 [R/W] 00000000 00000000		
00C134$_H$	IF1DTB21 [R/W] 00000000 00000000		IF1DTB11 [R/W] 00000000 00000000		
00C138$_H$ to 00C13C$_H$	Reserved				

Address	Register				Block
	+0	**+1**	**+2**	**+3**	
00C140$_H$	IF2CREQ1 [R/W] 00000000 00000001		IF2CMSK1 [R/W] 00000000 00000000		CAN 1 IF 2 Register
00C144$_H$	IF2MSK21 [R/W] 11111111 11111111		IF2MSK11 [R/W] 11111111 11111111		
00C148$_H$	IF2ARB21 [R/W] 00000000 00000000		IF2ARB11 [R/W] 00000000 00000000		
00C14C$_H$	IF2MCTR1 [R/W] 00000000 00000000		Reserved		
00C150$_H$	IF2DTA11 [R/W] 00000000 00000000		IF2DTA21 [R/W] 00000000 00000000		
00C154$_H$	IF2DTB11 [R/W] 00000000 00000000		IF2DTB21 [R/W] 00000000 00000000		
00C158$_H$ to 00C15C$_H$	Reserved				
00C160$_H$	IF2DTA21 [R/W] 00000000 00000000		IF2DTA11 [R/W] 00000000 00000000		
00C164$_H$	IF2DTB21 [R/W] 00000000 00000000		IF2DTB11 [R/W] 00000000 00000000		
00C168$_H$ to 00C17C$_H$	Reserved				
00C180$_H$	TREQR21 [R] 00000000 00000000		TREQR11 [R] 00000000 00000000		CAN 1 Status Flags
00C184$_H$ to 00C18C$_H$	Reserved		Reserved		
00C190$_H$	NEWDT21 [R] 00000000 00000000		NEWDT11 [R] 00000000 00000000		
00C194$_H$ to 00C19C$_H$	Reserved		Reserved		
00C1A0$_H$	INTPND21 [R] 00000000 00000000		INTPND11 [R] 00000000 00000000		
00C1A4$_H$ to 00C1AC$_H$	Reserved		Reserved		
00C1B0$_H$	MSGVAL21 [R] 00000000 00000000		MSGVAL11 [R] 00000000 00000000		
00C1B4$_H$ to 00C1FC$_H$	Reserved		Reserved		
00C200$_H$	CTRLR2 [R/W] 00000000 00000001		STATR2 [R/W] 00000000 00000000		CAN 2 Control Register
00C204$_H$	ERRCNT2 [R] 00000000 00000000		BTR2 [R/W] 00100011 00000001		
00C208$_H$	INTR2 [R] 00000000 00000000		TESTR2 [R/W] 00000000 X0000000		
00C20C$_H$	BRPE2 [R/W] 00000000 00000000		CBSYNC2		

Address	Register				Block
	+0	**+1**	**+2**	**+3**	
00C210_H	IF1CREQ2 [R/W] 00000000 00000001		IF1CMSK2 [R/W] 00000000 00000000		CAN 2 IF 1 Register
00C214_H	IF1MSK22 [R/W] 11111111 11111111		IF1MSK12 [R/W] 11111111 11111111		
00C218_H	IF1ARB22 [R/W] 00000000 00000000		IF1ARB12 [R/W] 00000000 00000000		
00C21C_H	IF1MCTR2 [R/W] 00000000 00000000		Reserved		
00C220_H	IF1DTA12 [R/W] 00000000 00000000		IF1DTA22 [R/W] 00000000 00000000		
00C224_H	IF1DTB12 [R/W] 00000000 00000000		IF1DTB22 [R/W] 00000000 00000000		
00C228_H to 00C22C_H	Reserved				
00C230_H	IF1DTA22 [R/W] 00000000 00000000		IF1DTA12 [R/W] 00000000 00000000		
00C234_H	IF1DTB22 [R/W] 00000000 00000000		IF1DTB12 [R/W] 00000000 00000000		
00C238_H to 00C23C_H	Reserved				CAN 2 IF 2 Register
00C240_H	IF2CREQ2 [R/W] 00000000 00000001		IF2CMSK2 [R/W] 00000000 00000000		
00C244_H	IF2MSK22 [R/W] 11111111 11111111		IF2MSK12 [R/W] 11111111 11111111		
00C248_H	IF2ARB22 [R/W] 00000000 00000000		IF2ARB12 [R/W] 00000000 00000000		
00C24C_H	IF2MCTR2 [R/W] 00000000 00000000		Reserved		
00C250_H	IF2DTA12 [R/W] 00000000 00000000		IF2DTA22 [R/W] 00000000 00000000		
00C254_H	IF2DTB12 [R/W] 00000000 00000000		IF2DTB22 [R/W] 00000000 00000000		
00C258_H to 00C25C_H	Reserved				
00C260_H	IF2DTA22 [R/W] 00000000 00000000		IF2DTA12 [R/W] 00000000 00000000		
00C264_H	IF2DTB22 [R/W] 00000000 00000000		IF2DTB12 [R/W] 00000000 00000000		
00C268_H to 00C27C_H	Reserved				

Address	Register				Block
	+0	**+1**	**+2**	**+3**	
00C280$_H$	TREQR22 [R] 00000000 00000000		TREQR12 [R] 00000000 00000000		CAN 2 Status Flags
00C284$_H$ to 00C28C$_H$	Reserved		Reserved		
00C290$_H$	NEWDT22 [R] 00000000 00000000		NEWDT12 [R] 00000000 00000000		
00C294$_H$ to 00C29C$_H$	Reserved		Reserved		
00C2A0$_H$	INTPND22 [R] 00000000 00000000		INTPND12 [R] 00000000 00000000		
00C2A4$_H$ to 00C2AC$_H$	Reserved		Reserved		
00C2B0$_H$	MSGVAL22 [R] 00000000 00000000		MSGVAL12 [R] 00000000 00000000		
00C2B4$_H$ to 00C2FC$_H$	Reserved				Reserved
00C300$_H$	CTRLR3 [R/W] 00000000 00000001		STATR3 [R/W] 00000000 00000000		CAN 3 Control Register **Note:** Not on MB91F465BB/MB91F464 BB
00C304$_H$	ERRCNT3 [R] 00000000 00000000		BTR3 [R/W] 00100011 00000001		
00C308$_H$	INTR3 [R] 00000000 00000000		TESTR3 [R/W] 00000000 X0000000		
00C30C$_H$	BRPE3 [R/W] 00000000 00000000		CBSYNC3		

Address	Register				Block
	+0	**+1**	**+2**	**+3**	
00C310$_H$	IF1CREQ3 [R/W] 00000000 00000001		IF1CMSK3 [R/W] 00000000 00000000		CAN 3 IF 1 Register **Note**: Not on MB91F465BB/MB91F464BB
00C314$_H$	IF1MSK23 [R/W] 11111111 11111111		IF1MSK13 [R/W] 11111111 11111111		
00C318$_H$	IF1ARB23 [R/W] 00000000 00000000		IF1ARB13 [R/W] 00000000 00000000		
00C31C$_H$	IF1MCTR3 [R/W] 00000000 00000000		Reserved		
00C320$_H$	IF1DTA13 [R/W] 00000000 00000000		IF1DTA23 [R/W] 00000000 00000000		
00C324$_H$	IF1DTB13 [R/W] 00000000 00000000		IF1DTB23 [R/W] 00000000 00000000		
00C328$_H$ to 00C32C$_H$	Reserved				
00C330$_H$	IF1DTA23 [R/W] 00000000 00000000		IF1DTA13 [R/W] 00000000 00000000		
00C334$_H$	IF1DTB23 [R/W] 00000000 00000000		IF1DTB13 [R/W] 00000000 00000000		
00C338$_H$ to 00C33C$_H$	Reserved				
00C340$_H$	IF2CREQ3 [R/W] 00000000 00000001		IF2CMSK3 [R/W] 00000000 00000000		CAN 3 IF 2 Register **Note:** Not on MB91F465BB/MB91F464BB
00C344$_H$	IF2MSK23 [R/W] 11111111 11111111		IF2MSK13 [R/W] 11111111 11111111		
00C348$_H$	IF2ARB23 [R/W] 00000000 00000000		IF2ARB13 [R/W] 00000000 00000000		
00C34C$_H$	IF2MCTR3 [R/W] 00000000 00000000		Reserved		
00C350$_H$	IF2DTA13 [R/W] 00000000 00000000		IF2DTA23 [R/W] 00000000 00000000		
00C354$_H$	IF2DTB13 [R/W] 00000000 00000000		IF2DTB23 [R/W] 00000000 00000000		
00C358$_H$ to 00C35C$_H$	Reserved				
00C360$_H$	IF2DTA23 [R/W] 00000000 00000000		IF2DTA13 [R/W] 00000000 00000000		
00C364$_H$	IF2DTB23 [R/W] 00000000 00000000		IF2DTB13 [R/W] 00000000 00000000		
00C368$_H$ to 00C37C$_H$	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
00C380H	TREQR23 [R] 00000000 00000000		TREQR13 [R] 00000000 00000000		CAN 3 Status Flags **Note**: Not on MB91F465BB/MB91F464 BB
00C384H to 00C38CH	Reserved				
00C390H	NEWDT23 [R] 00000000 00000000		NEWDT13 [R] 00000000 00000000		
00C394H to 00C39CH	Reserved				
00C3A0H	INTPND23 [R] 00000000 00000000		INTPND13 [R] 00000000 00000000		
00C3A4H to 00C3ACH	Reserved				
00C3B0H	MSGVAL23 [R] 00000000 00000000		MSGVAL13 [R] 00000000 00000000		
00C3B4H to 00C3FCH	Reserved				
00C400H	CTRLR4 [R/W] 00000000 00000001		STATR4 [R/W] 00000000 00000000		CAN 4 Control Register **Note**: Not on MB91F465BB/MB91F464 BB
00C404H	ERRCNT4 [R] 00000000 00000000		BTR4 [R/W] 00100011 00000001		
00C408H	INTR4 [R] 00000000 00000000		TESTR4 [R/W] 00000000 X0000000		
00C40CH	BRPE4 [R/W] 00000000 00000000		CBSYNC4		
00C410H	IF1CREQ4 [R/W] 00000000 00000001		IF1CMSK4 [R/W] 00000000 00000000		CAN 4 IF 1 Register **Note:** Not on MB91F465BB/MB91F464 BB
00C414H	IF1MSK24 [R/W] 11111111 11111111		IF1MSK14 [R/W] 11111111 11111111		
00C418H	IF1ARB24 [R/W] 00000000 00000000		IF1ARB14 [R/W] 00000000 00000000		
00C41CH	IF1MCTR4 [R/W] 00000000 00000000		Reserved		
00C420H	IF1DTA14 [R/W] 00000000 00000000		IF1DTA24 [R/W] 00000000 00000000		
00C424H	IF1DTB14 [R/W] 00000000 00000000		IF1DTB24 [R/W] 00000000 00000000		
00C428H to 00C42CH	Reserved				
00C430H	IF1DTA24 [R/W] 00000000 00000000		IF1DTA14 [R/W] 00000000 00000000		
00C434H	IF1DTB24 [R/W] 00000000 00000000		IF1DTB14 [R/W] 00000000 00000000		
00C438H to 00C43CH	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
00C440_H	IF2CREQ4 [R/W] 00000000 00000001		IF2CMSK4 [R/W] 00000000 00000000		CAN 4 IF 2 Register **Note:** Not on MB91F465BB/MB91F464 BB
00C444_H	IF2MSK24 [R/W] 11111111 11111111		IF2MSK14 [R/W] 11111111 11111111		
00C448_H	IF2ARB24 [R/W] 00000000 00000000		IF2ARB14 [R/W] 00000000 00000000		
00C44C_H	IF2MCTR4 [R/W] 00000000 00000000		Reserved		
00C450_H	IF2DTA14 [R/W] 00000000 00000000		IF2DTA24 [R/W] 00000000 00000000		
00C454_H	IF2DTB14 [R/W] 00000000 00000000		IF2DTB24 [R/W] 00000000 00000000		
00C458_H to 00C45C_H	Reserved				
00C460_H	IF2DTA24 [R/W] 00000000 00000000		IF2DTA14 [R/W] 00000000 00000000		
00C464_H	IF2DTB24 [R/W] 00000000 00000000		IF2DTB14 [R/W] 00000000 00000000		
00C468_H to 00C47C_H	Reserved				
00C480_H	TREQR24 [R] 00000000 00000000		TREQR14 [R] 00000000 00000000		CAN 4 Status Flags **Note:** Not on MB91F465BB/MB91F464 BB
00C484_H to 00C48C_H	Reserved				
00C490_H	NEWDT24 [R] 00000000 00000000		NEWDT14 [R] 00000000 00000000		
00C494_H to 00C49C_H	Reserved				
00C4A0_H	INTPND24 [R] 00000000 00000000		INTPND14 [R] 00000000 00000000		
00C4A4_H to 00C4AC_H	Reserved				
00C4B0_H	MSGVAL24 [R] 00000000 00000000		MSGVAL14 [R] 00000000 00000000		
00C4B4_H to 00C4FC_H	Reserved				
00C500_H	CTRLR5 [R/W] 00000000 00000001		STATR5 [R/W] 00000000 00000000		CAN 5 Control Register **Note:** Not on MB91F465BB/MB91F464 BB
00C504_H	ERRCNT5 [R] 00000000 00000000		BTR5 [R/W] 00100011 00000001		
00C508_H	INTR5 [R] 00000000 00000000		TESTR5 [R/W] 00000000 X0000000		
00C50C_H	BRPE5 [R/W] 00000000 00000000		CBSYNC5		

Address	Register				Block
	+0	+1	+2	+3	
00C510_H	IF1CREQ5 [R/W] 00000000 00000001		IF1CMSK5 [R/W] 00000000 00000000		CAN 5 IF 1 Register **Note:** Not on MB91F465BB/MB91F464 BB
00C514_H	IF1MSK25 [R/W] 11111111 11111111		IF1MSK15 [R/W] 11111111 11111111		
00C518_H	IF1ARB25 [R/W] 00000000 00000000		IF1ARB15 [R/W] 00000000 00000000		
00C51C_H	IF1MCTR5 [R/W] 00000000 00000000		Reserved		
00C520_H	IF1DTA15 [R/W] 00000000 00000000		IF1DTA25 [R/W] 00000000 00000000		
00C524_H	IF1DTB15 [R/W] 00000000 00000000		IF1DTB25 [R/W] 00000000 00000000		
00C528_H to 00C52C_H	Reserved				
00C530_H	IF1DTA25 [R/W] 00000000 00000000		IF1DTA15 [R/W] 00000000 00000000		
00C534_H	IF1DTB25 [R/W] 00000000 00000000		IF1DTB15 [R/W] 00000000 00000000		
00C538_H to 00C53C_H	Reserved				
00C540_H	IF2CREQ5 [R/W] 00000000 00000001		IF2CMSK5 [R/W] 00000000 00000000		CAN 5 IF 2 Register **Note**: Not on MB91F465BB/MB91F464 BB
00C544_H	IF2MSK25 [R/W] 11111111 11111111		IF2MSK15 [R/W] 11111111 11111111		
00C548_H	IF2ARB25 [R/W] 00000000 00000000		IF2ARB15 [R/W] 00000000 00000000		
00C54C_H	IF2MCTR5 [R/W] 00000000 00000000		Reserved		
00C550_H	IF2DTA15 [R/W] 00000000 00000000		IF2DTA25 [R/W] 00000000 00000000		
00C554_H	IF2DTB15 [R/W] 00000000 00000000		IF2DTB25 [R/W] 00000000 00000000		
00C558_H to 00C55C_H	Reserved				
00C560_H	IF2DTA25 [R/W] 00000000 00000000		IF2DTA15 [R/W] 00000000 00000000		
00C564_H	IF2DTB25 [R/W] 00000000 00000000		IF2DTB15 [R/W] 00000000 00000000		
00C568_H to 00C57C_H	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
00C580$_H$	TREQR25 [R] 00000000 00000000		TREQR15 [R] 00000000 00000000		CAN 5 Status Flags **Note:** Not on MB91F465BB/MB91F464BB
00C584$_H$ to 00C58C$_H$	Reserved				
00C590$_H$	NEWDT25 [R] 00000000 00000000		NEWDT15 [R] 00000000 00000000		
00C594$_H$ to 00C59C$_H$	Reserved				
00C5A0$_H$	INTPND25 [R] 00000000 00000000		INTPND15 [R] 00000000 00000000		
00C5A4$_H$ to 00C5AC$_H$	Reserved				
00C5B0$_H$	MSGVAL25 [R] 00000000 00000000		MSGVAL15 [R] 00000000 00000000		
00C5B4$_H$ to 00EFFC$_H$	Reserved				
00F000$_H$	BCTRL [R/W] -------- -------- 11111100 00000000				EDSU / MPU
00F004$_H$	BSTAT [R/W] -------- -----000 00000000 10 - - 000000				
00F008$_H$	BIAC [R] -------- -------- 00000000 00000000				
00F00C$_H$	BOAC [R] -------- -------- 00000000 00000000				
00F010$_H$	BIRQ [R/W] -------- -------- 00000000 00000000				
00F014$_H$ to 00F01C$_H$	Reserved				
00F020$_H$	BCR0 [R/W] -------- 00000000 00000000 00000000				
00F024$_H$	BCR1 [R/W] -------- 00000000 00000000 00000000				
00F028$_H$	BCR2 [R/W] -------- 00000000 00000000 00000000				
00F02C$_H$	BCR3 [R/W] -------- 00000000 00000000 00000000				
00F030$_H$ to 00F07C$_H$	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
00F080_H	BAD0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				EDSU / MPU
00F084_H	BAD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F088_H	BAD2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F08C_H	BAD3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F090_H	BAD4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F094_H	BAD5 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F098_H	BAD6 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F09C_H	BAD7 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0A0_H	BAD8 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0A4_H	BAD9 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0A8_H	BAD10 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0AC_H	BAD11 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0B0_H	BAD12 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0B4_H	BAD13 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0B8_H	BAD14 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0BC_H	BAD15 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0C0_H to 01FFFC_H	Reserved				EDSU / MPU
020000_H to 02FFFC_H	D-RAM size is 24 Kbytes : 02A000_H - 02FFFC_H (data access is 0 wait cycles)				D-RAM area
030000_H to 03FFFC_H	ID-RAM size is 16 Kbytes : 030000_H - 033FFC_H (instruction access is 0 wait cycles, data access is 1 wait cycle)				ID-RAM area

1. depends on the number of available CAN channels

2. ACR0 [11 : 10] depends on Mode vector fetch information on bus width

3. TCR [3 : 0] INIT value = 0000, keeps value after RST

12.2   Flash Memory and External Bus Area

12.2.1   MB91F467BA/466BA

64bit read	dat[63:0]							
32bit read/write	dat[31:0]				dat[31:0]			
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]	
Address	**Register**							**Block**
	+ 0	+ 1	+ 2	+ 3	+ 4	+ 5	+ 6	+ 7	
040000$_H$ to 05FFF8$_H$	SA8 (64KB)				SA9 (64KB)				ROMS0
060000$_H$ to 07FFF8$_H$	SA10 (64KB)				SA11 (64KB)				ROMS1
080000$_H$ to 09FFF8$_H$	SA12 (64KB)				SA13 (64KB)				ROMS2
0A0000$_H$ to 0BFFF8$_H$	SA14 (64KB)				SA15 (64KB)				ROMS3
0C0000$_H$ to 0DFFF8$_H$	SA16 (64KB)				SA17 (64KB)				ROMS4
0E0000$_H$ to 0FFFF0$_H$	SA18 (64KB)				SA19 (64KB)				ROMS5
0FFFF8$_H$	FMV [R] 06 00 00 00$_H$				FRV [R] 00 00 BF F8$_H$				
100000$_H$ to 11FFF8$_H$	SA20 (64KB, MB91F467BA) Reserved (MB91F466BA)				SA21 (64KB, MB91F467BA) Reserved (MB91F466BA)				ROMS6
120000$_H$ to 13FFF8$_H$	SA22 (64KB, MB91F467BA) Reserved (MB91F466BA)				SA23 (64KB, MB91F467B) Reserved (MB91F466BA)				
140000$_H$ to 143FF8$_H$	SA0 (8KB)				SA1 (8KB)				ROMS7
144000$_H$ to 17FF8$_H$	SA2 (8KB)				SA3 (8KB)				
148000$_H$ to 14BFF8$_H$	SA4 (8KB)				SA5 (8KB)				
14C000$_H$ to 14FFF8$_H$	SA6 (8KB)				SA7 (8KB)				
150000$_H$ to17FFF8$_H$	Reserved								

64bit read	dat[63:0]								
32bit read/write	dat[31:0]				dat[31:0]				
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
Address	**Register**								**Block**
	+ 0	+ 1	+ 2	+ 3	+ 4	+ 5	+ 6	+ 7	
180000$_H$ to 1BFFF8$_H$									ROMS8
1C0000$_H$ to 1FFFF8$_H$									ROMS9
200000$_H$ to 27FFF8$_H$									ROMS10
280000$_H$ to 2FFFF8$_H$									ROMS11
300000$_H$ to 37FFF8$_H$				External Bus Area					ROMS12
380000$_H$ to 3FFFF8$_H$									ROMS13
400000$_H$ to 47FFF8$_H$									ROMS14
480000$_H$ to 4FFFF8$_H$									ROMS15

Notes: Write operations to address 0FFFF8$_H$ and 0FFFFC$_H$ are not possible. When reading these addresses, the values shown above will be read.

12.2.2 MB91F465BB/464BB

32bit read	dat[31:0]				dat[31:0]				
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
Address	Register								Block
	+ 0	+ 1	+ 2	+ 3	+ 4	+ 5	+ 6	+ 7	
040000$_H$ to 05FFF8$_H$	Reserved				Reserved				ROMS0
060000$_H$ to 07FFF8$_H$	Reserved				Reserved				ROMS1
080000$_H$ to 09FFF8$_H$	SA12 (64KB) Reserved (MB91F464BB)				SA13 (64KB) Reserved (MB91F464BB)				ROMS2
0A0000$_H$ to 0BFFF8$_H$	SA14 (64KB)				SA15 (64KB)				ROMS3
0C0000$_H$ to 0DFFF8$_H$	SA16 (64KB)				SA17 (64KB)				ROMS4
0E0000$_H$ to 0FFFF0$_H$	SA18 (64KB)				SA19 (64KB)				ROMS5
0FFFF8$_H$	FMV [R] 06 00 00 00$_H$				FRV [R] 00 00 BF F8$_H$				
100000$_H$ to 11FFF8$_H$	External Bus Area								ROMS6
120000$_H$ to 13FFF8$_H$									
140000$_H$ to 143FF8$_H$	External Bus Area								ROMS7
144000$_H$ to 17FF8$_H$									
148000$_H$ to 14BFF8$_H$	SA4 (8KB)				SA5 (8KB)				
14C000$_H$ to 14FFF8$_H$	SA6 (8KB)				SA7 (8KB)				
150000$_H$ to17FFF8$_H$	Reserved								

32bit read/write	dat[31:0]				dat[31:0]				
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
Address	**Register**								**Block**
	+ 0	+ 1	+ 2	+ 3	+ 4	+ 5	+ 6	+ 7	
180000_H to $1BFFF8_H$	External Bus Area								ROMS8
$1C0000_H$ to $1FFFF8_H$									ROMS9
200000_H to $27FFF8_H$									ROMS10
280000_H to $2FFFF8_H$									ROMS11
300000_H to $37FFF8_H$									ROMS12
380000_H to $3FFFF8_H$									ROMS13
400000_H to $47FFF8_H$									ROMS14
480000_H to $4FFFF8_H$									ROMS15

Notes: Write operations to address $0FFFF8_H$ and $0FFFFC_H$ are not possible. When reading these addresses, the values shown above will be read. On MB91F465BB/F464BB, write access to the flash is only possible in 16-bit mode.

13. Interrupt Vector Table

Interrupt	Interrupt number		Interrupt level [1]		Interrupt vector [2]		DMA Resource number
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default vector address	
Reset	0	00	—	—	$3FC_H$	$000FFFFC_H$	—
Mode vector	1	01	—	—	$3F8_H$	$000FFFF8_H$	—
System reserved	2	02	—	—	$3F4_H$	$000FFFF4_H$	—
System reserved	3	03	—	—	$3F0_H$	$000FFFF0_H$	—
System reserved	4	04	—	—	$3EC_H$	$000FFFEC_H$	—
CPU supervisor mode (INT #5 instruction) [5]	5	05	—	—	$3E8_H$	$000FFFE8_H$	—
Memory Protection exception [5]	6	06	—	—	$3E4_H$	$000FFFE4_H$	—
System reserved	7	07	—	—	$3E0_H$	$000FFFE0_H$	—
System reserved	8	08	—	—	$3DC_H$	$000FFFDC_H$	—
System reserved	9	09	—	—	$3D8_H$	$000FFFD8_H$	—
System reserved	10	0A	—	—	$3D4_H$	$000FFFD4_H$	—
System reserved	11	0B	—	—	$3D0_H$	$000FFFD0_H$	—
System reserved	12	0C	—	—	$3CC_H$	$000FFFCC_H$	—
System reserved	13	0D	—	—	$3C8_H$	$000FFFC8_H$	—
Undefined instruction exception	14	0E	—	—	$3C4_H$	$000FFFC4_H$	—
NMI request	15	0F	F_H fixed		$3C0_H$	$000FFFC0_H$	—
External Interrupt 0	16	10	ICR00	440_H	$3BC_H$	$000FFFBC_H$	0, 16
External Interrupt 1	17	11			$3B8_H$	$000FFFB8_H$	1, 17
External Interrupt 2	18	12	ICR01	441_H	$3B4_H$	$000FFFB4_H$	2, 18
External Interrupt 3	19	13			$3B0_H$	$000FFFB0_H$	3, 19
External Interrupt 4	20	14	ICR02	442_H	$3AC_H$	$000FFFAC_H$	20
External Interrupt 5	21	15			$3A8_H$	$000FFFA8_H$	21
External Interrupt 6	22	16	ICR03	443_H	$3A4_H$	$000FFFA4_H$	22
External Interrupt 7	23	17			$3A0_H$	$000FFFA0_H$	23
External Interrupt 8	24	18	ICR04	444_H	$39C_H$	$000FFF9C_H$	—
External Interrupt 9	25	19			398_H	$000FFF98_H$	—
External Interrupt 10	26	1A	ICR05	445_H	394_H	$000FFF94_H$	—
External Interrupt 11	27	1B			390_H	$000FFF90_H$	—
External Interrupt 12	28	1C	ICR06	446_H	$38C_H$	$000FFF8C_H$	—
External Interrupt 13	29	1D			388_H	$000FFF88_H$	—
External Interrupt 14	30	1E	ICR07	447_H	384_H	$000FFF84_H$	—
External Interrupt 15	31	1F			380_H	$000FFF80_H$	—
Reload Timer 0	32	20	ICR08	448_H	$37C_H$	$000FFF7C_H$	4, 32
Reload Timer 1	33	21			378_H	$000FFF78_H$	5, 33
Reload Timer 2	34	22	ICR09	449_H	374_H	$000FFF74_H$	34
Reload Timer 3	35	23			370_H	$000FFF70_H$	35

Interrupt	Interrupt number		Interrupt level [1]		Interrupt vector [2]		DMA Resource number
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default vector address	
Reload Timer 4	36	24	ICR10	44A$_H$	36C$_H$	000FFF6C$_H$	36
Reload Timer 5	37	25			368$_H$	000FFF68$_H$	37
Reload Timer 6	38	26	ICR11	44B$_H$	364$_H$	000FFF64$_H$	38
Reload Timer 7	39	27			360$_H$	000FFF60$_H$	39
Free Run Timer 0	40	28	ICR12	44C$_H$	35C$_H$	000FFF5C$_H$	40
Free Run Timer 1	41	29			358$_H$	000FFF58$_H$	41
Free Run Timer 2	42	2A	ICR13	44D$_H$	354$_H$	000FFF54$_H$	42
Free Run Timer 3	43	2B			350$_H$	000FFF50$_H$	43
Free Run Timer 4	44	2C	ICR14	44E$_H$	34C$_H$	000FFF4C$_H$	44
Free Run Timer 5	45	2D			348$_H$	000FFF48$_H$	45
Free Run Timer 6	46	2E	ICR15	44F$_H$	344$_H$	000FFF44$_H$	46
Free Run Timer 7	47	2F			340$_H$	000FFF40$_H$	47
CAN 0	48	30	ICR16	450$_H$	33C$_H$	000FFF3C$_H$	—
CAN 1	49	31			338$_H$	000FFF38$_H$	—
CAN 2	50	32	ICR17	451$_H$	334$_H$	000FFF34$_H$	—
CAN 3 Not on MB91F465BB/464BB	51	33			330$_H$	000FFF30$_H$	—
CAN 4 Not on MB91F465BB/464BB	52	34	ICR18	452$_H$	32C$_H$	000FFF2C$_H$	—
CAN 5 Not on MB91F465BB/464BB	53	35			328$_H$	000FFF28$_H$	—
LIN-USART 0 RX	54	36	ICR19	453$_H$	324$_H$	000FFF24$_H$	6, 48
LIN-USART 0 TX	55	37			320$_H$	000FFF20$_H$	7, 49
Reserved	56	38	ICR20	454$_H$	31C$_H$	000FFF1C$_H$	8, 50
Reserved	57	39			318$_H$	000FFF18$_H$	9, 51
LIN-USART 2 RX	58	3A	ICR21	455$_H$	314$_H$	000FFF14$_H$	52
LIN-USART 2 TX	59	3B			310$_H$	000FFF10$_H$	53
LIN-USART 3 RX	60	3C	ICR22	456$_H$	30C$_H$	000FFF0C$_H$	54
LIN-USART 3 TX	61	3D			308$_H$	000FFF08$_H$	55
System Reserved	62	3E	ICR23 *3	457$_H$	304$_H$	000FFF04$_H$	—
Delayed Interrupt	63	3F			300$_H$	000FFF00$_H$	—
System Reserved [4]	64	40	ICR24	458$_H$	2FC$_H$	000FFEFC$_H$	—
System Reserved [4]	65	41			2F8$_H$	000FFEF8$_H$	—
LIN-USART (FIFO) 4 RX	66	42	ICR25	459$_H$	2F4$_H$	000FFEF4$_H$	10, 56
LIN-USART (FIFO) 4 TX	67	43			2F0$_H$	000FFEF0$_H$	11, 57
LIN-USART (FIFO) 5 RX	68	44	ICR26	45A$_H$	2EC$_H$	000FFEEC$_H$	12, 58
LIN-USART (FIFO) 5 TX	69	45			2E8$_H$	000FFEE8$_H$	13, 59
LIN-USART (FIFO) 6 RX	70	46	ICR27	45B$_H$	2E4$_H$	000FFEE4$_H$	60
LIN-USART (FIFO) 6 TX	71	47			2E0$_H$	000FFEE0$_H$	61
LIN-USART (FIFO) 7 RX	72	48	ICR28	45C$_H$	2DC$_H$	000FFEDC$_H$	62
LIN-USART (FIFO) 7 TX	73	49			2D8$_H$	000FFED8$_H$	63

Interrupt	Interrupt number		Interrupt level [1]		Interrupt vector [2]		DMA Resource number
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default vector address	
I²C 0	74	4A	ICR29	45D$_H$	2D4$_H$	000FFED4$_H$	—
I²C 1	75	4B			2D0$_H$	000FFED0$_H$	—
Reserved	76	4C	ICR30	45E$_H$	2CC$_H$	000FFECC$_H$	64
Reserved	77	4D			2C8$_H$	000FFEC8$_H$	65
Reserved	78	4E	ICR31	45F$_H$	2C4$_H$	000FFEC4$_H$	66
Reserved	79	4F			2C0$_H$	000FFEC0$_H$	67
Reserved	80	50	ICR32	460$_H$	2BC$_H$	000FFEBC$_H$	68
Reserved	81	51			2B8$_H$	000FFEB8$_H$	69
Reserved	82	52	ICR33	461$_H$	2B4$_H$	000FFEB4$_H$	70
Reserved	83	53			2B0$_H$	000FFEB0$_H$	71
Reserved	84	54	ICR34	462$_H$	2AC$_H$	000FFEAC$_H$	72
Reserved	85	55			2A8$_H$	000FFEA8$_H$	73
Reserved	86	56	ICR35	463$_H$	2A4$_H$	000FFEA4$_H$	74
Reserved	87	57			2A0$_H$	000FFEA0$_H$	75
Reserved	88	58	ICR36	464$_H$	29C$_H$	000FFE9C$_H$	76
Reserved	89	59			298$_H$	000FFE98$_H$	77
Reserved	90	5A	ICR37	465$_H$	294$_H$	000FFE94$_H$	78
Reserved	91	5B			290$_H$	000FFE90$_H$	79
Input Capture 0	92	5C	ICR38	466$_H$	28C$_H$	000FFE8C$_H$	80
Input Capture 1	93	5D			288$_H$	000FFE88$_H$	81
Input Capture 2	94	5E	ICR39	467$_H$	284$_H$	000FFE84$_H$	82
Input Capture 3	95	5F			280$_H$	000FFE80$_H$	83
Input Capture 4	96	60	ICR40	468$_H$	27C$_H$	000FFE7C$_H$	84
Input Capture 5	97	61			278$_H$	000FFE78$_H$	85
Input Capture 6	98	62	ICR41	469$_H$	274$_H$	000FFE74$_H$	86
Input Capture 7	99	63			270$_H$	000FFE70$_H$	87
Output Compare 0	100	64	ICR42	46A$_H$	26C$_H$	000FFE6C$_H$	88
Output Compare 1	101	65			268$_H$	000FFE68$_H$	89
Output Compare 2	102	66	ICR43	46B$_H$	264$_H$	000FFE64$_H$	90
Output Compare 3	103	67			260$_H$	000FFE60$_H$	91
Output Compare 4	104	68	ICR44	46C$_H$	25C$_H$	000FFE5C$_H$	92
Output Compare 5	105	69			258$_H$	000FFE58$_H$	93
Output Compare 6	106	6A	ICR45	46D$_H$	254$_H$	000FFE54$_H$	94
Output Compare 7	107	6B			250$_H$	000FFE50$_H$	95
Sound Generator	108	6C	ICR46	46E$_H$	24C$_H$	000FFE4C$_H$	—
Reserved	109	6D			248$_H$	000FFE48$_H$	—
System Reserved	110	6E	ICR47 [3]	46F$_H$	244$_H$	000FFE44$_H$	—
System Reserved	111	6F			240$_H$	000FFE40$_H$	—
PPG 0	112	70	ICR48	470$_H$	23C$_H$	000FFE3C$_H$	15, 96
PPG 1	113	71			238$_H$	000FFE38$_H$	97

Interrupt	Interrupt number		Interrupt level [1]		Interrupt vector [2]		DMA Resource number
	Decimal	**Hexa-decimal**	**Setting Register**	**Register address**	**Offset**	**Default vector address**	
PPG 2	114	72	ICR49	471_H	234_H	$000FFE34_H$	98
PPG 3	115	73			230_H	$000FFE30_H$	99
PPG 4	116	74	ICR50	472_H	$22C_H$	$000FFE2C_H$	100
PPG 5	117	75			228_H	$000FFE28_H$	101
PPG 6	118	76	ICR51	473_H	224_H	$000FFE24_H$	102
PPG 7	119	77			220_H	$000FFE20_H$	103
PPG 8	120	78	ICR52	474_H	$21C_H$	$000FFE1C_H$	104
PPG 9	121	79			218_H	$000FFE18_H$	105
PPG 10	122	7A	ICR53	475_H	214_H	$000FFE14_H$	106
PPG 11	123	7B			210_H	$000FFE10_H$	107
PPG 12	124	7C	ICR54	476_H	$20C_H$	$000FFE0C_H$	108
PPG 13	125	7D			208_H	$000FFE08_H$	109
PPG 14	126	7E	ICR55	477_H	204_H	$000FFE04_H$	110
PPG 15	127	7F			200_H	$000FFE00_H$	111
Up/Down Counter 0	128	80	ICR56	478_H	$1FC_H$	$000FFDFC_H$	—
Up/Down Counter 1	129	81			$1F8_H$	$000FFDF8_H$	—
Reserved	130	82	ICR57	479_H	$1F4_H$	$000FFDF4_H$	—
Reserved	131	83			$1F0_H$	$000FFDF0_H$	—
Real Time Clock	132	84	ICR58	$47A_H$	$1EC_H$	$000FFDEC_H$	—
Calibration Unit	133	85			$1E8_H$	$000FFDE8_H$	—
A/D Converter 0	134	86	ICR59	$47B_H$	$1E4_H$	$000FFDE4_H$	14, 112
System reserved	135	87			$1E0_H$	$000FFDE0_H$	—
Alarm Comparator 0	136	88	ICR60	$47C_H$	$1DC_H$	$000FFDDC_H$	—
Reserved	137	89			$1D8_H$	$000FFDD8_H$	—
Low Voltage Detection	138	8A	ICR61	$47D_H$	$1D4_H$	$000FFDD4_H$	—
Reserved	139	8B			$1D0_H$	$000FFDD0_H$	—
Time base Overflow	140	8C	ICR62	$47E_H$	$1CC_H$	$000FFDCC_H$	—
PLL Clock Gear	141	8D			$1C8_H$	$000FFDC8_H$	—
DMA Controller	142	8E	ICR63	$47F_H$	$1C4_H$	$000FFDC4_H$	—
Main/Sub OSC stability wait	143	8F			$1C0_H$	$000FFDC0_H$	—
Security vector	144	90	—	—	$1BC_H$	$000FFDBC_H$	—
Used by the INT instruction.	145 to 255	91 to FF	—	—	$1B8_H$ to 000_H	$000FFDB8_H$ to $000FFC00_H$	—

1. The Interrupt Control Registers (ICRs) are located in the interrupt controller and set the interrupt level for each interrupt request. An ICR is provided for each interrupt request.
2. The vector address for each EIT (exception, interrupt or trap) is calculated by adding the listed offset to the table base register value (TBR) . The TBR specifies the top of the EIT vector table. The addresses listed in the table are for the default TBR value ($000FFC00_H$) . The TBR is initialized to this value by a reset. The TBR is set to $000FFC00_H$ after the internal boot ROM is executed.
3. ICR23 and ICR47 can be exchanged by setting the REALOS compatibility bit (addr $0C03_H$: IOS[0])
4. Used by REALOS
5. Memory Protection Unit (MPU) support

14. Recommended Settings

14.1 PLL and Clock Gear Settings

Please note that for MB91F467BA/466BA and MB91F465BB/464BB the core base clock frequencies are valid in the 1.8V operation mode of the Main regulator and Flash.

Table 7. Recommended PLL divider and clock gear settings

PLL Input (CLK) [MHz]	Frequency Parameter		Clockgear Parameter		PLL Output (X) [MHz]	Core Base Clock [MHz]	Remarks
	DIVM	DIVN	DIVG	MULG	MULG		
4	2	25	16	24	200	100	Not on MB91F467BA/466BA
4	2	24	16	24	192	96	
4	2	23	16	24	184	92	
4	2	22	16	24	176	88	
4	2	21	16	20	168	84	
4	2	20	16	20	160	80	
4	2	19	16	20	152	76	
4	2	18	16	20	144	72	
4	2	17	16	16	136	68	
4	2	16	16	16	128	64	
4	2	15	16	16	120	60	
4	2	14	16	16	112	56	
4	2	13	16	12	104	52	
4	2	12	16	12	96	48	
4	2	11	16	12	88	44	
4	4	10	16	24	160	40	
4	4	9	16	24	144	36	
4	4	8	16	24	128	32	
4	4	7	16	24	112	28	
4	6	6	16	24	144	24	
4	8	5	16	28	160	20	
4	10	4	16	32	160	16	
4	12	3	16	32	144	12	

14.2 Clock Modulator settings

The following table shows all possible settings for the Clock Modulator in a base clock frequency range from 32MHz up to 88MHz.

The Flash access time settings need to be adjusted according to Fmax while the PLL and clockgear settings should be set according to base clock frequency.

Table 8. Clock Modulator settings, frequency range and supported supply voltage

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]
1	3	026F	88	79.5	98.5 Not on MB91F467BA/466BA
1	3	026F	84	76.1	93.8
1	3	026F	80	72.6	89.1
1	5	02AE	80	68.7	95.8
2	3	046E	80	68.7	95.8
1	3	026F	76	69.1	84.5
1	5	02AE	76	65.3	90.8
1	7	02ED	76	62	98.1 Not on MB91F467BA/466BA
2	3	046E	76	65.3	90.8
3	3	066D	76	62	98.1 Not on MB91F467BA/466BA
1	3	026F	72	65.5	79.9
1	5	02AE	72	62	85.8
1	7	02ED	72	58.8	92.7
2	3	046E	72	62	85.8
3	3	066D	72	58.8	92.7
1	3	026F	68	62	75.3
1	5	02AE	68	58.7	80.9
1	7	02ED	68	55.7	87.3
1	9	032C	68	53	95
2	3	046E	68	58.7	80.9
2	5	04AC	68	53	95
3	3	066D	68	55.7	87.3
4	3	086C	68	53	95
1	3	026F	64	58.5	70.7
1	5	02AE	64	55.3	75.9
1	7	02ED	64	52.5	82
1	9	032C	64	49.9	89.1
1	11	036B	64	47.6	97.6 Not on MB91F467BA/466BA
2	3	046E	64	55.3	75.9
2	5	04AC	64	49.9	89.1
3	3	066D	64	52.5	82
4	3	086C	64	49.9	89.1

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]
5	3	0A6B	64	47.6	97.6 Not on MB91F467BA/466BA
1	3	026F	60	54.9	66.1
1	5	02AE	60	51.9	71
1	7	02ED	60	49.3	76.7
1	9	032C	60	46.9	83.3
1	11	036B	60	44.7	91.3
2	3	046E	60	51.9	71
2	5	04AC	60	46.9	83.3
3	3	066D	60	49.3	76.7
4	3	086C	60	46.9	83.3
5	3	0A6B	60	44.7	91.3
1	3	026F	56	51.4	61.6
1	5	02AE	56	48.6	66.1
1	7	02ED	56	46.1	71.4
1	9	032C	56	43.8	77.6
1	11	036B	56	41.8	84.9
1	13	03AA	56	39.9	93.8
2	3	046E	56	48.6	66.1
2	5	04AC	56	43.8	77.6
2	7	04EA	56	39.9	93.8
3	3	066D	56	46.1	71.4
3	5	06AA	56	39.9	93.8
4	3	086C	56	43.8	77.6
5	3	0A6B	56	41.8	84.9
6	3	0C6A	56	39.9	93.8
1	3	026F	52	47.8	57
1	5	02AE	52	45.2	61.2
1	7	02ED	52	42.9	66.1
1	9	032C	52	40.8	71.8
1	11	036B	52	38.8	78.6
1	13	03AA	52	37.1	86.8
1	15	03E9	52	35.5	96.9 Not on MB91F467BA/466BA
2	3	046E	52	45.2	61.2
2	5	04AC	52	40.8	71.8
2	7	04EA	52	37.1	86.8
3	3	066D	52	42.9	66.1
3	5	06AA	52	37.1	86.8
4	3	086C	52	40.8	71.8

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]
5	3	0A6B	52	38.8	78.6
6	3	0C6A	52	37.1	86.8
7	3	0E69	52	35.5	96.9 Not on MB91F467BA/466BA
1	3	026F	48	44.2	52.5
1	5	02AE	48	41.8	56.4
1	7	02ED	48	39.6	60.9
1	9	032C	48	37.7	66.1
1	11	036B	48	35.9	72.3
1	13	03AA	48	34.3	79.9
1	15	03E9	48	32.8	89.1
2	3	046E	48	41.8	56.4
2	5	04AC	48	37.7	66.1
2	7	04EA	48	34.3	79.9
3	3	066D	48	39.6	60.9
3	5	06AA	48	34.3	79.9
4	3	086C	48	37.7	66.1
5	3	0A6B	48	35.9	72.3
6	3	0C6A	48	34.3	79.9
7	3	0E69	48	32.8	89.1
1	3	026F	44	40.6	48.1
1	5	02AE	44	38.4	51.6
1	7	02ED	44	36.4	55.7
1	9	032C	44	34.6	60.4
1	11	036B	44	33	66.1
1	13	03AA	44	31.5	73
1	15	03E9	44	30.1	81.4
2	3	046E	44	38.4	51.6
2	5	04AC	44	34.6	60.4
2	7	04EA	44	31.5	73
2	9	0528	44	28.9	92.1
3	3	066D	44	36.4	55.7
3	5	06AA	44	31.5	73
4	3	086C	44	34.6	60.4
4	5	08A8	44	28.9	92.1
5	3	0A6B	44	33	66.1
6	3	0C6A	44	31.5	73
7	3	0E69	44	30.1	81.4
8	3	1068	44	28.9	92.1
1	3	026F	40	37	43.6

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]
1	5	02AE	40	34.9	46.8
1	7	02ED	40	33.1	50.5
1	9	032C	40	31.5	54.8
1	11	036B	40	30	59.9
1	13	03AA	40	28.7	66.1
1	15	03E9	40	27.4	73.7
2	3	046E	40	34.9	46.8
2	5	04AC	40	31.5	54.8
2	7	04EA	40	28.7	66.1
2	9	0528	40	26.3	83.3
3	3	066D	40	33.1	50.5
3	5	06AA	40	28.7	66.1
3	7	06E7	40	25.3	95.8
4	3	086C	40	31.5	54.8
4	5	08A8	40	26.3	83.3
5	3	0A6B	40	30	59.9
6	3	0C6A	40	28.7	66.1
7	3	0E69	40	27.4	73.7
8	3	1068	40	26.3	83.3
9	3	1267	40	25.3	95.8
1	3	026F	36	33.3	39.2
1	5	02AE	36	31.5	42
1	7	02ED	36	29.9	45.3
1	9	032C	36	28.4	49.2
1	11	036B	36	27.1	53.8
1	13	03AA	36	25.8	59.3
1	15	03E9	36	24.7	66.1
2	3	046E	36	31.5	42
2	5	04AC	36	28.4	49.2
2	7	04EA	36	25.8	59.3
2	9	0528	36	23.7	74.7
3	3	066D	36	29.9	45.3
3	5	06AA	36	25.8	59.3
3	7	06E7	36	22.8	85.8
4	3	086C	36	28.4	49.2
4	5	08A8	36	23.7	74.7
5	3	0A6B	36	27.1	53.8
6	3	0C6A	36	25.8	59.3
7	3	0E69	36	24.7	66.1
8	3	1068	36	23.7	74.7

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]
9	3	1267	36	22.8	85.8
1	3	026F	32	29.7	34.7
1	5	02AE	32	28	37.3
1	7	02ED	32	26.6	40.2
1	9	032C	32	25.3	43.6
1	11	036B	32	24.1	47.7
1	13	03AA	32	23	52.5
1	15	03E9	32	22	58.6
2	3	046E	32	28	37.3
2	5	04AC	32	25.3	43.6
2	7	04EA	32	23	52.5
2	9	0528	32	21.1	66.1
2	11	0566	32	19.5	89.1
3	3	066D	32	26.6	40.2
3	5	06AA	32	23	52.5
3	7	06E7	32	20.3	75.9
4	3	086C	32	25.3	43.6
4	5	08A8	32	21.1	66.1
5	3	0A6B	32	24.1	47.7
5	5	0AA6	32	19.5	89.1
6	3	0C6A	32	23	52.5
7	3	0E69	32	22	58.6
8	3	1068	32	21.1	66.1
9	3	1267	32	20.3	75.9
10	3	1466	32	19.5	89.1

15. Electrical Characteristics

15.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply slew rate	–	–	50	V/ms	
Power supply voltage 1[1]	$V_{DD}5R$	– 0.3	+ 6.0	V	
Power supply voltage 2[1]	$V_{DD}5$	– 0.3	+ 6.0	V	
Relationship of the supply voltages	$AV_{CC}5$	$V_{DD}5$-0.3 $V_{DD}35$-0.3	$V_{DD}5$+0.3 $V_{DD}35$+0.3	V	At least one pin of the Ports 26 to 29 (ANn) is used as digital input or output.
		$V_{SS}5$-0.3 $V_{DD}35$-0.3	$V_{DD}5$+0.3 $V_{DD}35$+0.3	V	All pins of the Ports 26 to 29 (ANn) follow the condition of V_{IA}
Analog power supply voltage[1]	$AV_{CC}5$	– 0.3	+ 6.0	V	[2]
Analog reference power supply voltage[1]	AVRH	– 0.3	+ 6.0	V	[2]
Input voltage 1[1]	V_{I1}	Vss5 – 0.3	$V_{DD}5$ + 0.3	V	
Analog pin input voltage[1]	V_{IA}	AVss5 – 0.3	AVcc5 + 0.3	V	
Output voltage 1[1]	V_{O1}	Vss5 – 0.3	$V_{DD}5$ + 0.3	V	
Maximum clamp current	I_{CLAMP}	– 4.0	+ 4.0	mA	[3]
Total maximum clamp current	$\Sigma |I_{CLAMP}|$	–	20	mA	[3]
"L" level maximum output current[4]	I_{OL}	–	10	mA	
"L" level average output current[5]	I_{OLAV}	–	8	mA	
"L" level total maximum output current	ΣI_{OL}	–	100	mA	
"L" level total average output current[6]	ΣI_{OLAV}	–	50	mA	
"H" level maximum output current[4]	I_{OH}	–	– 10	mA	
"H" level average output current[5]	I_{OHAV}	–	– 4	mA	
"H" level total maximum output current	ΣI_{OH}	–	– 100	mA	
"H" level total average output current[6]	ΣI_{OHAV}	–	– 25	mA	
Permitted operating frequency MB91F465BB/F464BB	$f_{max, CLKB}$	–	100	MHz	$T_A \leq 105\ °C$
	$f_{max, CLKP}$	–	50		
	$f_{max, CLKT}$	–	50		
	$f_{max, CLKCAN}$	–	50		
Permitted operating frequency MB91F465BB/F464BB	$f_{max, CLKB}$	–	96	MHz	$T_A \leq 125\ °C$
	$f_{max, CLKP}$	–	48		
	$f_{max, CLKT}$	–	48		
	$f_{max, CLKCAN}$	–	48		
Permitted operating frequency MB91F467BA/F466BA	$f_{max, CLKB}$	–	96	MHz	$T_A \leq 105\ °C$
	$f_{max, CLKP}$	–	48		
	$f_{max, CLKT}$	–	48		
	$f_{max, CLKCAN}$	–	48		

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Permitted operating frequency MB91F467BA/F466BA	$f_{max, CLKB}$	–	92	MHz	$T_A \leq 125\ °C$
	$f_{max, CLKP}$	–	46		
	$f_{max, CLKT}$	–	46		
	$f_{max, CLKCAN}$	–	46		
Permitted power dissipation [7]	P_D	–	1200 [*8]	mW	$T_A \leq 85\ °C$
		–	600 [*8]	mW	$T_A \leq 105\ °C$
		–	1300 [*8]	mW	$T_A \leq 105\ °C$, no Flash program/erase [9]
		–	1000 [*8]	mW	$T_A \leq 115\ °C$, no Flash program/erase [9]
		–	750 [*8]	mW	$T_A \leq 125\ °C$, no Flash program/erase [9]
Operating temperature	T_A	– 40	+ 125	°C	
Storage temperature	Tstg	– 55	+ 150	°C	

1. The parameter is based on $V_{SS}5 = AV_{SS}5 = 0.0$ V.
2. $AV_{CC}5$ and AVRH5 must not exceed $V_{DD}5 + 0.3$ V.
3.

■ Use within recommended operating conditions.

■ Use with DC voltage (current).

■ +B signals are input signals that exceed the $V_{DD}5$ voltage. +B signals should always be applied by connecting a limiting resistor between the +B signal and the microcontroller.

■ The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed the rated value at any time, either instantaneously or for an extended period, when the +B signal is input.

■ Note that when the microcontroller drive current is low, such as in the low power consumption modes, the +B input potential can increase the potential at the power supply pin via a protective diode, possibly affecting other devices.

■ Note that if the +B signal is input when the microcontroller is off (not fixed at 0 V), power is supplied through the +B input pin; therefore, the microcontroller may partially operate.

■ Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.

■ Do not leave +B input pins open.

Figure 2. Example of recommended circuit :
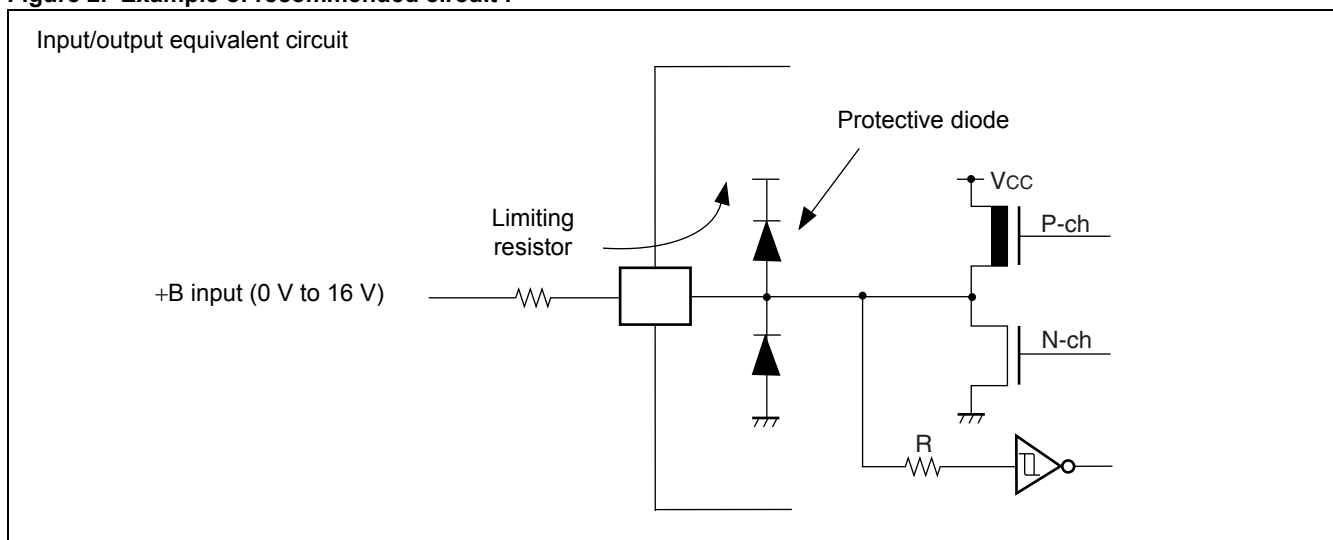
4. Maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

5. Average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 100 ms period.

6. Total average output current is defined as the value of the average current flowing through all of the corresponding pins for a 100 ms period.

7. The maximum permitted power dissipation depends onm the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.

The actual power dissipation depends on the customer application and can be calculated as follows:

$P_D = P_{IO} + P_{INT}$

$P_{IO} = \Sigma (V_{OL} * I_{OL} + V_{OH} + I_{OH})$ (IO load power dissipation, sum is performed on all IO ports)

$P_{INT} = V_{DD}5R * I_{CC} + AV_{CC}5 * I_A + AVRH5 * I_R$ (internal power dissipation)

8. Worst case value for the QFP package mounted on a 4-layer PCB at specified T_A without air flow.

9. Please contact Fujitsu for reliability limitations when using under these conditions.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

15.2   Recommended Operating Conditions

$(V_{SS}5 = AV_{SS}5 = 0.0\ V)$

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	$V_{DD}5$	3.0	-	5.5	V	
	$V_{DD}5R$	3.0	-	5.5	V	Internal regulator
	$AV_{CC}5$	3.0	-	5.5	V	A/D converter
Smoothing capacitor at VCC18C pin	C_S	-	4.7	-	mF	Use a X7R ceramic capacitor or a capacitor that has similar frequency characteristics.
Power supply slew rate		-	-	50	V/ms	
Operating temperature	T_A	- 40	-	+ 125	°C	
Main Oscillation stabilisation time		10			ms	
Lock-up time PLL (4 MHz ->16 ...100MHz)				0.6	ms	
ESD Protection (Human body model)	V_{surge}	2			kV	$R_{discharge}$ = 1.5kW $C_{discharge}$ = 100pF
RC Oscillator	$f_{RC100kHz}$ f_{RC2MHz}	50 1	100 2	200 4	kHz MHz	VDD_{CORE} ≥ 1.65V

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

15.3 DC Characteristics

($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40\ °C$ to $+125\ °C$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input "H" voltage	V_{IH}	-	Port inputs if CMOS Hysteresis 0.8/0.2 input is selected	$0.8 × V_{DD}$	-	$V_{DD} + 0.3$	V	CMOS hysteresis input
		-	Port inputs if CMOS Hysteresis 0.7/0.3 input is selected	$0.7 × V_{DD}$	-	$V_{DD} + 0.3$	V	4.5 V ? V_{DD} ? 5.5 V
				$0.74 × V_{DD}$	-	$V_{DD} + 0.3$	V	3 V ? V_{DD} < 4.5 V
		-	AUTOMOTIVE Hysteresis input is selected	$0.8 × V_{DD}$	-	$V_{DD} + 0.3$	V	
		-	Port inputs if TTL input is selected	2.0	-	$V_{DD} + 0.3$	V	
	V_{IHR}	INITX	-	$0.8 × V_{DD}$	-	$V_{DD} + 0.3$	V	INITX input pin (CMOS Hysteresis)
	V_{IHM}	MD_3 to MD_0	-	$V_{DD} - 0.3$	-	$V_{DD} + 0.3$	V	Mode input pins
	V_{IHX0S}	X0, X0A	-	2.5	-	$V_{DD} + 0.3$	V	External clock in "Oscillation mode"
	V_{IHX0F}	X0	-	$0.8 × V_{DD}$	-	$V_{DD} + 0.3$	V	External clock in "Fast Clock Input mode"
Input "L" voltage	V_{IL}	-	Port inputs if CMOS Hysteresis 0.8/0.2 input is selected	$V_{SS} - 0.3$	-	$0.2 × V_{DD}$	V	
		-	Port inputs if CMOS Hysteresis 0.7/0.3 input is selected	$V_{SS} - 0.3$	-	$0.3 × V_{DD}$	V	
		-	Port inputs if AUTOMOTIVE Hysteresis input is selected	$V_{SS} - 0.3$	-	$0.5 × V_{DD}$	V	4.5 V ≤ V_{DD} ≤ 5.5 V
				$V_{SS} - 0.3$	-	$0.46 × V_{DD}$	V	3 V ≤ V_{DD} < 4.5 V
		-	Port inputs if TTL input is selected	$V_{SS} - 0.3$	-	0.8	V	
	V_{ILR}	INITX	-	$V_{SS} - 0.3$	-	$0.2 × V_{DD}$	V	INITX input pin (CMOS Hysteresis)
	V_{ILM}	MD_3 to MD_0	-	$V_{SS} - 0.3$	-	$V_{SS} + 0.3$	V	Mode input pins
	V_{ILXDS}	X0, X0A	-	$V_{SS} - 0.3$	-	0.5	V	External clock in "Oscillation mode"

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input "L" voltage	V_{ILXDF}	X0	-	V_{SS} - 0.3	-	$0.2 \times V_{DD}$	V	External clock in "Fast Clock Input mode"
Output "H" voltage	V_{OH2}	Normal outputs	$4.5V \leq V_{DD} \leq 5.5V$, I_{OH} = - 2mA	V_{DD} - 0.5	-	-	V	Driving strength set to 2 mA
			$3.0V \leq V_{DD} \leq 4.5V$, I_{OH} = - 1.6mA					
	V_{OH5}	Normal outputs	$4.5V \leq V_{DD} \leq 5.5V$, I_{OH} = - 5mA	V_{DD} - 0.5	-	-	V	Driving strength set to 5 mA
			$3.0V \leq V_{DD} \leq 4.5V$, I_{OH} = - 3mA					
	V_{OH3}	I²C outputs	$3.0V \leq V_{DD} \leq 5.5V$, I_{OH} = - 3mA	V_{DD} - 0.5	-	-	V	
Output "L" voltage	V_{OL2}	Normal outputs	$4.5V \leq V_{DD} \leq 5.5V$, I_{OH} = + 2mA	-	-	0.4	V	Driving strength set to 2 mA
			$3.0V \leq V_{DD} \leq 4.5V$, I_{OH} = + 1.6mA					
	V_{OL5}	Normal outputs	$4.5V \leq V_{DD} \leq 5.5V$, I_{OH} = + 5mA	-	-	0.4	V	Driving strength set to 5 mA
			$3.0V \leq V_{DD} \leq 4.5V$, I_{OH} = + 3mA					
	V_{OL3}	I²C outputs	$3.0V \leq V_{DD} \leq 5.5V$, I_{OH} = + 3mA	-	-	0.4	V	
Input leakage current	I_{IL}	Pnn_m[1]	$3.0V \leq V_{DD} \leq 5.5V$ $V_{SS}5 < V_I < V_{DD}$ T_A=25 °C	- 1	-	+ 1	mA	
			$3.0V \leq V_{DD} \leq 5.5V$ $V_{SS}5 < V_I < V_{DD}$ T_A=125 °C	- 3	-	+ 3		
Analog input leakage current	I_{AIN}	ANn[2]	$3.0V \leq V_{DD} \leq 5.5V$ T_A=25 °C	- 1	-	+ 1	mA	
			$3.0V \leq V_{DD} \leq 5.5V$ T_A=125 °C	- 3	-	+ 3	mA	
Pull-up resistance	R_{UP}	Pnn_m [3] INITX	$3.0V \leq V_{DD} \leq 3.6V$	40	100	160	kW	
			$4.5V \leq V_{DD} \leq 5.5V$	25	50	100		
Pull-down resistance	R_{DOWN}	Pnn_m [4]	$3.0V \leq V_{DD} \leq 3.6V$	40	100	180	kW	
			$4.5V \leq V_{DD} \leq 5.5V$	25	50	100		
Input capacitance	C_{IN}	All except $V_{DD}5$, $V_{DD}5R$, $V_{SS}5$, $AV_{CC}5$, $AV_{SS}5$, AVRH5	f = 1 MHz	-	5	15	pF	

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current F467BA F466BA	I_{CC}	$V_{DD}5R$	CLKB: 96 MHz CLKP: 48 MHz CLKT: 48 MHz CLKCAN: 48 MHz	–	120	150	mA	Code fetch from Flash
	I_{CCH}	$V_{DD}5R$	$T_A = + 25$ °C	–	30	150	µA	At stop mode [5]
			$T_A = + 105$ °C	–	0.4	2.0	mA	
			$T_A = + 125$ °C	–	1.0	5.0	mA	
			$T_A = + 25$ °C	–	100	500	µA	RTC: 4 MHz mode [5]
			$T_A = + 105$ °C	–	0.5	2.4	mA	
			$T_A = + 125$ °C	–	1.1	5.4	mA	
			$T_A = + 25$ °C	–	50	250	µA	RTC: 100 kHz mode [5]
			$T_A = + 105$ °C	–	0.45	2.2	mA	
			$T_A = + 125$ °C	–	1.05	5.2	mA	
	I_{LVE}	$V_{DD}5$	–	–	70	150	µA	External low voltage detection
	I_{LVI}	$V_{DD}5R$	–	–	50	100	µA	Internal low voltage detection
	I_{OSC}	$V_{DD}5$	–	–	250	500	µA	Main clock (4 MHz)
			–	–	20	40	µA	Sub clock (32 kHz)
Power supply current F465BB F464BB	I_{CC}	$V_{DD}5R$	CLKB: 100 MHz CLKP: 50 MHz CLKT: 50 MHz CLKCAN: 50 MHz	-	110	140	mA	Code fetch from Flash
	I_{CCH}	$V_{DD}5R$	$T_A = + 25$ °C	-	30	150	µA	At stop mode [5]
			$T_A = + 105$ °C	-	0.3	2.0	mA	
			$T_A = + 125$ °C	-	0.75	5.0	mA	
			$T_A = + 25$ °C	-	100	500	µA	RTC: 4 MHz mode [5]
			$T_A = + 105$ °C	-	0.5	2.4	mA	
			$T_A = + 125$ °C	-	0.85	5.4	mA	
			$T_A = + 25$ °C	-	50	250	µA	RTC: 100 kHz mode[5]
			$T_A = + 105$ °C	-	0.4	2.2	mA	
			$T_A = + 125$ °C	-	0.8	5.2	mA	
	I_{LVE}	$V_{DD}5$	–	–	70	150	µA	External low voltage detection
	I_{LVI}	$V_{DD}5R$	–	–	50	100	µA	Internal low voltage detection
	I_{OSC}	$V_{DD}5$	-	-	250	500	µA	Main clock (4 MHz)
			-	-	20	40	µA	Sub clock (32 kHz)

1. Pnn_m includes all GPIO pins. Analog (AN) channels and PullUp/PullDown are disabled.
2. ANn includes all pins where AN channels are enabled.
3. Pnn_m includes all GPIO pins. The pull up resistors must be enabled by PPER/PPCR setting and the pins must be in input direction.
4. Pnn_m includes all GPIO pins. The pull down resistors must be enabled by PPER/PPCR setting and the pins must be in input direction.
5. Main regulator OFF, sub regulator set to 1.2V, Low voltage detection disabled.

15.4   A/D Converter Characteristics

($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40\ °C$ to $+125\ °C$)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	–	–	–	–	10	bit	
Total error	–	–	-3	–	$+3$	LSB	
Nonlinearity error	–	–	-2.5	–	$+2.5$	LSB	
Differential nonlinearity error	–	–	-1.9	–	$+1.9$	LSB	
Zero reading voltage	V_{OT}	ANn	AVRL-1.5 LSB	AVRL$+0.5$ LSB	AVRL$+2.5$ LSB	V	
Full scale reading voltage	V_{FST}	ANn	AVRH-3.5 LSB	AVRH-1.5 LSB	AVRH$+0.5$ LSB	V	
Compare time	T_{comp}	–	0.6	–	16,500	μs	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V
			2.0	–	–	μs	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V
Sampling time	T_{samp}	–	0.4	–	–	μs	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V, R_{EXT} < 2 kΩ
			1.0	–	–	μs	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V, R_{EXT} < 1 kΩ
Conversion time	T_{conv}	–	1.0	–	–	μs	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V
			3.0	–	–	μs	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V
Input capacitance	C_{IN}	ANn	–	–	11	pF	
Input resistance	R_{IN}	ANn	–	–	2.6	kΩ	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V
			–	–	12.1	kΩ	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V
Analog input leakage current	I_{AIN}	ANn	-1	–	$+1$	μA	$T_A = +25\ °C$
			-3	–	$+3$	μA	$T_A = +125\ °C$
Analog input voltage range	V_{AIN}	ANn	AVRL	–	AVRH	V	
Offset between input channels	–	ANn	–	–	4	LSB	

Note: The accuracy gets worse as AVRH - AVRL becomes smaller

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	**Typ**	**Max**		
Reference voltage range	AVRH	AVRH5	$0.75 \times AV_{CC}5$	-	$AV_{CC}5$	V	
	AVRL	$AV_{SS}5$	$AV_{SS}5$	-	$AV_{CC}5 \times 0.25$	V	
Power supply current per ADC macro [3]	I_A	$AV_{CC}5$	-	2.5	5	mA	A/D Converter active
	I_{AH}	$AV_{CC}5$	-	-	5	µA	A/D Converter not operated [1]
Reference voltage current per ADC macro [3]	I_R	AVRH5	-	0.7	1	mA	A/D Converter active
	I_{RH}	AVRH5	-	-	5	µA	A/D Converter not operated [2]

1. Supply current at $AV_{CC}5$, if A/D converter and ALARM comparator are not operating, ($V_{DD}5 = AV_{CC}5 = AVRH = 5.0$ V)
2. Input current at AVRH5, if A/D converter is not operating, ($V_{DD}5 = AV_{CC}5 = AVRH = 5.0$ V)
3. The current consumption per ADC macro is given here. On devices having more then one A/D converter, the current values have to be multiplied by the number of macros.

Sampling Time Calculation
$T_{samp} = (2.6 \text{ kOhm} + R_{EXT}) \times 11pF \times 7$; for $4.5V \leq AV_{CC}5 \leq 5.5V$
$T_{samp} = (12.1 \text{ kOhm} + R_{EXT}) \times 11pF \times 7$; for $3.0V \leq AV_{CC}5 \leq 4.5V$

Conversion Time Calculation
$T_{conv} = T_{samp} + T_{comp}$

15.4.1   Definition of A/D Converter Terms

■ Resolution
Analog variation that is recognizable by the A/D converter.

■ Nonlinearity error
Deviation between actual conversion characteristics and a straight line connecting the zero transition point
($00\ 0000\ 0000_B \leftrightarrow 00\ 0000\ 0001_B$) and the full scale transition point ($11\ 1111\ 1110_B \leftrightarrow 11\ 1111\ 1111_B$).

■ Differential nonlinearity error
Deviation of the input voltage from the ideal value that is required to change the output code by 1 LSB.

■ Total error
This error indicates the difference between actual and theoretical values, including the zero transition error, full scale transition error, and nonlinearity error.
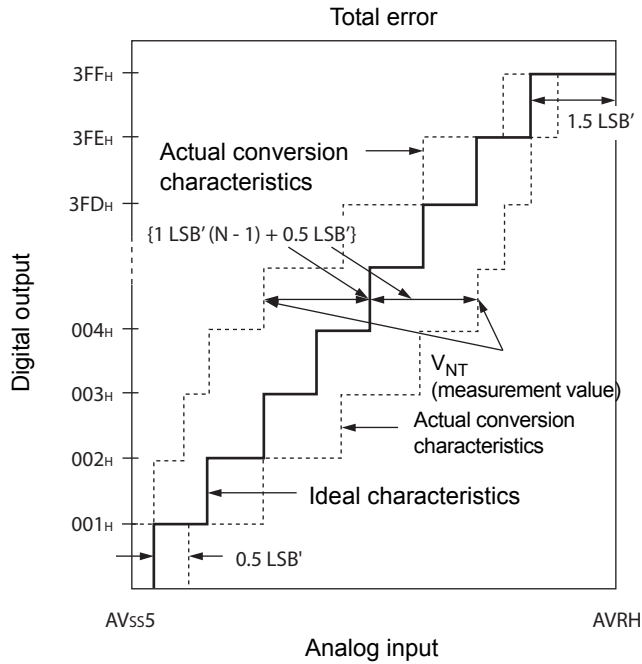
Total error

$$1\text{LSB' (ideal value)} = \frac{AVRH - AV_{SS}5}{1024} \ [V]$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ LSB' \times (N - 1) + 0.5\ LSB'\}}{1\ LSB'}$$

N: A/D converter digital output value
V_{OT}' (ideal value) $= AV_{SS}5 + 0.5\ LSB'$ [V]
V_{FST}' (ideal value) $= AVRH - 1.5\ LSB'$ [V]
V_{NT}: Voltage at which the digital output changes from $(N + 1)_H$ to N_H

Nonlinearity error

Differential nonlinearity error
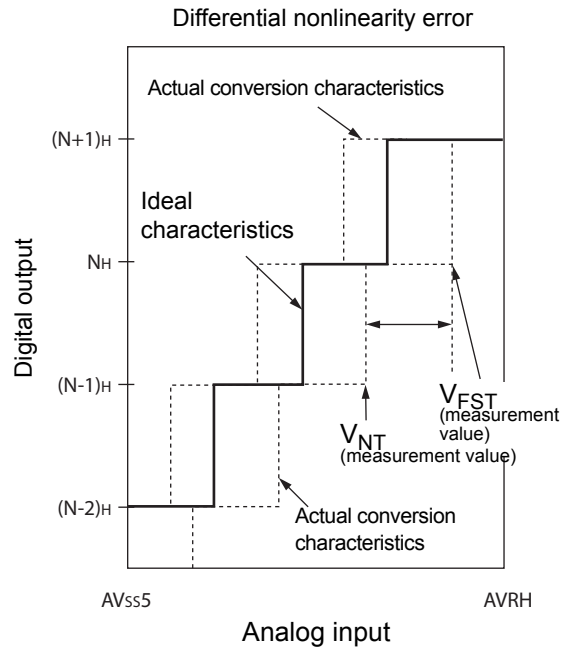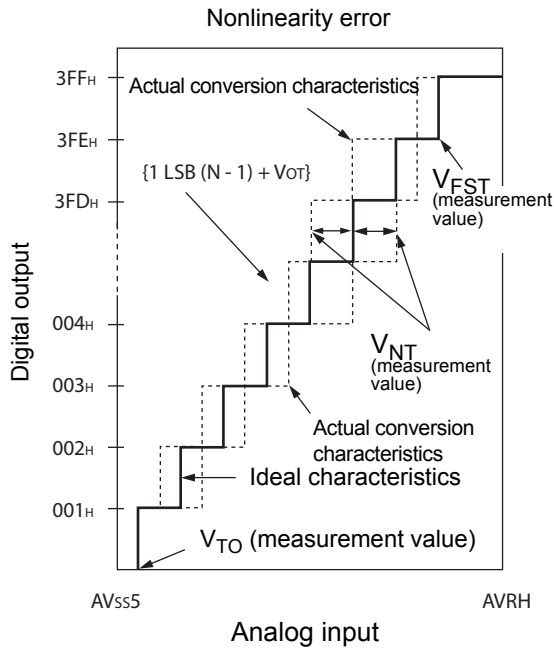
$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N-1) + V_{OT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

N: A/D converter digital output value
V_{OT}: Voltage at which the digital output changes from 000_H to 001_H.
V_{FST}: Voltage at which the digital output changes from $3FE_H$ to $3FF_H$.

15.5   Alarm Comparator Characteristics

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Power supply current	I_{A5ALMF}	$AV_{CC}5$	–	25	40	μA	Alarm comparator enabled in fast mode (per channel) [1]
	I_{A5ALMS}		–	7	10	μA	Alarm comparator enabled in normal mode (per channel) [1]
	I_{A5ALMH}		–	–	5	μA	Alarm comparator disabled
ALARM pin input current	I_{ALIN}	ALARM_n	– 1	–	+ 1	μA	T_A=25 °C
			– 3	–	+ 3	μA	T_A=125 °C
ALARM pin input voltage range	V_{ALIN}		0	–	$AV_{CC}5$	V	
Alarm upper limit voltage	V_{IAH}		$AV_{CC}5 \times 0.78 - 3\%$	$AV_{CC}5 \times 0.78$	$AV_{CC}5 \times 0.78 + 3\%$	V	
Alarm lower limit voltage	V_{IAL}		$AV_{CC}5 \times 0.36 - 5\%$	$AV_{CC}5 \times 0.36$	$AV_{CC}5 \times 0.36 + 5\%$	V	
Alarm hysteresis voltage	V_{IAHYS}		50	-	250	mV	
Alarm input resistance	R_{IN}		5	–	–	MΩ	
Comparion time	t_{COMPF}		–	0.1	0.2	μs	Alarm comparator enabled in fast mode [1]
	t_{COMPS}		–	1	2	μs	Alarm comparator enabled in normal mode [1]

1. The fast Alarm Comparator mode is enabled by setting ACSR.MD=1 Setting ACSR.MD=0 sets the normal mode.

15.6   Flash Memory Program/Erase Characteristics

15.6.1   MB91F467BA/466BA

($V_{DD}5 = 3.0$ V to 5.5 V, $V_{DD}5R = 3.0$ V to 5.5 V, $V_{SS}5 = 0$ V, $T_A = -40$ °C to $+105$ °C)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.5	2.0	s	Erasure programming time not included
Chip erase time	-	n*0.5	n*2.0	s	n is the number of Flash sector of the device
Word (16-bit width) programming time	-	6	100	μs	System overhead time not included
Program/Erase cycle	10 000			cycle	
Flash data retention time	20			year	[1]

1. This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85°C)

15.6.2   MB91F465BB/464BB

($V_{DD}5 = 3.0$ V to 5.5 V, $V_{DD}5R = 3.0$ V to 5.5 V, $V_{SS}5 = 0$ V, $T_A = -40$ °C to $+105$ °C)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.9	3.6	s	Erasure programming time not included
Chip erase time	-	n*0.9	n*3.6	s	n is the number of Flash sector of the device
Word (16-bit or 32-bit width) programming time	-	23	370	μs	System overhead time not included
Program/Erase cycle	10 000			cycle	
Flash data retention time	20			year	[1]

1. This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85°C)

15.7   AC Characteristics

15.7.1   Clock Timing

($V_{DD}5 = 3.0$ V to 5.5 V, Vss5 = AVss5 = 0 V, $T_A = -40$ °C to $+125$ °C)

Parameter	Symbol	Pin name	Value			Unit	Condition
			Min	Typ	Max		
Clock frequency	f_C	X0 X1	3.5	4	16	MHz	Opposite phase external supply or crystal
		X0A X1A	32	32.768	100	kHz	

Figure 3. Clock timing condition
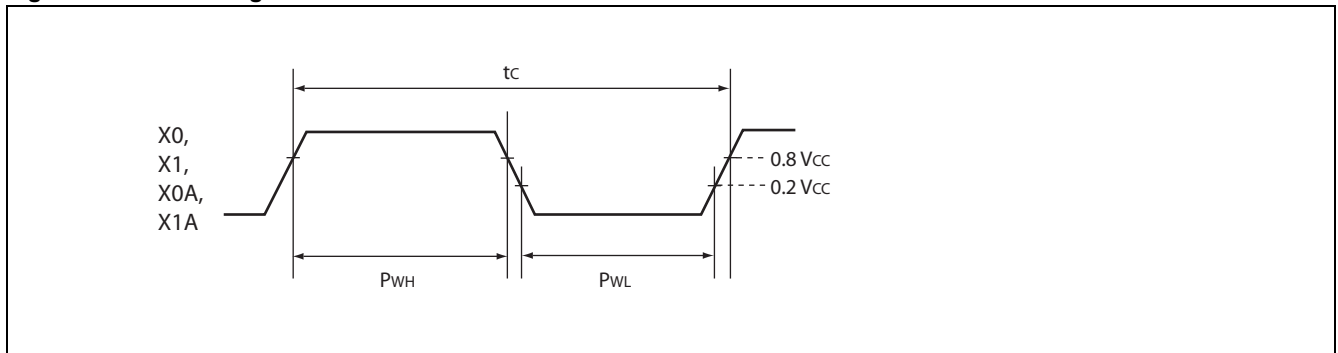
15.7.2   Reset Input Ratings

($V_{DD}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40$ °C to $+125$ °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
INITX input time (at power-on)	t_{INTL}	INITX	–	8	–	ms
INITX input time (other than the above)				20	–	μs
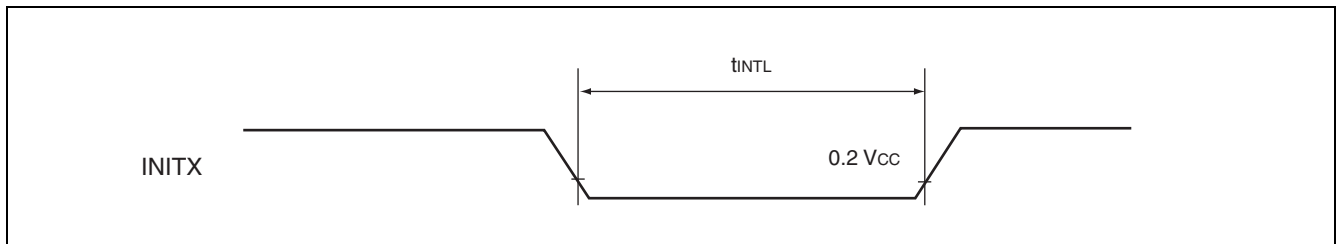
15.7.3 LIN-USART Timings at $V_{DD}5$ = 3.0 to 5.5 V

■ Conditions during AC measurements

■ All AC tests were measured under the following conditions:

  ❏ - IO_{drive} = 5 mA
  ❏ - $V_{DD}5$ = 3.0 V to 5.5 V, I_{load} = 3 mA
  ❏ - $V_{SS}5$ = 0 V
  ❏ - T_a = -40 °C to +125× °C
  ❏ - C_I = 50 pF (load capacity value of pins when testing)
  ❏ - VOL = 0.2 x $V_{DD}5$
  ❏ - VOH = 0.8 x $V_{DD}5$
  ❏ - EPILR = 0, PILR = 1 (Automotive Level = worst case)

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = −40 °C to + 125 °C)

Parameter	Symbol	Pin name	Condition	$V_{DD}5$ = 3.0 V to 4.5 V		$V_{DD}5$ = 4.5 V to 5.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYCI}	SCKn		4 t_{CLKP}	-	4 t_{CLKP}	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKn SOTn		- 30	30	- 20	20	ns
SOT → SCK ↓ delay time	t_{OVSHI}	SCKn SOTn	Internal clock operation (master mode)	m × t_{CLKP} - 30[1]	-	m × t_{CLKP} - 20[1]	-	ns
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCKn SINn		t_{CLKP} + 55	-	t_{CLKP} + 45	-	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}	SCKn SINn		0	-	0	-	ns
Serial clock "H" pulse width	t_{SHSLE}	SCKn		t_{CLKP} + 10	-	t_{CLKP} + 10	-	ns
Serial clock"L" pulse width	t_{SLSHE}	SCKn		t_{CLKP} + 10	-	t_{CLKP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKn SOTn	External clock operation (slave mode)	-	2 t_{CLKP} + 55	-	2 t_{CLKP} + 45	ns
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCKn SINn		10	-	10	-	ns
SCK ↑ → valid SIN hold time	t_{SHIXE}	SCKn SINn		t_{CLKP} + 10	-	t_{CLKP} + 10	-	ns
SCK rising time	t_{FE}	SCKn		-	20	-	20	ns
SCK falling time	t_{RE}	SCKn		-	20	-	20	ns

1. Parameter m depends on t_{SCYCI} and can be calculated as :

■ if t_{SCYCI} = 2*k*t_{CLKP}, then m = k, where k is an integer > 2

■ if t_{SCYCI} = (2*k + 1)*t_{CLKP}, then m = k + 1, where k is an integer > 1

Notes :

■ The above values are AC characteristics for CLK synchronous mode.

■ t_{CLKP} is the cycle time of the peripheral clock.

Figure 4. Internal Clock Mode (Master Mode)
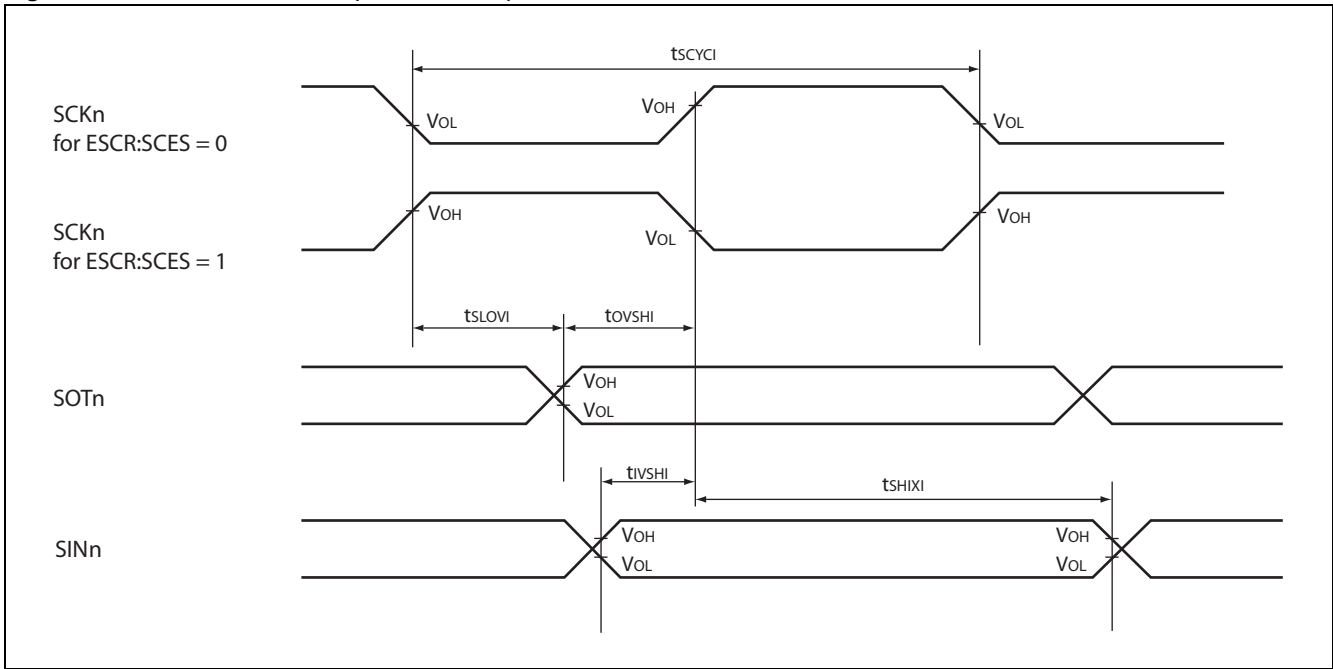
Figure 5. External Clock Mode (Slave Mode)
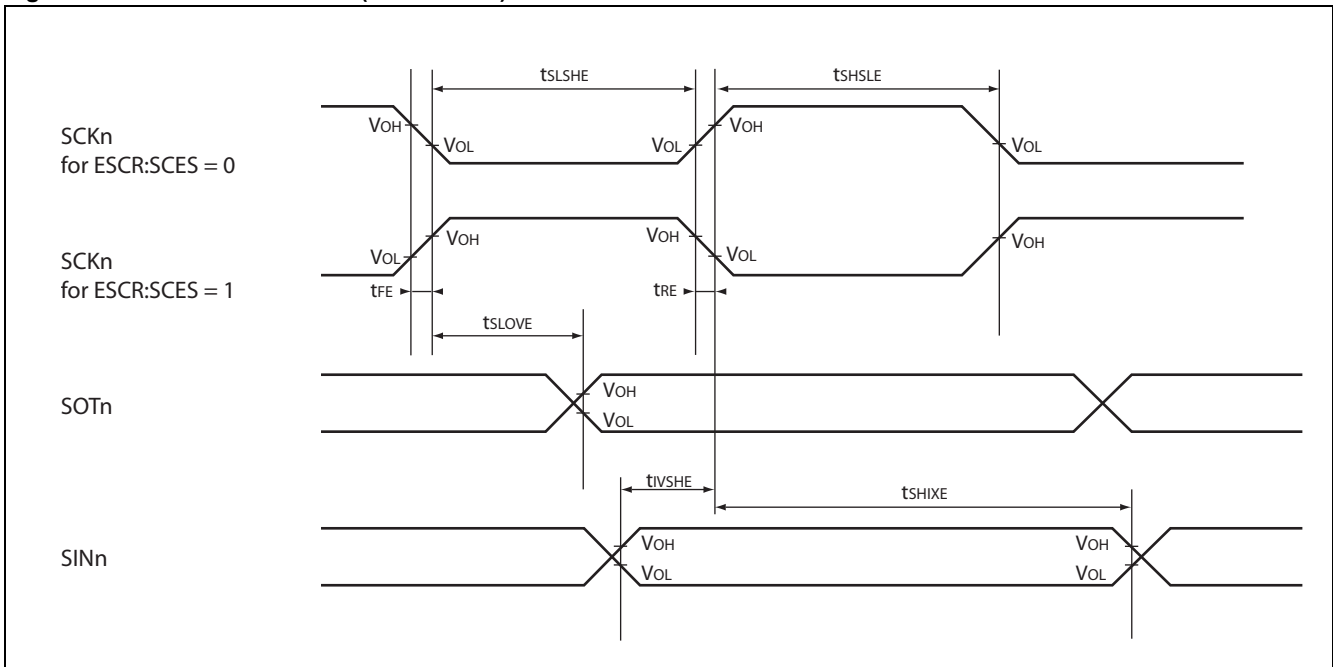
15.7.4 I ^{2}C AC Timings at V$_{DD}$5 = 3.0 to 5.5 V

■ Conditions during AC measurements
  All AC tests were measured under the following conditions:
  ❏ -IO$_{drive}$ = 3 mA
  ❏ -V$_{DD}$5 = 3.0 V to 5.5 V, I$_{load}$ = 3 mA
  ❏ -V$_{SS}$5 = 0 V
  ❏ -Ta = - 40 °C to + 125 °C
  ❏ -C$_I$ = 50 pF
  ❏ -VOL = 0.3 × V$_{DD}$5
  ❏ -VOH = 0.7 × V$_{DD}$5
  ❏ -EPILR = 0, PILR = 0 (CMOS Hysteresis 0.3 × V$_{DD}$5/0.7 × V$_{DD}$5)

15.7.4.1 Fast mode:

(V$_{DD}$5 = 3.5 V to 5.5 V, V$_{SS}$5 = AV$_{SS}$5 = 0 V, T$_A$ = −40 °C to + 125 °C)

Parameter	Symbol	Pin name	Value		Unit	Remark
			Min	Max		
SCL clock frequency	f$_{SCL}$	SCLn	0	400	kHz	
Hold time (repeated) START condition. After this period, the first clock pulse is generated	t$_{HD;STA}$	SCLn, SDAn	0.6	–	μs	
LOW period of the SCL clock	t$_{LOW}$	SCLn	1.3	–	μs	
HIGH period of the SCL clock	t$_{HIGH}$	SCLn	0.6	–	μs	
Setup time for a repeated START condition	t$_{SU;STA}$	SCLn, SDAn	0.6	–	μs	
Data hold time for I^{2}C-bus devices	t$_{HD;DAT}$	SCLn, SDAn	0	0.9	μs	
Data setup time	t$_{SU;DAT}$	SCLn SDAn	100	–	ns	
Rise time of both SDA and SCL signals	t$_r$	SCLn, SDAn	20 + 0.1Cb	300	ns	
Fall time of both SDA and SCL signals	t$_f$	SCLn, SDAn	20 + 0.1Cb	300	ns	
Setup time for STOP condition	t$_{SU;STO}$	SCLn, SDAn	0.6	–	μs	
Bus free time between a STOP and START condition	t$_{BUF}$	SCLn, SDAn	1.3	–	μs	
Capacitive load for each bus line	C$_b$	SCLn, SDAn	–	400	pF	
Pulse width of spike suppressed by input filter	t$_{SP}$	SCLn, SDAn	0	(1..1.5) × t$_{CLKP}$	ns	[1]

1. The noise filter will suppress single spikes with a pulse width of 0ns and between (1 to 1.5) cycles of peripheral clock, depending on the phase relationship between I^{2}C signals (SDA, SCL) and peripheral clock.

Note: t$_{CLKP}$ is the cycle time of the peripheral clock.
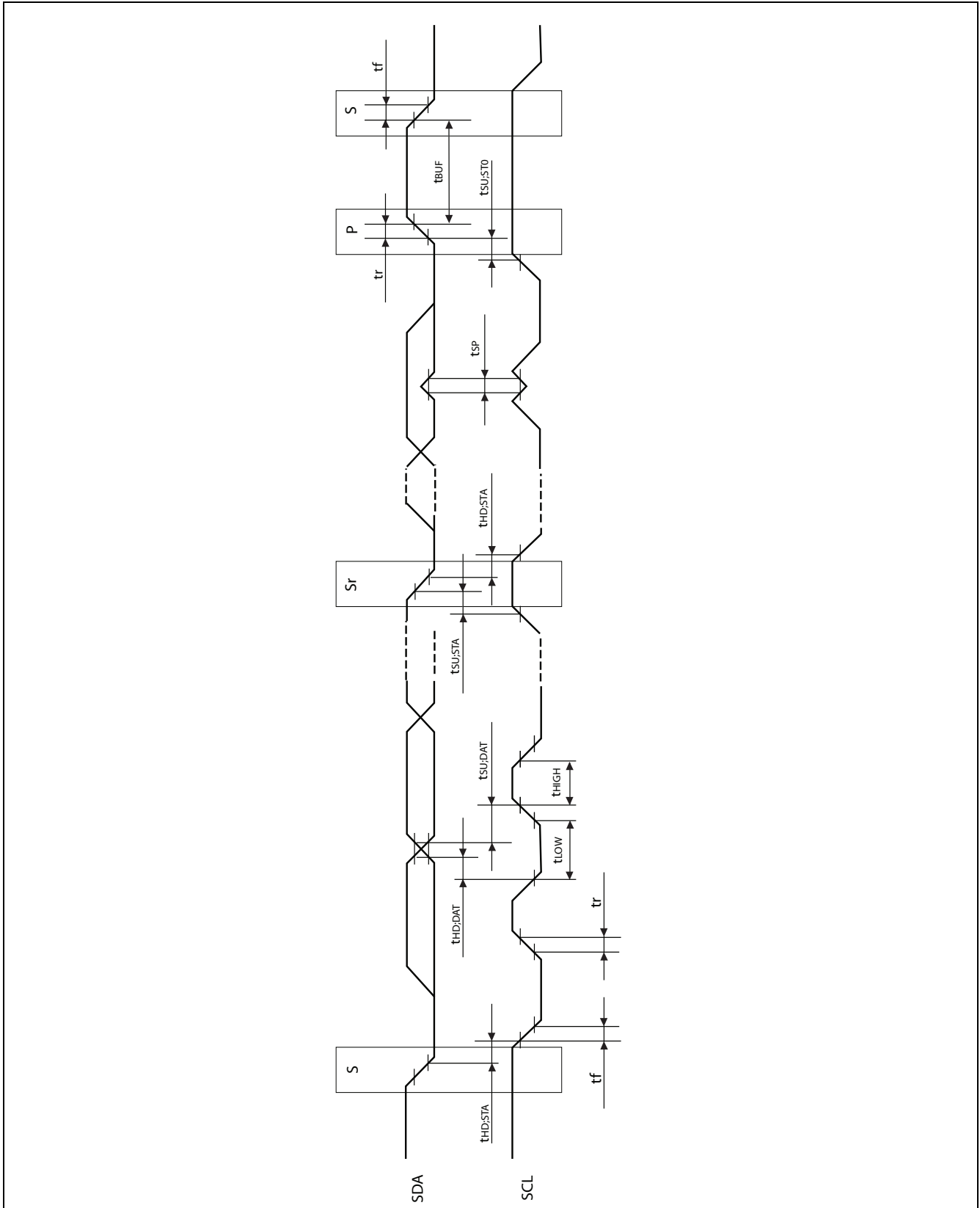
15.7.5   Free-Run Timer Clock

($V_{DD}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40$ °C to $+125$ °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	**Max**	
Input pulse width	t_{TIWH} t_{TIWL}	CKn	–	$4t_{CLKP}$	–	ns

Note: t_{CLKP} is the cycle time of the peripheral clock.
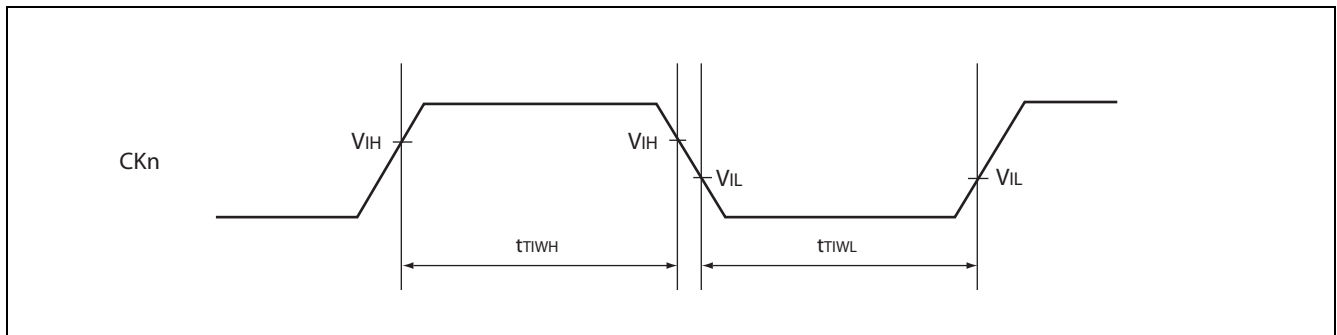
15.7.6   Trigger Input Timing

($V_{DD}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40$ °C to $+125$ °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	**Max**	
Input capture input trigger	t_{INP}	ICUn	–	$5t_{CLKP}$	–	ns
A/D converter trigger	t_{ATGX}	ATGX	–	$5t_{CLKP}$	–	ns

Note: t_{CLKP} is the cycle time of the peripheral clock.
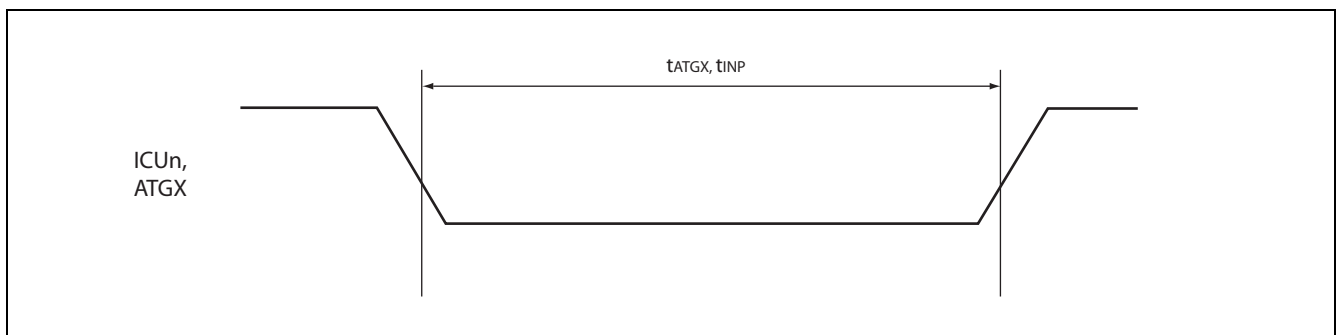
15.7.7 External Bus AC Timings at $V_{DD}35 = 3.0$ to 5.5 V

Note: This chapter is applicable to MB91F467BA/F466BA

■ Conditions during AC measurements
All AC tests were measured under the following conditions:

❏ -$IO_{drive} = 5$ mA
❏ -$V_{DD}35 = 4.5$ V to 5.5 V, $I_{load} = 3$ mA
❏ -$V_{SS}5 = 0$ V
❏ -$Ta = -40$ °C to $+125$ °C
❏ -$C_I = 50$ pF
❏ -$VOL = 0.5 \times V_{DD}35$
❏ -$VOH = 0.5 \times V_{DD}35$
❏ -$EPILR = 0$, $PILR = 1$ (Automotive Level = worst case)

15.7.7.1 Basic Timing

($V_{DD}35 = 3.0$ V to 5.5 V, $Vss5 = AVss5 = 0$ V, $T_A = -40$ °C to $+125$ °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK	t_{CLCH}	SYSCLK	$1/2 \times t_{CLKT} - 1$	$1/2 \times t_{CLKT} + 9$	ns
	t_{CHCL}		$1/2 \times t_{CLKT} - 9$	$1/2 \times t_{CLKT} + 1$	ns
SYSCLK ↓ to CSXn delay time	t_{CLCSL}	SYSCLK CSXn	-	8	ns
	t_{CLCSH}		-	12	ns
SYSCLK ↑ to CSXn delay time (Addr → CS delay)	t_{CHCSL}		- 6	+ 1	ns
SYSCLK ↓ to Address valid delay time	t_{CLAV}	SYSCLK A21 to A0	-	13	ns

Note: t_{CLKT} is the cycle time of the external bus clock.
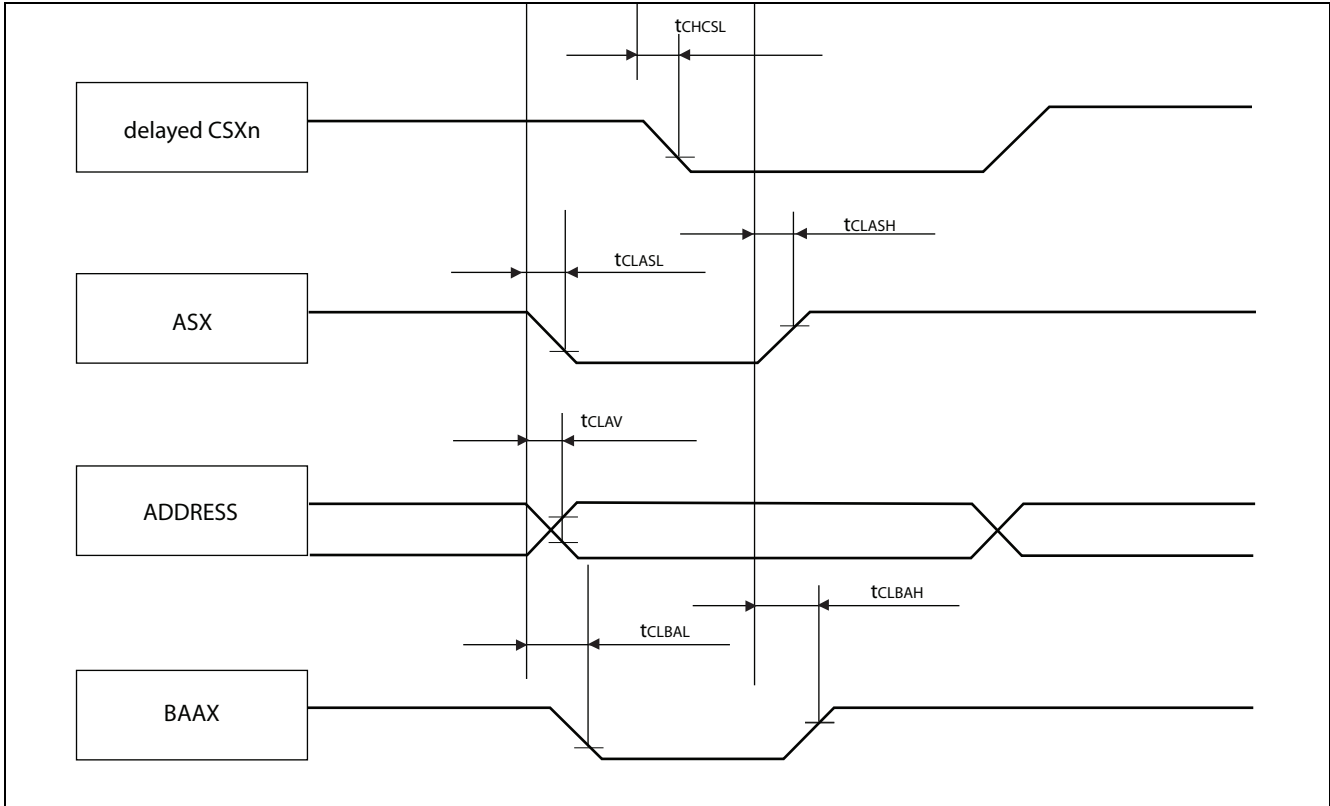
15.7.7.2 Synchronous/Asynchronous Read Access

($V_{DD}35 = 3.0$ V to 5.5 V, Vss5 = AVss5 = 0 V, $T_A = -40$ °C to $+125$ °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK ↑ to RDX delay time	TCHRL	SYSCLK RDX	- 7	1	ns
	TCHRH		- 4	2	ns
Data valid to RDX ↑ setup time	TDSRH	RDX D31 to D16	33	-	ns
RDX ↑ to Data valid hold time	TRHDX	RDX D31 to D16	0	-	ns
SYSCLK ↓ to WRXn (as byte enable) delay time	TCLWRL	SYSCLK WRXn	-	8	ns
	TCLWRH		0	-	ns
SYSCLK ↓ to CSXn delay time	TCLCSL	SYSCLK CSXn	-	8	ns
	TCLCSH		-	12	ns
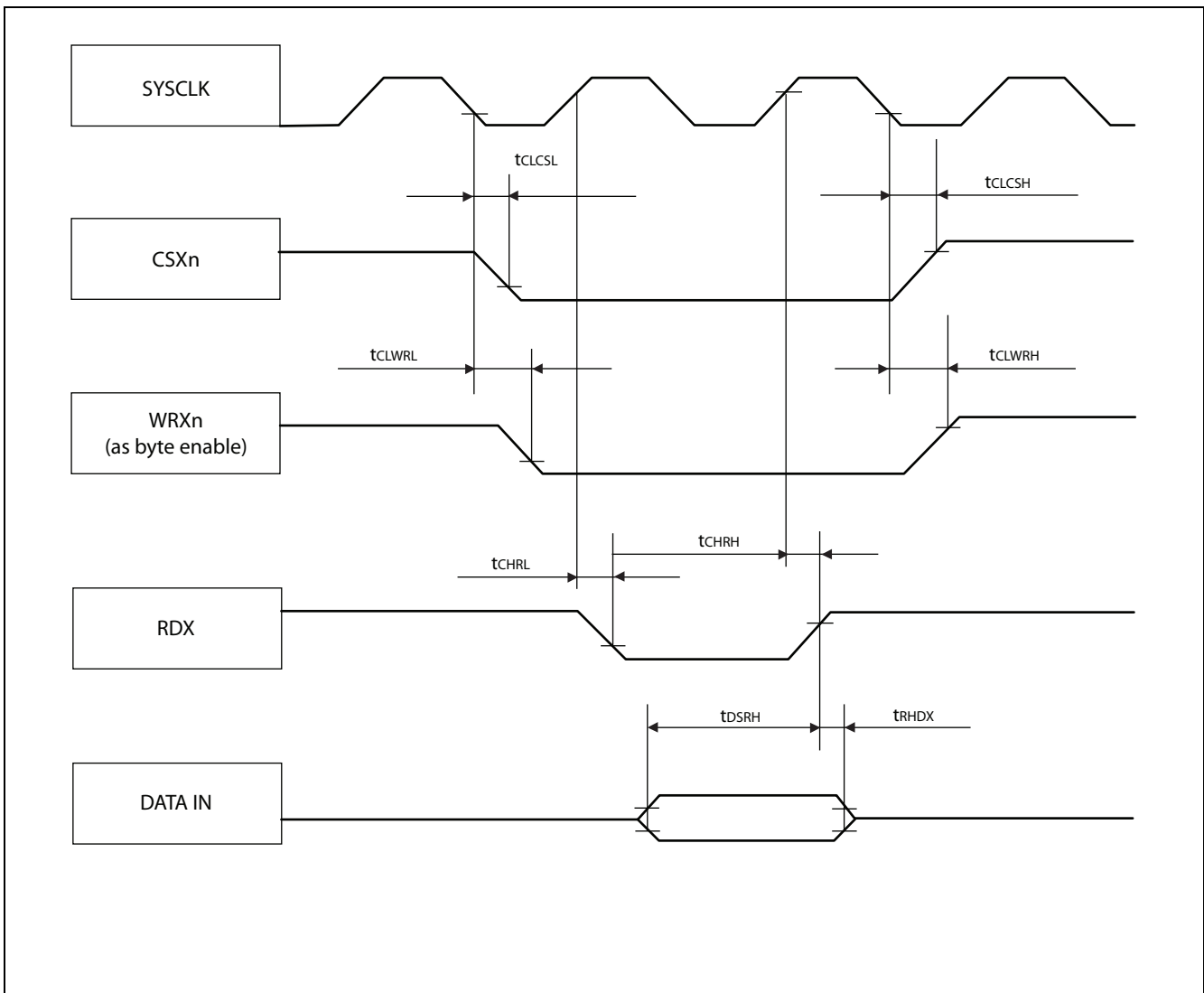
15.7.7.3   Synchronous write access

$(V_{DD}35 = 3.0 \text{ V to } 5.5 \text{ V}, Vss5 = AVss5 = 0 \text{ V}, T_A = -40 °C \text{ to } +125 °C)$

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK ↓ to WRXn delay time	TCLWRL	SYSCLK WRXn	-	8	ns
	TCLWRH		0	-	ns
Data valid to WRXn ↓ setup time	TDSWRL	WRXn D31 to D16	- 7	-	ns
WRXn ↑ to Data valid hold time	TWRHDH	WRXn D31 to D16	t_{CLKT} - 20	-	ns
SYSCLK ↓ to CSXn delay time	TCLCSL	SYSCLK CSXn	-	8	ns
	TCLCSH		-	12	ns
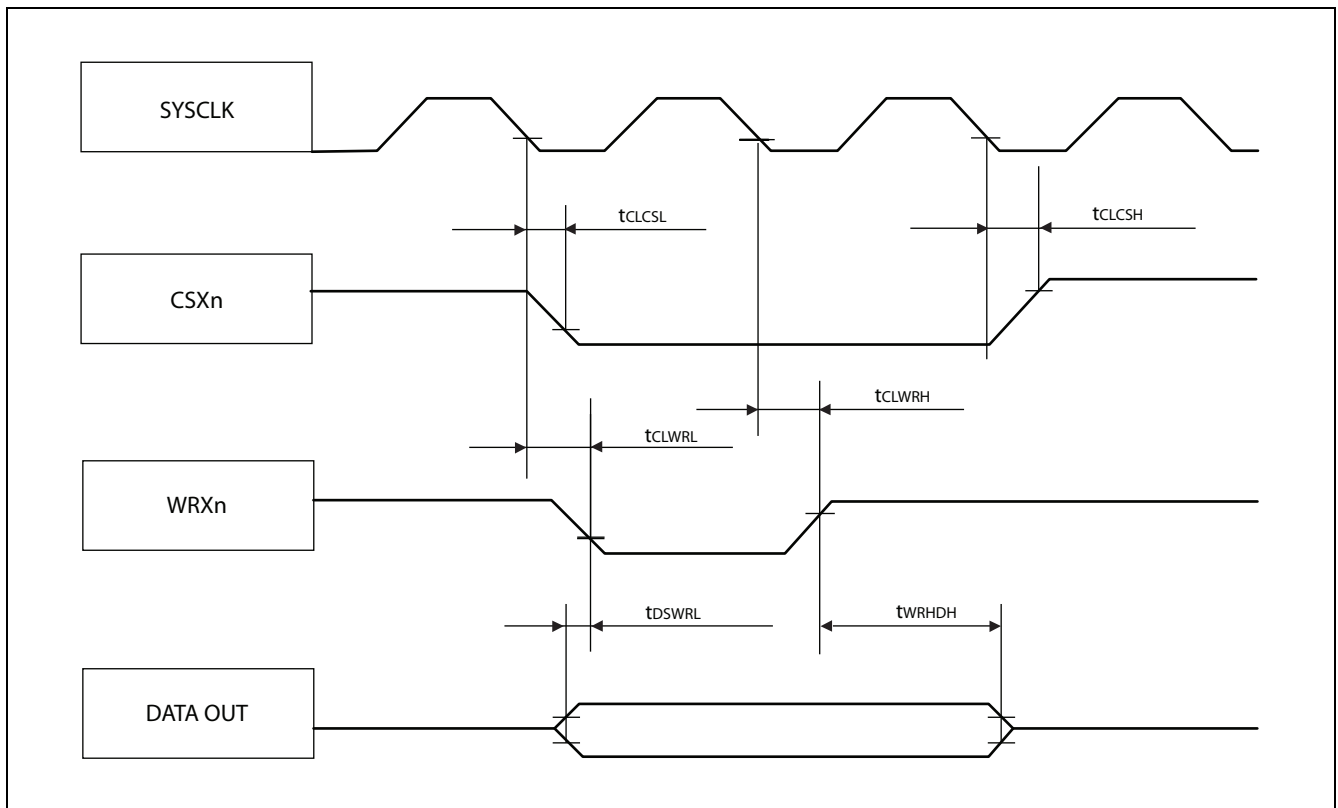
15.7.7.4 Asynchronous Write Access

($V_{DD}35 = 3.0$ V to 5.5 V, Vss5 = AVss5 = 0 V, $T_A = -40$ °C to $+125$ °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	**Max**	
WRXn ↓ to WRXn ↑ pulse width	TWRLWRH	WRXn	t_{CLKT}	-	ns
Data valid to WRXn ↓ setup time	TDSWRL	WRXn D31 to D16	$1/2 \times t_{CLKT} - 10$	-	ns
WRXn ↑ to Data valid hold time	TWRHDH	WRXn D31 to D16	$1/2 \times t_{CLKT} - 19$	-	ns
WRXn to CSXn delay time	TCLWRL	WRXn CSXn	-	$1/2 \times t_{CLKT}$	ns
	TWRHCH		$1/2 \times t_{CLKT}$	-	ns
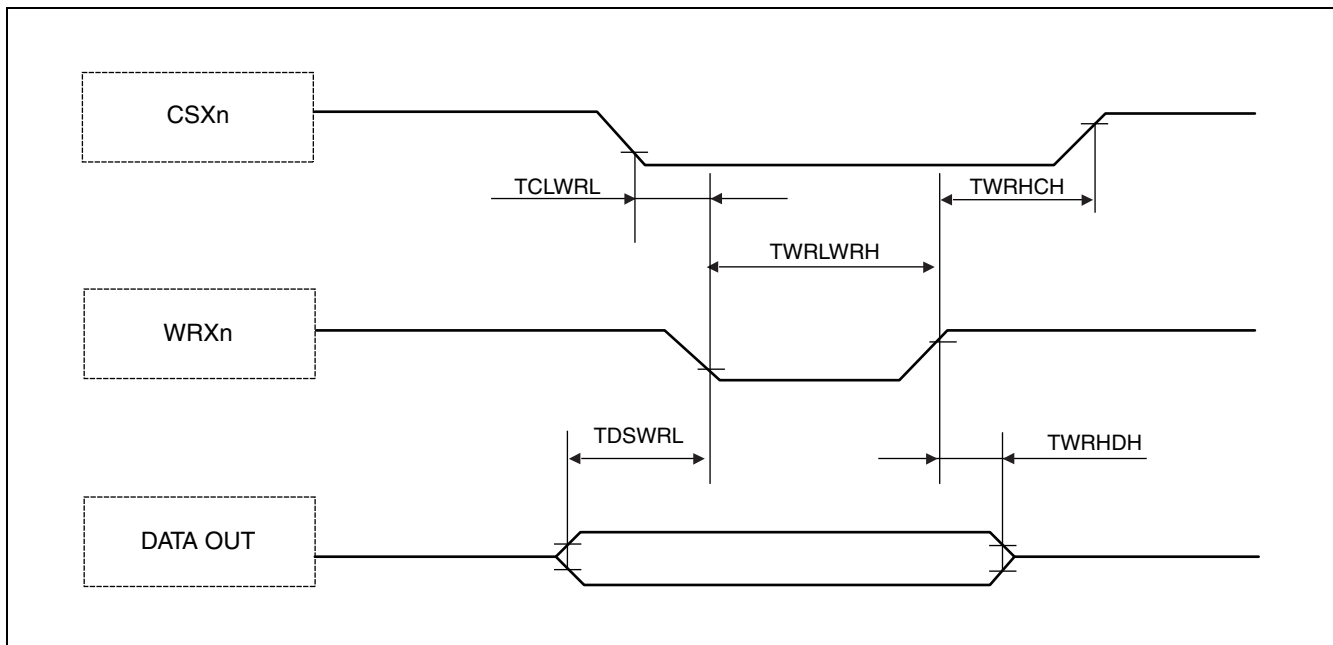
15.7.7.5 RDY Waitcycle Insertion

($V_{DD}35 = 3.0$ V to 5.5 V, Vss5 = AVss5 = 0 V, $T_A = -40$ °C to $+125$ °C)
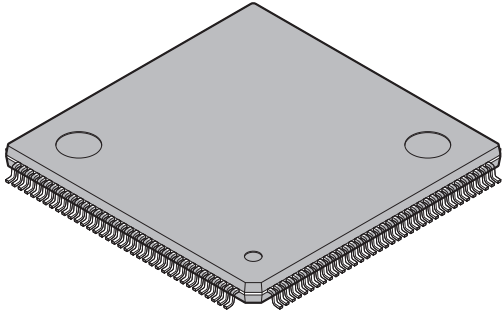
Parameter	Symbol	Pin name	Value		Unit
			Min	**Max**	
RDY setup time	TRDYS	SYSCLK RDY	34	–	ns
RDY hold time	TRDYH	SYSCLK RDY	0	–	ns
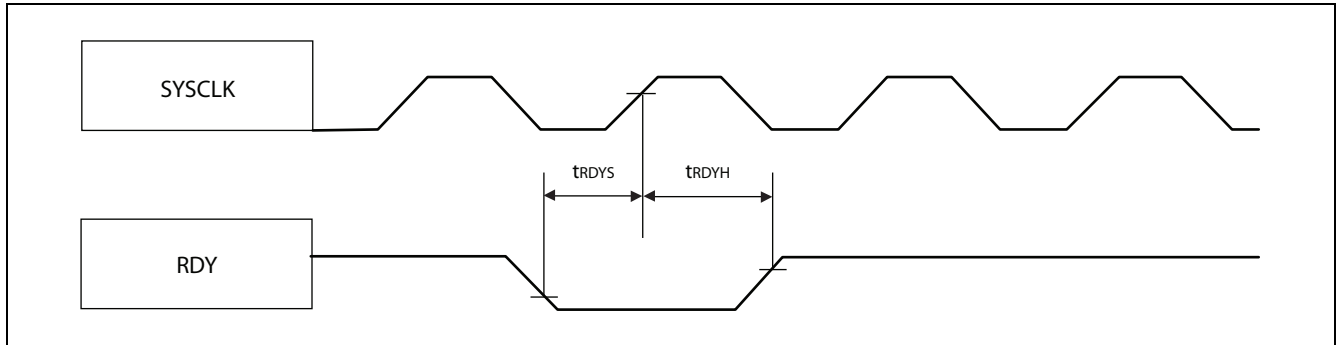
16. Ordering Information

Part number	Package	Remarks
MB91F465BBPMC-GSE2 MB91F467BAPMC-GSE2	144-pin plastic LQFP (FPT-144P-M08)	Lead-free package

17. Package Dimension

144-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	20.0 × 20.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	1.20g
(FPT-144P-M08)	Code (Reference)	P-LFQFP144-20×20-0.50

144-pin plastic LQFP
(FPT-144P-M08)

Note 1) *:Values do not include resin protrusion.
Resin protrusion is +0.25(.010)Max(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

22.00±0.20(.866±.008)SQ

* 20.00±0.10(.787±.004)SQ

108   73
109   72
144   37
LEAD No. 1   36

INDEX

0.50(.020)

0.22±0.05
(.009±.002)   ⊕ 0.08(.003) Ⓜ

©2003-2008 FUJITSU MICROELECTRONICS LIMITED F144019S-c-4-7

0.145±0.055
(.006±.002)

▱ 0.08(.003)

"A"

Details of "A" part

1.50 $^{+0.20}_{-0.10}$ (Mounting height)
(.059 $^{+.008}_{-.004}$)

0.10±0.10
(.004±.004)
(Stand off)

0°~8°

0.25(.010)

0.50±0.20
(.020±.008)

0.60±0.15
(.024±.006)

Dimensions in mm (inches).
Note: The values in parentheses are reference values.

18. Revision History

Spansion Publication Number: DS07-16609-1E

Version	Date	Remark
2.0	2008-06-19	Initial version
2.1	2008-08-15	Proof reading results from FJ incorporated; Corrected pinout drawings; IO CIRCUIT TYPES: corrected some typos like on the other datasheets; HANDLING DEVICES: updated the section "Notes on PS register" for better understanding; Interrupt Vector Table: corrected the footnotes FLASH: added note about the operation mode switching capability in Boot ROM; corrected flash security vector FSV2 assignments, corrected section about parallel programming, corrected section pin connections in parallel programming mode so that there is only one page added section "Poweron Sequence in parallel programming mode"; ELECTRICAL CHARACTERISTICS: removed the note that analog input/output pins cannot accept +B signal input; splitted I_{LV} into external and internal LV detection current ADC Characteristics: Corrected the items about nonlinearity error; Corrected the company name
3.0	2009-01-09	Page 1: Corrected document name field in top header Block Diagram: Removed SCK0 (LIN-USART0 is asynchronous only) Added Ta=125C characteristics

19. Main Changes in this Edition

Page	Section	Change Results
104	15. Electrical Characteristics 15.4. A/D converter characteristics	Corrected the column "Value" and "Unit" of the parameter "Zero reading voltage" and "Full scale reading voltage". (Value : AVRL - 1.5 → AVRL - 1.5 LSB AVRL + 0.5 → AVRL + 0.5 LSB AVRL + 2.5 → AVRL + 2.5 LSB AVRH - 3.5 → AVRH - 3.5 LSB AVRH - 1.5 → AVRH - 1.5 LSB AVRH + 0.5 → AVRH + 0.5 LSB Unit : LSB → V)

NOTE: Please see "Document History" for later revised information.

Document History

Document Title: MB91F467BA/466BA, MB91F465BB/464BB, FR60 MB91460B Series, 32-bit Microcontroller Datasheet Document Number: 002-04608				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	08/17/2009	Migrated to Cypress and assigned document number 002-04608. No change to document contents or format.
*A	5221423	AKIH	04/25/2016	Updated to Cypress template

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products		**PSoC®Solutions**
ARM® Cortex® Microcontrollers	cypress.com/arm	PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP
Automotive	cypress.com/automotive	
Clocks & Buffers	cypress.com/clocks	**Cypress Developer Community**
Interface	cypress.com/interface	Forums | Projects | Video | Blogs | Training | Components
Lighting & Power Control	cypress.com/powerpsoc	
Memory	cypress.com/memory	**Technical Support**
PSoC	cypress.com/psoc	cypress.com/support
Touch Sensing	cypress.com/touch	
USB Controllers	cypress.com/usb	
Wireless/RF	cypress.com/wireless	

ARM and Cortex are the trademarks of ARM Limited in the EU and other countries