

NGB18N40CLB, NGB18N40ACLB

Ignition IGBT 18 Amps, 400 Volts N-Channel D²PAK

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features monolithic circuitry integrating ESD and Over-Voltage clamped protection for use in inductive coil drivers applications. Primary uses include Ignition, Direct Fuel Injection, or wherever high voltage and high current switching is required.

Features

- Ideal for Coil-on-Plug Applications
- Gate-Emitter ESD Protection
- Temperature Compensated Gate-Collector Voltage Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- New Design Increases Unclamped Inductive Switching (UIS) Energy Per Area
- Low Threshold Voltage to Interface Power Loads to Logic or Microprocessor Devices
- Low Saturation Voltage
- High Pulsed Current Capability
- Integrated Gate-Emitter Resistor (R_{GE})
- Emitter Ballasting for Short-Circuit Capability
- These are Pb-Free Devices

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|----------------|-------------|--------------------------|
| Collector-Emitter Voltage | V_{CES} | 430 | V_{DC} |
| Collector-Gate Voltage | V_{CER} | 430 | V_{DC} |
| Gate-Emitter Voltage | V_{GE} | 18 | V_{DC} |
| Collector Current-Continuous @ $T_C = 25^\circ\text{C}$ - Pulsed | I_C | 18 50 | A_{DC} A_{AC} |
| ESD (Human Body Model) $R = 1500 \Omega$, $C = 100 \text{ pF}$ | ESD | 8.0 | kV |
| ESD (Machine Model) $R = 0 \Omega$, $C = 200 \text{ pF}$ | ESD | 800 | V |
| Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C | P_D | 115 0.77 | W W/ $^\circ\text{C}$ |
| Operating and Storage Temperature Range | T_J, T_{stg} | -55 to +175 | $^\circ\text{C}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

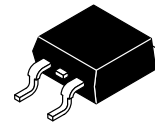
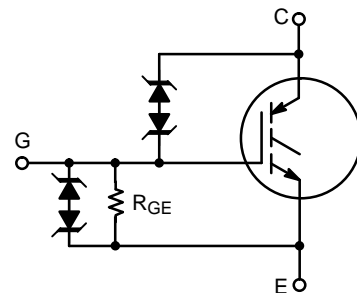


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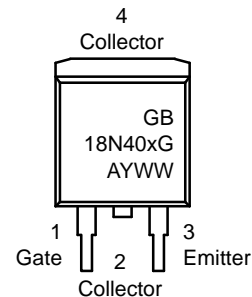
18 AMPS, 400 VOLTS

$V_{CE(on)} \leq 2.0 \text{ V @}$
 $I_C = 10 \text{ A}, V_{GE} \geq 4.5 \text{ V}$



D²PAK
CASE 418B
STYLE 4

MARKING DIAGRAM



GB18N40x = Device Code
x = B or A
A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

| Device | Package | Shipping† |
|-----------------|--------------------|-----------------|
| NGB18N40CLBT4G | D ² PAK | 800/Tape & Reel |
| NGB18N40ACLBT4G | (Pb-Free) | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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UNCLAMPED COLLECTOR-TO-EMITTER AVALANCHE CHARACTERISTICS ($-55^{\circ} \leq T_J \leq 175^{\circ}C$)

| Characteristic | Symbol | Value | Unit |
|---|-------------|------------|------|
| Single Pulse Collector-to-Emitter Avalanche Energy $V_{CC} = 50\text{ V}$, $V_{GE} = 5.0\text{ V}$, Pk $I_L = 21.1\text{ A}$, $L = 1.8\text{ mH}$, Starting $T_J = 25^{\circ}C$ $V_{CC} = 50\text{ V}$, $V_{GE} = 5.0\text{ V}$, Pk $I_L = 18.3\text{ A}$, $L = 1.8\text{ mH}$, Starting $T_J = 125^{\circ}C$ | E_{AS} | 400 300 | mJ |
| Reverse Avalanche Energy $V_{CC} = 100\text{ V}$, $V_{GE} = 20\text{ V}$, Pk $I_L = 25.8\text{ A}$, $L = 6.0\text{ mH}$, Starting $T_J = 25^{\circ}C$ | $E_{AS(R)}$ | 2000 | mJ |

MAXIMUM SHORT-CIRCUIT TIMES ($-55^{\circ}C \leq T_J \leq 150^{\circ}C$)

| Characteristic | Symbol | Value | Unit |
|--|-----------|-------|---------|
| Short Circuit Withstand Time 1 (See Figure 17, 3 Pulses with 10 ms Period) | t_{sc1} | 750 | μs |
| Short Circuit Withstand Time 2 (See Figure 18, 3 Pulses with 10 ms Period) | t_{sc2} | 5.0 | ms |

THERMAL CHARACTERISTICS

| Characteristic | Symbol | Value | Unit |
|---|-----------------|-------|---------------|
| Thermal Resistance, Junction-to-Case | $R_{\theta JC}$ | 1.3 | $^{\circ}C/W$ |
| Thermal Resistance, Junction-to-Ambient D ² PAK (Note 1) | $R_{\theta JA}$ | 50 | $^{\circ}C/W$ |
| Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds | T_L | 275 | $^{\circ}C$ |

ELECTRICAL CHARACTERISTICS

| Characteristic | Symbol | Test Conditions | Temperature | Min | Typ | Max | Unit |
|----------------|--------|-----------------|-------------|-----|-----|-----|------|
|----------------|--------|-----------------|-------------|-----|-----|-----|------|

OFF CHARACTERISTICS

| | | | | | | | |
|---|---------------|--|--|-----|-----|----------|------------|
| Collector-Emitter Clamp Voltage | BV_{CES} | $I_C = 2.0\text{ mA}$ | $T_J = -40^{\circ}C$ to $150^{\circ}C$ | 380 | 395 | 420 | V |
| | | $I_C = 10\text{ mA}$ | $T_J = -40^{\circ}C$ to $150^{\circ}C$ | 390 | 405 | 430 | |
| Zero Gate Voltage Collector Current | I_{CES} | $V_{CE} = 350\text{ V}$, $V_{GE} = 0\text{ V}$ | $T_J = 25^{\circ}C$ | - | 2.0 | 20 | μA |
| | | | $T_J = 150^{\circ}C$ | - | 10 | 40* | |
| | | | $T_J = -40^{\circ}C$ | - | 1.0 | 10 | |
| Reverse Collector-Emitter Leakage Current | I_{ECS} | $V_{CE} = -24\text{ V}$ | $T_J = 25^{\circ}C$ | - | 0.7 | 2.0 | mA |
| | | | $T_J = 150^{\circ}C$ | - | 12 | 25* | |
| | | | $T_J = -40^{\circ}C$ | - | 0.1 | 1.0 | |
| Reverse Collector-Emitter Clamp Voltage | $BV_{CES(R)}$ | $I_C = -75\text{ mA}$ | $T_J = 25^{\circ}C$ | 27 | 33 | 37 | V |
| | | | $T_J = 150^{\circ}C$ | 30 | 36 | 40 | |
| | | | $T_J = -40^{\circ}C$ | 25 | 32 | 35 | |
| Gate-Emitter Clamp Voltage | BV_{GES} | $I_G = 5.0\text{ mA}$ | $T_J = -40^{\circ}C$ to $150^{\circ}C$ | 11 | 13 | 15 | V |
| Gate-Emitter Leakage Current | I_{GES} | $V_{GE} = 10\text{ V}$ | $T_J = -40^{\circ}C$ to $150^{\circ}C$ | 384 | 640 | 100 0 | μA |
| Gate Emitter Resistor | R_{GE} | - | $T_J = -40^{\circ}C$ to $150^{\circ}C$ | 10 | 16 | 26 | k Ω |

ON CHARACTERISTICS (Note 2)

| | | | | | | | |
|--|--------------|--|----------------------|------|-----|------|-----------------|
| Gate Threshold Voltage | $V_{GE(th)}$ | $I_C = 1.0\text{ mA}$, $V_{GE} = V_{CE}$ | $T_J = 25^{\circ}C$ | 1.1 | 1.4 | 1.9 | V |
| | | | $T_J = 150^{\circ}C$ | 0.75 | 1.0 | 1.4 | |
| | | | $T_J = -40^{\circ}C$ | 1.2 | 1.6 | 2.1* | |
| Threshold Temperature Coefficient (Negative) | - | - | - | - | 3.4 | - | mV/ $^{\circ}C$ |

*Maximum Value of Characteristic across Temperature Range.

- When surface mounted to an FR4 board using the minimum recommended pad size.
- Pulse Test: Pulse Width $\leq 300\ \mu s$, Duty Cycle $\leq 2\%$.

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ELECTRICAL CHARACTERISTICS

| Characteristic | Symbol | Test Conditions | Temperature | Min | Typ | Max | Unit |
|------------------------------------|--------------|---|---|-----|------|------|------|
| ON CHARACTERISTICS (Note 2) | | | | | | | |
| Collector-to-Emitter On-Voltage | $V_{CE(on)}$ | $I_C = 6.0 \text{ A}, V_{GE} = 4.0 \text{ V}$ | $T_J = 25^\circ\text{C}$ | 1.0 | 1.4 | 1.6 | V |
| | | | $T_J = 150^\circ\text{C}$ | 0.9 | 1.3 | 1.6 | |
| | | | $T_J = -40^\circ\text{C}$ | 1.1 | 1.45 | 1.7* | |
| | | $I_C = 8.0 \text{ A}, V_{GE} = 4.0 \text{ V}$ | $T_J = 25^\circ\text{C}$ | 1.3 | 1.6 | 1.9* | |
| | | | $T_J = 150^\circ\text{C}$ | 1.2 | 1.55 | 1.8 | |
| | | | $T_J = -40^\circ\text{C}$ | 1.4 | 1.6 | 1.9* | |
| | | $I_C = 10 \text{ A}, V_{GE} = 4.0 \text{ V}$ | $T_J = 25^\circ\text{C}$ | 1.4 | 1.8 | 2.05 | |
| | | | $T_J = 150^\circ\text{C}$ | 1.5 | 1.8 | 2.0 | |
| | | | $T_J = -40^\circ\text{C}$ | 1.4 | 1.8 | 2.1* | |
| | | $I_C = 15 \text{ A}, V_{GE} = 4.0 \text{ V}$ | $T_J = 25^\circ\text{C}$ | 1.6 | 1.9 | 2.2 | |
| | | | $T_J = 150^\circ\text{C}$ | 1.7 | 2.1 | 2.3* | |
| | | | $T_J = -40^\circ\text{C}$ | 1.6 | 1.8 | 2.2 | |
| | | $I_C = 10 \text{ A}, V_{GE} = 4.5 \text{ V}$ | $T_J = 25^\circ\text{C}$ | 1.3 | 1.8 | 2.0* | |
| | | | $T_J = 150^\circ\text{C}$ | 1.3 | 1.75 | 2.0* | |
| | | | $T_J = -40^\circ\text{C}$ | 1.4 | 1.8 | 2.0* | |
| Forward Transconductance | gfs | $V_{CE} = 5.0 \text{ V}, I_C = 6.0 \text{ A}$ | $T_J = -40^\circ\text{C to } 150^\circ\text{C}$ | 8.0 | 14 | 25 | Mhos |

DYNAMIC CHARACTERISTICS

| | | | | | | | |
|----------------------|-----------|--|---|-----|-----|------|----|
| Input Capacitance | C_{ISS} | $V_{CC} = 25 \text{ V}, V_{GE} = 0 \text{ V}$ $f = 1.0 \text{ MHz}$ | $T_J = -40^\circ\text{C to } 150^\circ\text{C}$ | 400 | 800 | 1000 | pF |
| Output Capacitance | C_{OSS} | | | 50 | 75 | 100 | |
| Transfer Capacitance | C_{RSS} | | | 4.0 | 7.0 | 10 | |

SWITCHING CHARACTERISTICS

| | | | | | | | |
|---------------------------------|--------------|--|--------------------------|---|-----|-----|---------------|
| Turn-Off Delay Time (Resistive) | $t_{d(off)}$ | $V_{CC} = 300 \text{ V}, I_C = 6.5 \text{ A}$ $R_G = 1.0 \text{ k}\Omega, R_L = 46 \Omega,$ | $T_J = 25^\circ\text{C}$ | - | 4.0 | 10 | μs |
| Fall Time (Resistive) | t_f | $V_{CC} = 300 \text{ V}, I_C = 6.5 \text{ A}$ $R_G = 1.0 \text{ k}\Omega, R_L = 46 \Omega,$ | $T_J = 25^\circ\text{C}$ | - | 9.0 | 15 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{CC} = 10 \text{ V}, I_C = 6.5 \text{ A}$ $R_G = 1.0 \text{ k}\Omega, R_L = 1.5 \Omega$ | $T_J = 25^\circ\text{C}$ | - | 0.7 | 4.0 | μs |
| Rise Time | t_r | $V_{CC} = 10 \text{ V}, I_C = 6.5 \text{ A}$ $R_G = 1.0 \text{ k}\Omega, R_L = 1.5 \Omega$ | $T_J = 25^\circ\text{C}$ | - | 4.5 | 7.0 | |

*Maximum Value of Characteristic across Temperature Range.

- When surface mounted to an FR4 board using the minimum recommended pad size.
- Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.

NGB18N40CLB, NGB18N40ACLB

TYPICAL ELECTRICAL CHARACTERISTICS

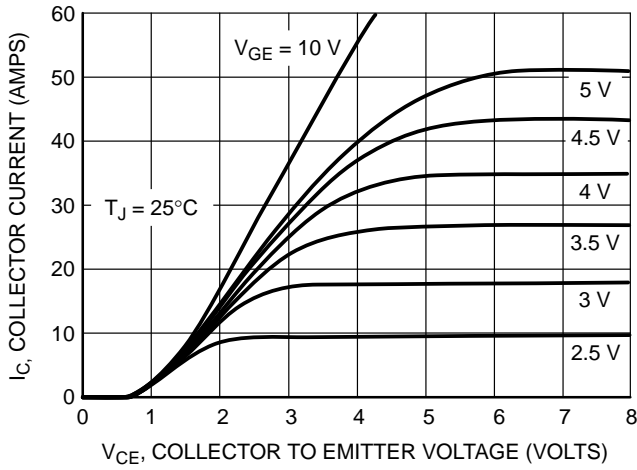


Figure 1. Output Characteristics

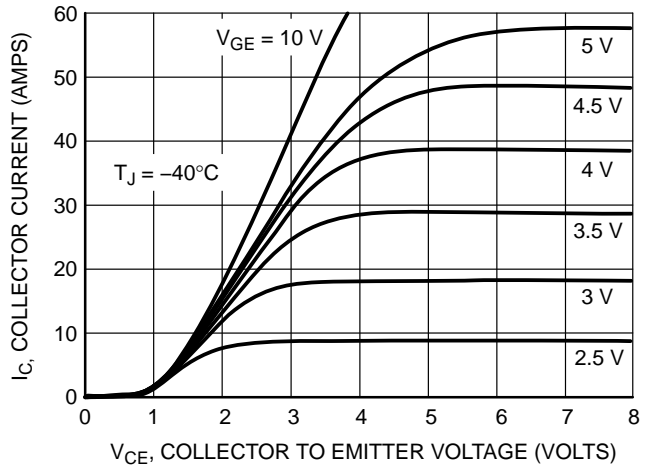


Figure 2. Output Characteristics

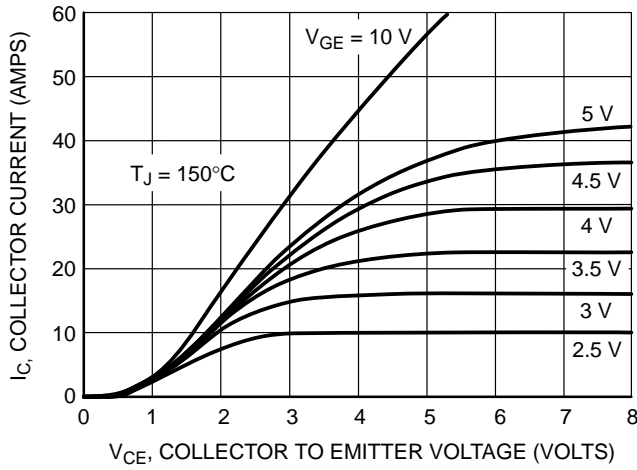


Figure 3. Output Characteristics

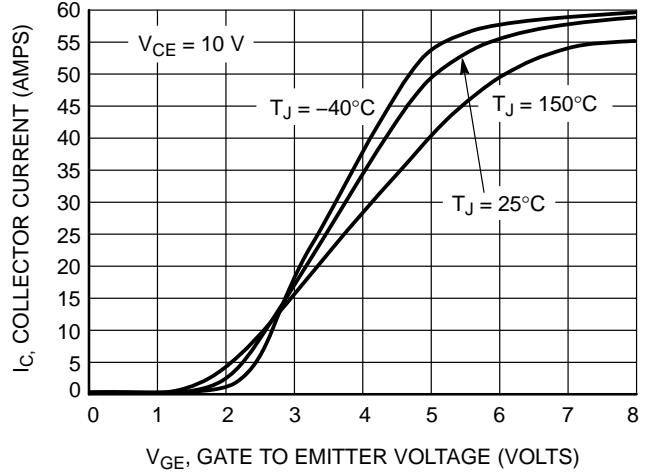


Figure 4. Transfer Characteristics

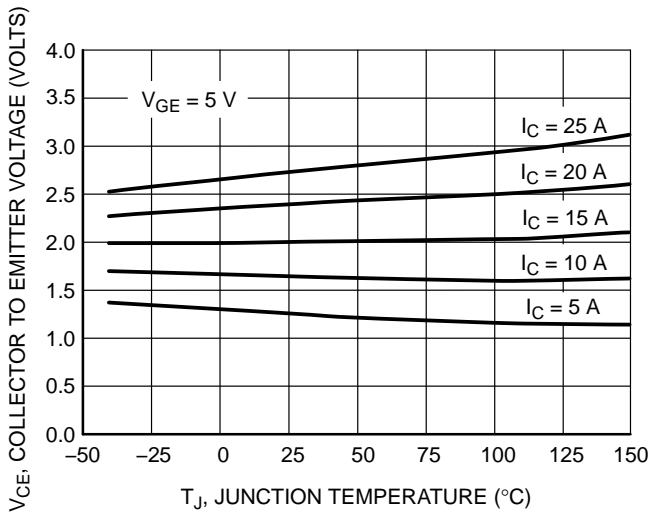


Figure 5. Collector-to-Emitter Saturation Voltage versus Junction Temperature

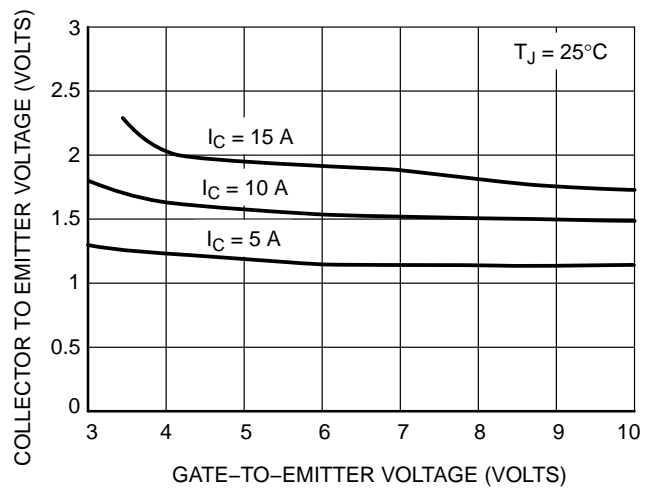


Figure 6. Collector-to-Emitter Voltage versus Gate-to-Emitter Voltage

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TYPICAL ELECTRICAL CHARACTERISTICS

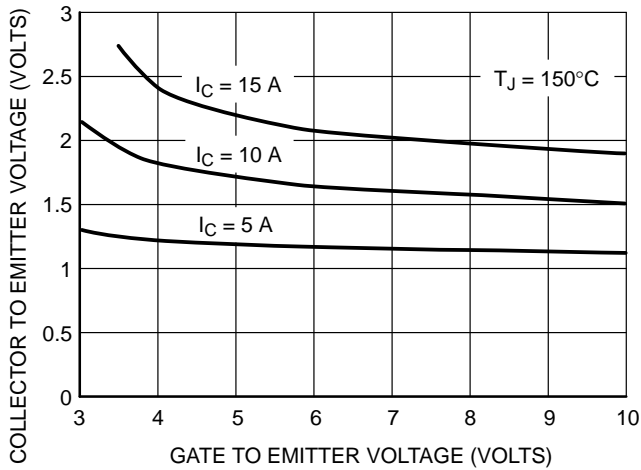


Figure 7. Collector-to-Emitter Voltage versus Gate-to-Emitter Voltage

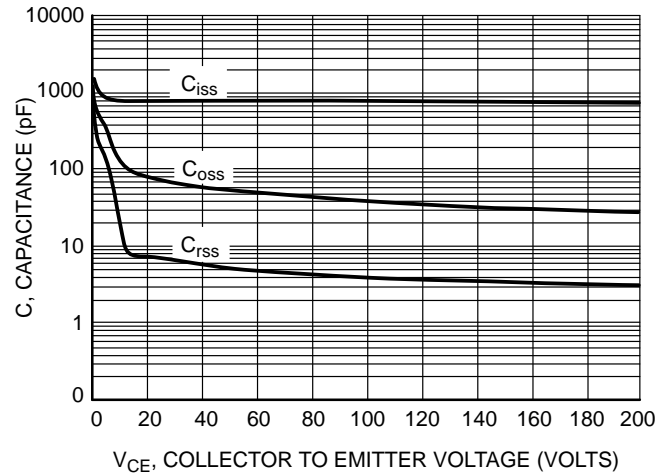


Figure 8. Capacitance Variation

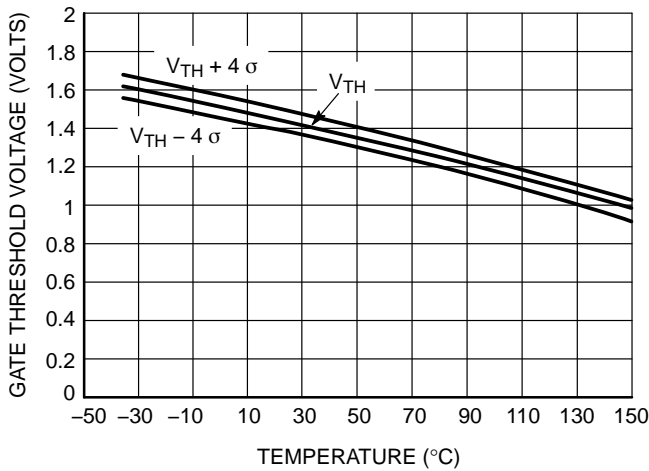


Figure 9. Gate Threshold Voltage versus Temperature

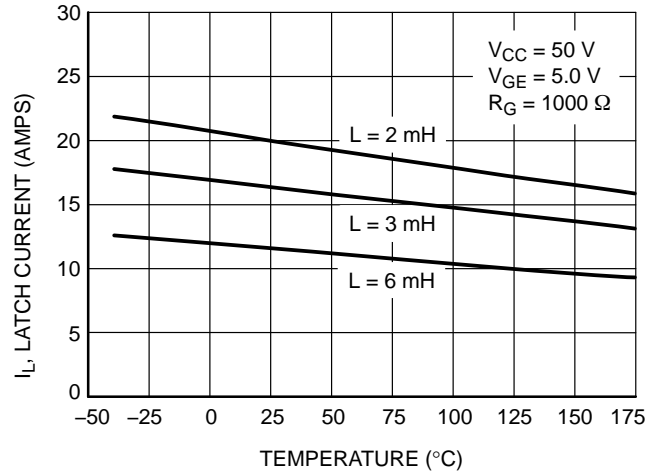


Figure 10. Minimum Open Secondary Latch Current versus Temperature

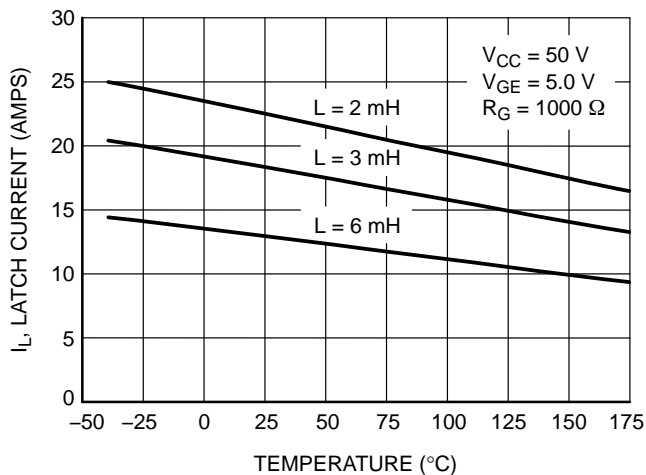


Figure 11. Typical Open Secondary Latch Current versus Temperature

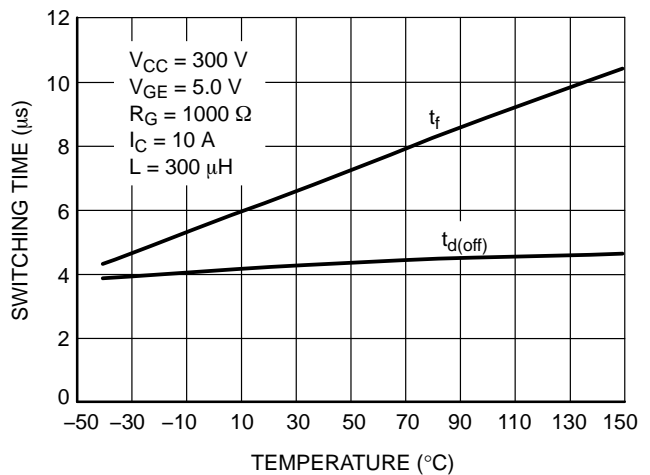


Figure 12. Inductive Switching Fall Time versus Temperature

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TYPICAL ELECTRICAL CHARACTERISTICS

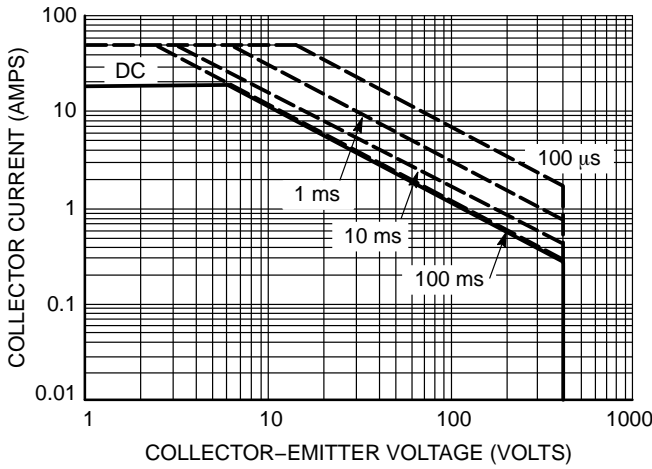


Figure 13. Single Pulse Safe Operating Area (Mounted on an Infinite Heatsink at $T_A = 25^\circ\text{C}$)

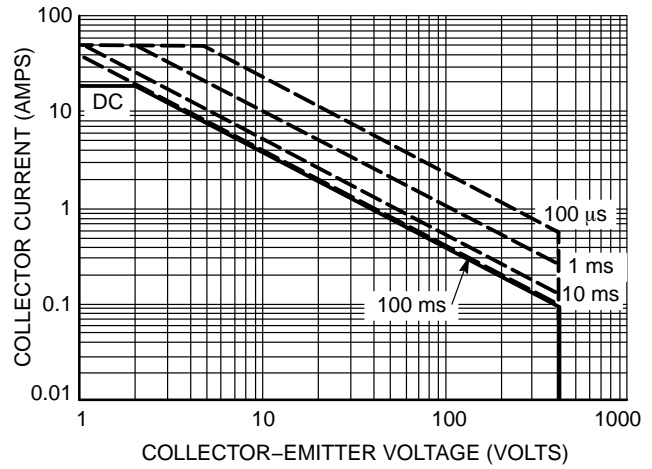


Figure 14. Single Pulse Safe Operating Area (Mounted on an Infinite Heatsink at $T_A = 125^\circ\text{C}$)

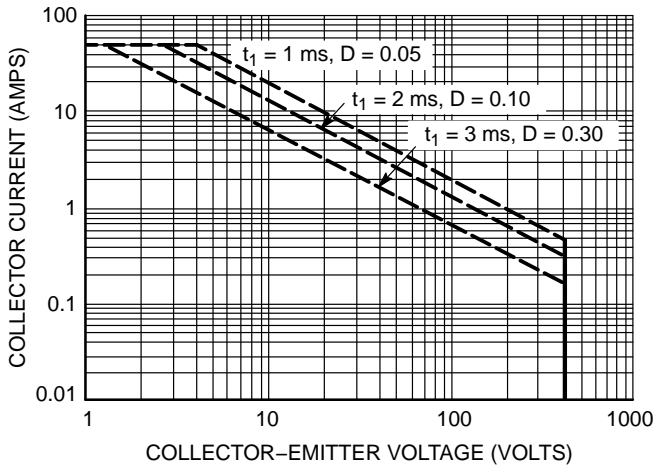


Figure 15. Pulse Train Safe Operating Area (Mounted on an Infinite Heatsink at $T_C = 25^\circ\text{C}$)

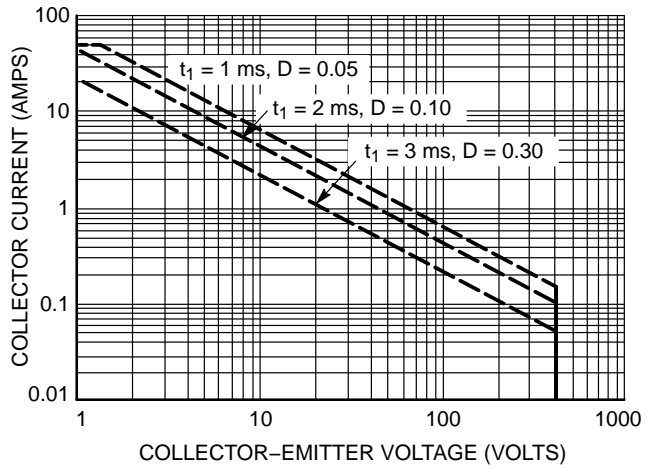


Figure 16. Pulse Train Safe Operating Area (Mounted on an Infinite Heatsink at $T_C = 125^\circ\text{C}$)

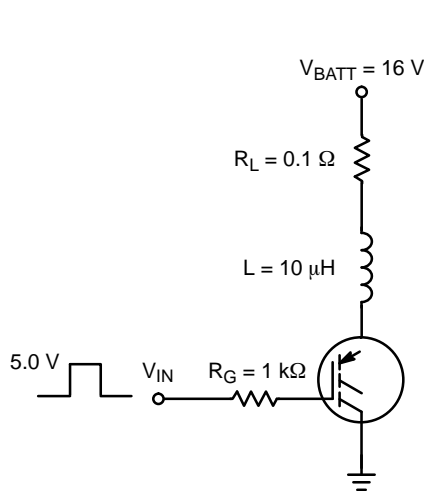


Figure 17. Circuit Configuration for Short Circuit Test #1

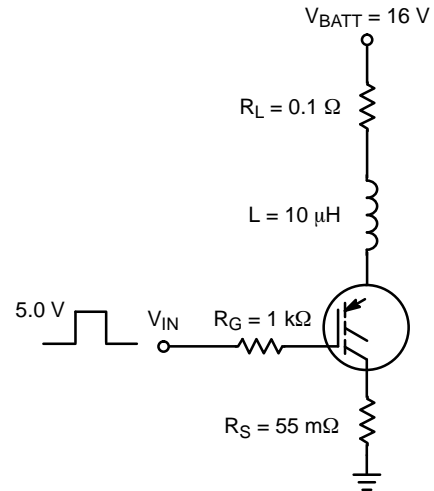


Figure 18. Circuit Configuration for Short Circuit Test #2

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TYPICAL ELECTRICAL CHARACTERISTICS

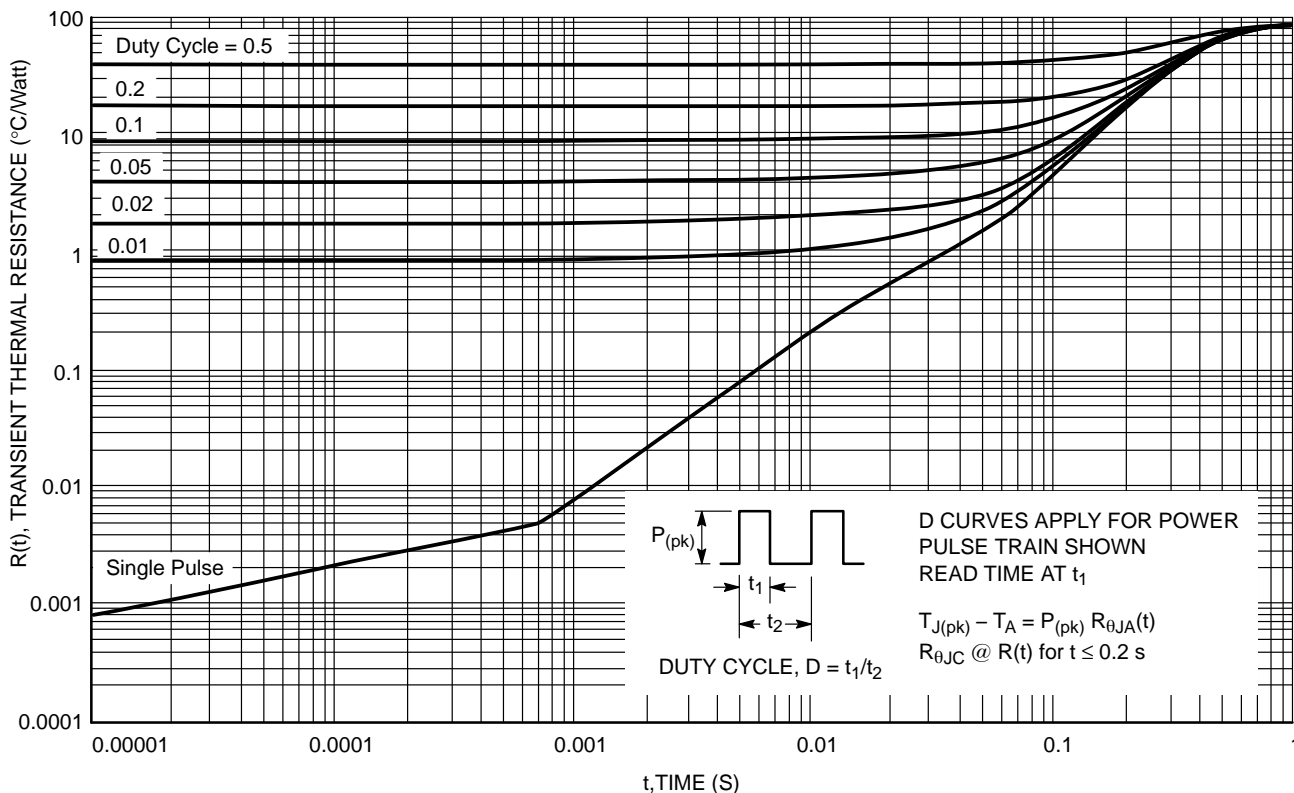
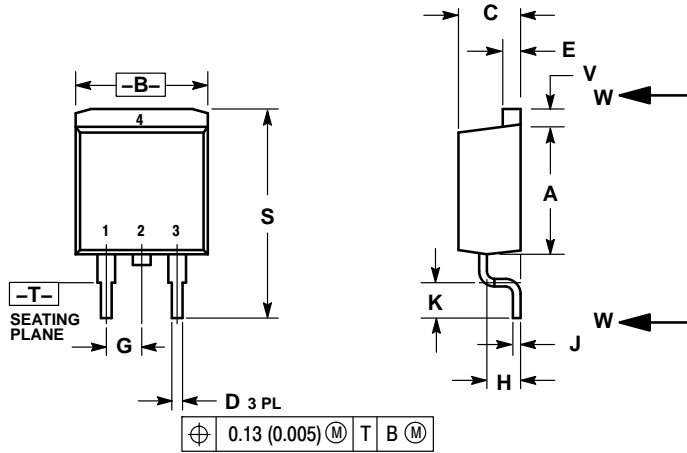


Figure 19. Transient Thermal Resistance (Non-normalized Junction-to-Ambient mounted on minimum pad area)

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PACKAGE DIMENSIONS

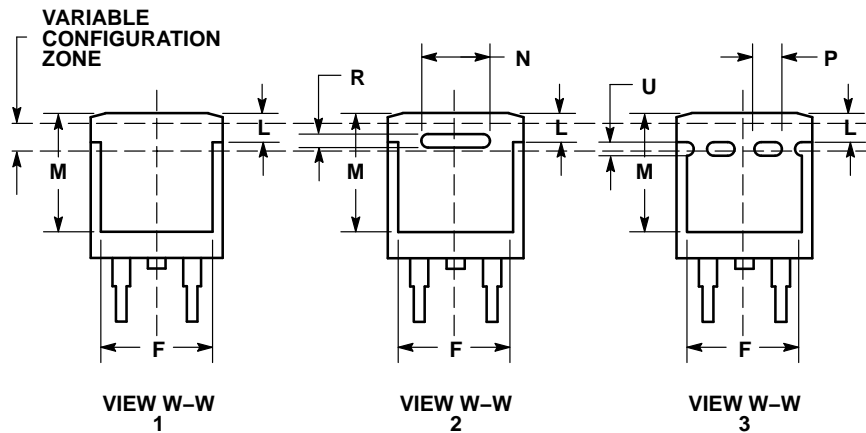
D²PAK 3
CASE 418B-04
ISSUE L



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

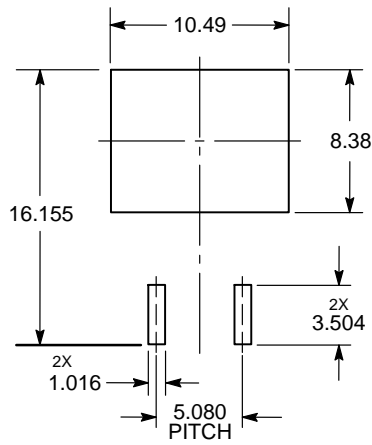
| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.340 | 0.380 | 8.64 | 9.65 |
| B | 0.380 | 0.405 | 9.65 | 10.29 |
| C | 0.160 | 0.190 | 4.06 | 4.83 |
| D | 0.020 | 0.035 | 0.51 | 0.89 |
| E | 0.045 | 0.055 | 1.14 | 1.40 |
| F | 0.310 | 0.350 | 7.87 | 8.89 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.080 | 0.110 | 2.03 | 2.79 |
| J | 0.018 | 0.025 | 0.46 | 0.64 |
| K | 0.090 | 0.110 | 2.29 | 2.79 |
| L | 0.052 | 0.072 | 1.32 | 1.83 |
| M | 0.280 | 0.320 | 7.11 | 8.13 |
| N | 0.197 REF | | 5.00 REF | |
| P | 0.079 REF | | 2.00 REF | |
| R | 0.039 REF | | 0.99 REF | |
| S | 0.575 | 0.625 | 14.60 | 15.88 |
| V | 0.045 | 0.055 | 1.14 | 1.40 |



STYLE 4:

- PIN 1. GATE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR


SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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