MAX77278 Programmer's Guide

UG6490; Rev 0; 9/17

Abstract

The MAX77278 provides highly integrated battery charging and power-supply solutions for low-power applications where size and efficiency are critical, as well as a current sink for IR LEDs typically found in remotes. The MAX77278 device data sheet provides the complete hardware and electrical description for these devices. This Programmer's Guide focuses on the register map for the devices and provides general advice for programmers.

Table of Contents

1 OTP Options 4
2 OTP Registers Quick Reference Table 4
3 Register Reset Conditions 5
3.1 System Power-On Reset Comparator (POR) 5
3.2 System Reset (SYSRST) 5
3.3 CHGPOK 5
3.4 CHGPOR 5
4 Baseline Initialization 6
5 Software Management of the Charger 7
5.1 Managing VSYS_REG, CHG_CV, and CHG_CV_JEITA 8
6 Managing SIMO Current Limits (IP_SBBx) 9
7 Managing Main-Bias Circuits (SBIA_LPM) 9
8 Changing Regulator Output Voltages 10
9 Register Description 11
9.1 Register Descriptions: Global Resources 11
9.1.1 CNFG_GLBL 11
9.1.2 INT_GLBL 12
9.1.3 INTM_GLBL 13
9.1.4 STAT_GLBL 14
9.1.5 ERCFLAG 15
9.1.6 CID 16
9.2 Register Descriptions: GPIO 17
9.2.1 INT_GPIO_R 17
9.2.2 INT_GPIO_F 18
9.2.3 CNFG_GPIO0 19
9.2.4 CNFG_GPIO1 20
9.2.5 CNFG_GPIO2 21
9.2.6 CNFG_GPIO3 22
9.2.7 CNFG_GPIO4 23
9.2.8 CNFG_GPIO5 24
9.2.9 CNFG_GPIO6 25
9.2.10 CNFG_GPIO7 26
9.2.11 MR_GPIO_INC 27
9.3 Register Descriptions: Charger 28
9.3.1 INT_CHG 28
9.3.2 INT_M_CHG 29
9.3.3 STAT_CHG_A 30
9.3.4 STAT_CHG_B 31
9.3.5 CNFG_CHG_A 32
9.3.6 CNFG_CHG_B 33
9.3.7 CNFG_CHG_C 34
9.3.8 CNFG_CHG_D 35
9.3.9 VSYS_REG Code Table 35
9.3.10 CNFG_CHG_E 36
9.3.11 CHG_CC and CHG_CC_JEITA Code Table 36
9.3.12 CNFG_CHG_F 37
9.3.13 CNFG_CHG_G 38
9.3.14 CHG_CV and CHG_CV_JEITA Code Table 39
9.3.15 CNFG_CHG_H 40

9.3.16 CNFG_CHG_I 41
9.3.17 IMON_DISCHG_SCALE Code Table 41
9.4 Register Descriptions: LDO 42
9.4.1 CNFG_LDO_A 42
9.4.2 TV_LDO Code Table 43
9.4.3 CNFG_LDO_B 44
9.5 Register Descriptions: SIMO Buck Boost 45
9.5.1 CNFG_SBB_TOP 45
9.5.2 CNFG_SBB0_A 46
9.5.3 TV_SBB0 Code Table 46
9.5.4 CNFG_SBB0_B 47
9.5.5 CNFG_SBB1_A 48
9.5.6 TV_SBB1 Code Table 48
9.5.7 CNFG_SBB1_B 49
9.5.8 CNFG_SBB2_A 50
9.5.9 TV_SBB2 Code Table 50
9.5.10 CNFG_SBB2_B 51
9.6 Register Descriptions: Current Sink 52
9.6.1 CNFG_CS 52
10 Revision History 53

1 OTP Options

Each register table that appears within this programmer's guide has a column for the register default value. If the default value is fixed for all versions of this device, then the value appears as "0" or "1". If the default value is one-time factory programmable (OTP), it varies depending on the version of device you are using and is listed as "x". See the *OTP Registers Quick Reference Table* to determine the default values for a given device.

2 OTP Registers Quick Reference Table

	MAX77278C
CID	0x3
DIDM	0x0
CHG_EN	disabled
MRT_OTP	8s reset
GPIO_MRT	5s reset
IP_SBB0	0.5A
TV_SBB0	5.3V
EN_SBB0	FPS slot 2
ADE_SBB0	enabled
IP_SBB1	1.0A
TV_SBB1	1.9V
EN_SBB1	FPS slot 0
ADE_SBB1	enabled
IP_SBB2	0.5A
TV_SBB2	3.2V
EN_SBB2	FPS slot 1
ADE_SBB2	enabled
TV_LDO	5.1375V
EN_LDO	FPS slot 3
ADE_LDO	enabled

3 Register Reset Conditions

3.1 System Power-On Reset Comparator (POR)

The SYS POR comparator monitors V_{SYS} and generates a power-on reset signal (POR). When V_{SYS} is below V_{POR}, the device is held in reset (SYSRST = 1). When V_{SYS} rises above V_{POR}, internal signals and on-chip memory stabilize and the device is released from reset (SYSRST = 0).

3.2 System Reset (SYSRST)

The majority of the registers within the device have the reset condition of SYSRST = 1. The SYSRST signal is created by the “On/Off Controller” logic and is continuously high when the system voltage is lower than the power-on reset threshold ($V_{SYS}<V_{POR}$). Additionally, SYSRST is pulsed high to reset the registers during the on/off controller’s “immediate shutdown” routine and “power-down sequence” routine (refer to the IC data sheet’s *On/Off Controller* section for more information).

3.3 CHGPOK

Registers with reset conditions specified as CHGPOK are held in their reset state whenever $V_{CHGIN}<V_{CHGIN\_UVLO}$ or USBS = 1. These registers contain charger status information and the charger input current limit setting. Writes to this register while they are being held in reset are ignored.

3.4 CHGPOR

The USBS bitfield is held in its reset state whenever V_{CHGIN} < 1.8V. Writes to USBS while it is held in reset are ignored.

4 Baseline Initialization

Each time the system's microprocessor boots, execute initialization code for the device per the following guidelines:

A) To maximize performance, set the main bias circuits to operate in normal power mode (SBIA_LPM = 0).
   a. See the *Managing Main-Bias Circuits (SBIA_LPM)* section for more information.
B) The default ONKEY style is for push-button. If your system is using a slide-switch style ONKEY, then set nEN_MODE = 1.
C) The default ONKEY debounce time is factory programmable with OTP. If your system prefers a time that is different that the factory programmed value program DBEN_nEN accordingly.
D) If you are using the GPIO's as a reset mechanism, check the debounce time set by GPIO_MRT.
E) Read the DIDM[1:0] and CID[2:0] to make sure that the correct version of the device is installed in your hardware.
   a. This version checking routine is highly recommended to catch any issues during the manufacturing process. For example, some manufacturers stock multiple versions of this device and this step help protect against any mixing of the stock.
F) Read the ERCFLAG register and take any necessary actions based on its information.
G) Read the interrupt and status registers INT_GLBL, STAT_GLBL, INT_CHG, STAT_CHG_A, STAT_CHG_B and take any necessary actions based on their information.
H) Set interrupt masks INT_GLBLM and INT_M_CHG as desired.
   a. It is highly recommended that systems using the battery charger program CHGIN_M = 0 so that they are notified through the nIRQ pin when an adapter has been plugged or unplugged from the device. See the *Software Management of the Charger* section for more information.
I) Set the GPIO as desired with the CNFG_GPIO register
J) Set the thermistor thresholds with the CNFG_CHG_A register
K) Configure each charger parameter with the reset condition of SYSRST = 1.
   a. Charger parameters with reset condition of CHGPOK do not need to be managed in the baseline initialization routine. See the *Software Management of the Charger* section for more information.
L) Configure the active discharge bits per your preference: ADE_SBB0, ADE_SBB1, ADE_SBB2, ADE_LDO.
M) To maximize efficiency, program the SIMO drive strength to the highest setting (DRV_SBB = 0b00).
   a. If noise issues appear in the system, experiment with slower setting options.
N) Adjust the SIMO current limits per your systems output current requirements (IP_SBB0[1:0], IP_SBB1[1:0], IP_SBB2[1:0]).
   a. Note that it is generally recommended to keep the SIMO current limits as low as possible. See the *Managing SIMO Current Limits (IP_SBBx)* section for more information.
O) To get the best quiescent current performance, set the main bias circuits to operate in low-power mode (SBIA_LPM = 1) before finishing the initialization routine.

5 Software Management of the Charger

1. All the charger configuration except for the charger input current limit (ICHGIN_LIM) should be managed in the baseline initialization routine. See the *Baseline Initialization* section for more information.
    a. It is a common misperception that the fast charge current limit should be modulated based off the available capacity of the charge adapter and/or the system load current requirements. This is not correct. The fast charge current limit should be set based on the characteristics of the battery only. The charger automatically modulates the charge current as required to meet the input current limit or provide for system load current.
2. Charging only happens when the on/off controller is in the “On via On/Off Controller” state.
3. Although the charger configuration happens during the baseline initialization, it is recommended that the processor read the charge configuration information periodically during the charge cycle as a safety measure to ensure everything is as it should be. It is critical that the battery regulation voltage (CHG_CV[5:0]) be correct.
4. Within the Baseline Initialization routine, program the charger interrupt mask (CHGIN_M) to 0. This allows any change in the charger input (CHGIN) status to be directly reported to the processor via the interrupt pin (nIRQ). See the *Baseline Initialization* section for more information.
5. When the charger input interrupt is pending (CHGIN_I = 1), read the CHG_DTLS:
    a. when the charger input is okay (CHGIN_DTLS = 0b11):
        i. enumerate the charger input if it is a USB source (not through the MAX77278)
        ii. program the desired charger input current limit (ICHGIN_LIM[2:0])
        iii. Read the charge configuration information to ensure it matches the desired values programmed by the baseline initialization routine. This step is not necessary but it is a recommended safety measure.
        iv. enable the charger (CHG_EN = 1)
    b. when the charger input is in undervoltage lockout (CHGIN_DTLS = 0b00):
        i. disable the charger (CHG_EN = 0)
        ii. note that the charger input current limit (ICHGIN_LIM) is continuously held in reset during this condition
    c. when the charger input is in overvoltage lockout (CHGIN_DTLS = 0b01):
        i. disable the charger (CHG_EN = 0)
            1. this is not really necessary but recommended
        ii. based on the user experience desired, software can either do nothing or provide a message to the user that something is wrong with their charge adapter and they should remove it from the device
    d. when the charger input is being debounce (CHGIN_DTLS = 0b10)
        i. based on the user experience desired, software can either do nothing or provide a message to the user that the charger input has been applied to the system
            1. Note that the charger input debounce time ($t_{CHGIN-DB}$) is typically 120ms.

5.1 Managing VSYS_REG, CHG_CV, and CHG_CV_JEITA

Program VSYS_REG to at least 200mV above the higher of CHG_CV and CHG_CV_JEITA. Any write request that violates this requirement causes the device to force CHG_CV and CHG_CV_JEITA to conform to this restraint.

Example 1: Program CHG_CV to any value above (VSYS_REG – 200mV)

If a write command tries to program CHG_CV to any value above (VSYS_REG – 200mV), the device overrides the write and programs CHG_CV to (VSYS_REG – 200mV).
For example, VSYS_REG = 4.5V and CHG_CV = 3.6V. A command tries to write CHG_CV to 4.4V; the device overrides this and programs CHG_CV to 4.3V.

Example 2: Program VSYS_REG below (CHG_CV + 200mV)

If a write command tries to program VSYS_REG below (CHG_CV + 200mV), the device writes VSYS_REG to the requested voltage, but forces CHG_CV to (VSYS_REG – 200mV).
For example, VSYS_REG = 4.5V and CHG_CV = 4.2V. A command programs VSYS_REG to 4.1V; the device automatically programs CHG_CV to 3.9V.

Example 3: Programming VSYS_REG, CHG_CV, CHG_CV_JEITA Use Case

Take the following case:
existing settings: VSYS_REG = 4.2V, CHG_CV =3.6V, CHG_CV_JEITA = 3.6V
desired settings: VSYS_REG = 4.4V, CHG_CV = 4.2V, CHG_CV_JEITA = 4.1V
Incorrect Method:

1) program CHG_CV = 4.2V
2) program CHG_CV_JEITA = 4.1V
3) program VSYS_REG = 4.4V

resulting settings are wrong: VSYS_REG = 4.4V, CHG_CV = 4.0V, CHG_CV_JEITA = 4.0V

Correct Method:

1) program VSYS_REG = 4.4V
2) program CHG_CV = 4.2V
3) program CHG_CV_JEITA = 4.1V

resulting settings are correct: VSYS_REG = 4.4V, CHG_CV = 4.2V, CHG_CV_JEITA = 4.1V

6 Managing SIMO Current Limits (IP_SBBx)

The available output current on a given SIMO channel is a function of the input voltage, the output voltage, the peak current limit setting, and the output current of the other SIMO channels. Maxim offers a SIMO calculator that outlines the available capacity for specific conditions. Visit the product page at www.maximintegrated.com/MAX77278 for more information on support documents.

Generally speaking, applications should use the lowest possible SIMO peak current limit for a given mode of operation. Lower SIMO peak current settings give better efficiency, lower output voltage ripple, and lower noise. For example, if a system has increasing power states of OFF>>HIBERNATE>>STANDBY>> ACTIVE, then it is recommended to tailor the SIMO current limits for the power needs of each particular state. HIBERNATE can use 500mA for each SIMO channel, STANDBY can use 0.866A, 0.707A, and 0.5A for SIMO SBB0, SBB1, and SBB2, while ACTIVE can use 1A for each SIMO channel. Once again, refer to the SIMO calculator for guidance on how to size the current limits for a given set of power needs.

7 Managing Main-Bias Circuits (SBIA_LPM)

1) Applications that are not concerned about quiescent current can leave the main-bias circuits in their normal-power mode indefinitely (SBIA_LPM = 0).
2) Applications that are concerned about quiescent current and want to have a simple software structure can leave the main-bias circuits in their low-power mode indefinitely (SBIA_LPM = 1).
3) Applications that want to maximize performance and have low quiescent current should dynamically control the main-bias circuits (SBIA_LPM).
    a) To maximize performance, set the main bias circuits to operate in normal power mode (SBIA_LPM = 0) whenever the system is doing a significant task. A tasks' significance is judged according to how much quiescent current is consumed current is consumed by the system in order to accomplish that task relative to the quiescent current of the MAX77278 when it is in its low-power mode.
    b) To get the best quiescent current performance, set the main bias circuits to operate in low-power mode (SBIA_LPM = 1) whenever the system's current consumption is less than ~2mA.

8 Changing Regulator Output Voltages

The regulator output voltages are programmable. When a regulator is off, the output voltage can be directly programmed. However, when the regulator is on and the output voltage needs to be increased or decrease program a voltage ramp from the existing voltage to the new desired voltage. Programming a ramp is recommended for voltage increases to minimize inrush current. Programming a ramp is recommended on voltage decreases to minimize regulator undershoot when it reaches its target voltage.

Example 1: Enabling a regulator to a static output voltage

1. When the regulator is disabled, program the output voltage to the desired value.
2. To maximize performance, set the main bias circuits to operate in normal-power mode. (SBIA_LPM = 0), wait 100us afterwards for the bias circuits to settle (not really needed but still a good idea).
3. Turn the regulator on.
4. To get the best quiescent current performance, wait for 2ms for the regulator to stabilize (enable delay + soft-start ramp + margin), and then program the main bias circuits to operate in low-power mode (SBIA_LPM = 1).

Example 2: Ramping a regulator output voltage while it is enabled

1. To maximize performance, set the main bias circuits to operate in normal-power mode (SBIA_LPM = 0), wait 100us afterwards for the bias circuits to settle (not really needed but still a good idea).
2. Ramp the regulator output voltage one LSB at a time (increasing or decreasing) until the target voltage is reached.
3. To get the best quiescent current performance, wait for 2ms for the regulator to stabilize (enable delay + soft-start ramp + margin), and then program the main bias circuits to operate in low-power mode (SBIA_LPM = 1).

9 Register Description

The following tables detail the registers for the MAX77278. Undocumented register locations are reserved.

9.1 Register Descriptions: Global Resources

9.1.1 CNFG_GLBL

Register Name	CNFG_GLBL
I²C Slave Address	0x48
Register Address	0x10
Reset Value (HEX)	OTP
Reset Value (BIN)	0b00000000
Reset Condition	SYSRSTB
Access Type	R/W
Register Type	Configuration

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	DB_CNFG[1:0]	GPIO Debounce Timer Configuration 0b00 = 1.25ms Debounce 0b01 = 2.5ms Debounce 0b10 = 5ms Debounce 0b11 = 10ms Debounce	SYSRSTB	R/W
6	0	BOK	Main Bias Okay Status Bit 0 = Main Bias not ready. 1 = Main Bias enabled and ready.	SYSRSTB	R/W
5	0	SBIA_LPM	Main Bias Low-Power Mode software request 0 = Main Bias requested to be in Normal Power Mode by software. 1 = Main Bias request to be in Low Power Mode by software.	SYSRSTB	R/W
4	0	SBIA_EN	Main Bias Enable Software Request 0 = Main Bias not enabled by software. Note that the main bias can be on via the on/off controller circuitry. 1 = Main Bias force enabled by software	SYSRSTB	R/W
3	0	nEN_MODE	nEN Input (ONKEY) Default Configuration Mode 0 = Push-Button Mode 1 = Slide-Switch Mode	SYSRSTB	R/W
2	0	DBEN_nEN	Debounce Timer Enable for the nEN Pin 0 = 100us Debounce 1 = 30ms Debounce	SYSRSTB	R/W
1	0	SFT_RST[1:0]	Software Reset Functions. Refer to the "On/Off Controller" section of the IC data sheet for more information. 0b00 = No Action 0b01 = Software Cold Reset (SFT_CRST). The device powers down, resets, and then powers up again. 0b10 = Software Off (SFT_OFF). The device powers down, resets, and then remains off and waiting for a wakeup event. 0b11 = Reserved	SYSRSTB	R/W
0	0			SYSRSTB	R/W

9.1.2 INT_GLBL

Register Name	INT_GLBL
I²C Slave Address	0x48
Register Address	0x00
Reset Value (HEX)	0x00
Reset Value (BIN)	0b00000000
Reset Condition	SYSRST = 1
Access Type	RC
Register Type	Interrupt

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	LDO_POK_R	LDO POK Interrupt 0 = The LDO is lower than POK level. 1 = The LDO is higher than POK level.	SYSRST = 1	RC
6	0	CS_WD_R	Current Sink Watchdog Timer Interrupt 0 = The current sink watchdog timer has not expired. 1 = The current sink watchdog timer has expired.	SYSRST = 1	RC
5	0	TJAL2_R	Thermal Alarm 2 Rising Interrupt 0 = The junction temperature has not risen above TJAL2 since the last time this bit was read. 1 = The junction temperature has risen above TJAL2T since the last time this bit was read.	SYSRST = 1	RC
4	0	TJAL1_R	Thermal Alarm 1 Rising Interrupt 0 = The junction temperature has not risen above TJAL1 since the last time this bit was read. 1 = The junction temperature has risen above TJAL1 since the last time this bit was read.	SYSRST = 1	RC
3	0	nEN_R	nEN Rising Interrupt 0 = No nEN rising edges have occurred since the last time this bit was read. 1 = A nEN rising edge as occurred since the last time this bit was read.	SYSRST = 1	RC
2	0	nEN_F	nEN Falling Interrupt 0 = No nEN falling edges have occurred since the last time this bit was read. 1 = A nEN falling edge as occurred since the last time this bit was read.	SYSRST = 1	RC
1	0	RESERVED	Reserved. Unutilized bit. Write to 0. Reads are don't care.	SYSRST = 1	RC
0	0	RESERVED	Reserved. Unutilized bit. Write to 0. Reads are don't care.	SYSRST = 1	RC

9.1.3 INTM_GLBL

Register Name	INTM_GLBL
I²C Slave Address	0x48
Register Address	0x08
Reset Value (HEX)	0xFF
Reset Value (BIN)	0b11111111
Reset Condition	SYSRST = 1
Access Type	R/W
Register Type	Interrupt Mask

Bit	Default	Bit Name	Description	Reset	Access Type
7	1	LDO_POK_RM	LDO POK Detector Rising Interrupt Mask 0 = Unmasked. If LDO_POK goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to LDO_POK	SYSRST = 1	R/W
6	1	CS_WD_RM	Current Sink Watchdog Timer Rising Interrupt Mask 0 = Unmasked. If CS_WD goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to CS_WD.	SYSRST = 1	R/W
5	1	TJAL2_RM	Thermal Alarm 2 Rising Interrupt Mask 0 = Unmasked. If TJAL2_R goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to TJAL2_R.	SYSRST = 1	R/W
4	1	TJAL1_RM	Thermal Alarm 1 Rising Interrupt Mask 0 = Unmasked. If TJAL1_R goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to TJAL1_R.	SYSRST = 1	R/W
3	1	nEN_RM	nEN Rising Interrupt Mask 0 = Unmasked. If nEN_R goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to nEN_R.	SYSRST = 1	R/W
2	1	nEN_FM	nEN Falling Interrupt Mask 0 = Unmasked. If nEN_F goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to nEN_F.	SYSRST = 1	R/W
1	1	RESERVED	Reserved. Unutilized bit. Write to 0. Reads are don't care.	SYSRST = 1	R/W
0	1	RESERVED	Reserved. Unutilized bit. Write to 0. Reads are don't care.	SYSRST = 1	R/W

9.1.4 STAT_GLBL

Register Name	STAT_GLBL
I²C Slave Address	0x48
Register Address	0x07
Reset Value (HEX)	NA
Reset Value (BIN)	NA
Reset Condition	SYSRST = 1
Access Type	R
Register Type	Status

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	DIDM[1:0]	Device Identification Bits for Metal Options: 0b00 = MAX77278 All others reserved for future use.	SYSRST = 1	R
6	0			SYSRST = 1	R
5	0	DOD_S	LDO Dropout Detector Rising Status 0 = The LDO is not in dropout 1 = The LDO is in dropout	SYSRST = 1	R
4	0	TJAL2_S	Thermal Alarm 2 Status 0 = The junction temperature is less than TJAL2 1 = The junction temperature is greater than TJAL2	SYSRST = 1	R
3	0	TJAL1_S	Thermal Alarm 1 Status 0 = The junction temperature is less than TJAL1 1 = The junction temperature is greater than TJAL1	SYSRST = 1	R
2	0	STAT_EN	Debounced Status for the nEN input. 0 = nEN0 is not active (logic-high) 1 = nEN0 is active (logic-low)	SYSRST = 1	R
1	0	BOK	Main Bias Okay Status Bit 0 = Main Bias not ready. 1 = Main Bias enabled and ready.	SYSRST = 1	R
0	0	STAT_IRQ	Software Version of the nIRQ MOSFET gate drive. 0 = unmasked gate drive is logic-low 1 = unmasked gate drive is logic-high	SYSRST = 1	R

9.1.5 ERCFLAG

Register Name	ERCFLAG
I²C Slave Address	0x48
Register Address	0x06
Reset Value (HEX)	NA
Reset Value (BIN)	NA
Reset Condition	POR = 1
Access Type	RC
Register Type	Status

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	RESERVED	Reserved. Unutilized bit. Write to 0. Reads are don't care.	POR = 1	RC
6	0	RESERVED	Reserved. Unutilized bit. Write to 0. Reads are don't care.	POR = 1	RC
5	0	SFT_CRST_F	Software Cold Reset Flag 0 = The software cold reset has not occurred since the last read of this register. 1 = The software cold reset has occurred since the last read of this register. This indicates that software has set SFT_RST = 0b01.	POR = 1	RC
4	0	SFT_OFF_F	Software Off Flag 0 = The SFT_OFF function has not occurred since the last read of this register. 1 = The SFT_OFF function has occurred since the last read of this register. This indicates that software has set SFT_RST = 0b10.	POR = 1	RC
3	0	MRST	Manual Reset Timer 0 = A Manual Reset has not occurred since this last read of this register. 1 = A Manual Reset has occurred since this last read of this register.	POR = 1	RC
2	0	SYSUVLO	SYS Domain Undervoltage Lockout 0 = The SYS domain undervoltage lockout has not occurred since this last read of this register. 1 = The SYS domain undervoltage lockout has occurred since the last read of this register. This indicates that the SYS domain voltage fell below VSYSUVLO (~2.4V)	POR = 1	RC
1	0	SYSOVLO	SYS Domain Overvoltage Lockout 0 = The SYS domain overvoltage lockout has not occurred since this last read of this register. 1 = The SYS domain overvoltage lockout has occurred since the last read of this register. This indicates that the SYS domain voltage rose below VSYSOVLO (~5.85V)	POR = 1	RC
0	0	TOVLD	Thermal Overload 0 = The thermal overload has not occurred since the last read of this register. 1 = The thermal overload has occurred since the list read of this register. This indicates that the junction temperature has exceeded 165C.	POR = 1	RC

9.1.6 CID

Register Name	CID
I²C Slave Address	0x48
Register Address	0x11
Reset Value (HEX)	OTP
Reset Value (BIN)	0bxxxxxxxx
Reset Condition	PORB
Access Type	R
Register Type	Data

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	RESERVED	Reserved. Unutilized bit. Write to 0. Reads are don't care.		
6	x	CLKS[2:0]	Sampling Clock Frequency. This 3-bit configuration is for Maxim internal use only and controls a clock divider to set the internal sampling frequency of the global resources. 0b011 = 160Hz 0b100 = 80Hz 0b101 = 40Hz 0b110 = 20Hz 0b111 = 10Hz	PORB	R
				PORB	R
5	x			PORB	R
4	x				
3	x	CID[4:0]	Chip Identification Code. These bits track the OTP configuration. The value is register corresponds to a set of reset values in the register map.	PORB	R
2	x			PORB	R
1	x			PORB	R
0	x			PORB	R

9.2 Register Descriptions: GPIO

9.2.1 INT_GPIO_R

Register Name	INT_GPIO_R
I²C Slave Address	0x48
Register Address	0x02
Reset Value (HEX)	0x00
Reset Value (BIN)	0b00000000
Reset Condition	SYSRST = 1
Access Type	RC
Register Type	Interrupt

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	R_GPIO7	GPI Rising Interrupt 0 = No GPI rising edges have occurred since the last time this bit was read. 1 = A GPI rising edge as occurred since the last time this bit was read. Note that the GPI is the GPIO programmed to be an input.	SYSRST = 1	RC
6	0	R_GPIO6	GPI Rising Interrupt 0 = No GPI rising edges have occurred since the last time this bit was read. 1 = A GPI rising edge as occurred since the last time this bit was read. Note that the GPI is the GPIO programmed to be an input.	SYSRST = 1	RC
5	0	R_GPIO5	GPI Rising Interrupt 0 = No GPI rising edges have occurred since the last time this bit was read. 1 = A GPI rising edge as occurred since the last time this bit was read. Note that the GPI is the GPIO programmed to be an input.	SYSRST = 1	RC
4	0	R_GPIO4	GPI Rising Interrupt 0 = No GPI rising edges have occurred since the last time this bit was read. 1 = A GPI rising edge as occurred since the last time this bit was read. Note that the GPI is the GPIO programmed to be an input.	SYSRST = 1	RC
3	0	R_GPIO3	GPI Rising Interrupt 0 = No GPI rising edges have occurred since the last time this bit was read. 1 = A GPI rising edge as occurred since the last time this bit was read. Note that the GPI is the GPIO programmed to be an input.	SYSRST = 1	RC
2	0	R_GPIO2	GPI Rising Interrupt 0 = No GPI rising edges have occurred since the last time this bit was read. 1 = A GPI rising edge as occurred since the last time this bit was read. Note that the GPI is the GPIO programmed to be an input.	SYSRST = 1	RC
1	0	R_GPIO1	GPI Rising Interrupt 0 = No GPI rising edges have occurred since the last time this bit was read. 1 = A GPI rising edge as occurred since the last time this bit was read. Note that the GPI is the GPIO programmed to be an input.	SYSRST = 1	RC
0	0	R_GPIO0	GPI Rising Interrupt 0 = No GPI rising edges have occurred since the last time this bit was read. 1 = A GPI rising edge as occurred since the last time this bit was read. Note that the GPI is the GPIO programmed to be an input.	SYSRST = 1	RC

9.2.2 INT_GPIO_F

Register Name	INT_GPIO_F
I²C Slave Address	0x48
Register Address	0x03
Reset Value (HEX)	0x00
Reset Value (BIN)	0b00000000
Reset Condition	SYSRST = 1
Access Type	RC
Register Type	Interrupt

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	F_GPIO7	GPI Falling Interrupt 0 = No GPI falling edges have occurred since the last time this bit was read. 1 = A GPI falling edge as occurred since the last time this bit was read. Note that the GPI is the GPIO programmed to be an input.	SYSRST = 1	RC
6	0	F_GPIO6	GPI Falling Interrupt 0 = No GPI falling edges have occurred since the last time this bit was read. 1 = A GPI falling edge as occurred since the last time this bit was read. Note that the GPI is the GPIO programmed to be an input.	SYSRST = 1	RC
5	0	F_GPIO5	GPI Falling Interrupt 0 = No GPI falling edges have occurred since the last time this bit was read. 1 = A GPI falling edge as occurred since the last time this bit was read. Note that the GPI is the GPIO programmed to be an input.	SYSRST = 1	RC
4	0	F_GPIO4	GPI Falling Interrupt 0 = No GPI falling edges have occurred since the last time this bit was read. 1 = A GPI falling edge as occurred since the last time this bit was read. Note that the GPI is the GPIO programmed to be an input.	SYSRST = 1	RC
3	0	F_GPIO3	GPI Falling Interrupt 0 = No GPI falling edges have occurred since the last time this bit was read. 1 = A GPI falling edge as occurred since the last time this bit was read. Note that the GPI is the GPIO programmed to be an input.	SYSRST = 1	RC
2	0	F_GPIO2	GPI Falling Interrupt 0 = No GPI falling edges have occurred since the last time this bit was read. 1 = A GPI falling edge as occurred since the last time this bit was read. Note that the GPI is the GPIO programmed to be an input.	SYSRST = 1	RC
1	0	F_GPIO1	GPI Falling Interrupt 0 = No GPI falling edges have occurred since the last time this bit was read. 1 = A GPI falling edge as occurred since the last time this bit was read. Note that the GPI is the GPIO programmed to be an input.	SYSRST = 1	RC
0	0	F_GPIO0	GPI Falling Interrupt 0 = No GPI falling edges have occurred since the last time this bit was read. 1 = A GPI falling edge as occurred since the last time this bit was read. Note that the GPI is the GPIO programmed to be an input.	SYSRST = 1	RC

9.2.3 CNFG_GPIO0

Register Name	CNFG_GPIO0
I²C Slave Address	0x48
Register Address	0x50
Reset Value (HEX)	0xF3
Reset Value (BIN)	0b11110011
Reset Condition	SYSRST = 1
Access Type	Mixed
Register Type	Mixed

Bit	Default	Bit Name	Description		Reset	Access Type
7	1	RM_GPIO0	GPIO0 Rising Interrupt Mask 0 = Unmasked. If R_GPIO0 goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to R_GPIO0.		SYSRST = 1	R/W
6	1	FM_GPIO0	GPIO0 Falling Interrupt Mask 0 = Unmasked. If F_GPIO0 goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to F_GPIO0.		SYSRST = 1	R/W
5	1	WK_EN0	General-Purpose Input Wakeup Enable		SYSRST = 1	R/W
4	1	DBEN_GPIO0	General-Purpose Input Debounce Timer Enable 0 = no debounce 1 = debounce time set by DB_CNFG[1:0]		SYSRST = 1	R/W
3	0	DO0	General-Purpose Output Data Output When set for GPO (DIR0 = 0): 0 = GPIO0 is output is logic-low 1 = GPIO0 is output logic-high when set as push-pull output (DRV0 = 1). GPIO0 is high-impedance when set as a and open-drain output (DRV0 = 0).	When set for GPI (DIR0 = 1): DO0 writes are don't care.	SYSRST = 1	R/W
2	0	DRV0	General-Purpose Output Driver Type When set for GPO (DIR0 = 0): 0 = open-drain 1 = Push-Pull	When set for GPI (DIR0 = 1): DRV0 is a don't care when GPI.	SYSRST = 1	R/W
1	1	DI0	GPIO0 Digital Input Value. Irrespective of whether the GPIO0 is set for GPI (DIR0 = 1) or GPO (DIR0 = 0), DI0 reflects the state of GPIO0 . 0 = input logic-low 1 = input logic-high		SYSRST = 1	R
0	1	DIR0	GPIO0 Direction. 0 = General-purpose output (GPO) 1 = General-purpose input (GPI)		SYSRST = 1	R/W

9.2.4 CNFG_GPIO1

Register Name	CNFG_GPIO1
I²C Slave Address	0x48
Register Address	0x51
Reset Value (HEX)	0xF3
Reset Value (BIN)	0b11110011
Reset Condition	SYSRST = 1
Access Type	Mixed
Register Type	Mixed

Bit	Default	Bit Name	Description		Reset	Access Type
7	1	RM_GPIO1	GPIO1 Rising Interrupt Mask 0 = Unmasked. If R_GPIO1 goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to R_GPIO1.		SYSRST = 1	R/W
6	1	FM_GPIO1	GPIO1 Falling Interrupt Mask 0 = Unmasked. If F_GPIO1 goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to F_GPIO1.		SYSRST = 1	R/W
5	1	WK_EN1	General-Purpose Input Wakeup Enable		SYSRST = 1	R/W
4	1	DBEN_GPIO1	General-Purpose Input Debounce Timer Enable 0 = no debounce 1 = debounce time set by DB_CNFG[1:0]		SYSRST = 1	R/W
3	0	DO1	General-Purpose Output Data Output When set for GPO (DIR1 = 0): 0 = GPIO1 is output is logic-low 1 = GPIO1 is output logic-high when set as push-pull output (DRV1 = 1). GPIO1 is high-impedance when set as a and open-drain output (DRV1 = 0).	When set for GPI (DIR1 = 1): DO1 writes are don't care.	SYSRST = 1	R/W
2	0	DRV1	General-Purpose Output Driver Type When set for GPO (DIR1 = 0): 0 = open-drain 1 = Push-Pull	When set for GPI (DIR1 =1): DRV1 is a don't care when GPI.	SYSRST = 1	R/W
1	1	DI1	GPIO1 Digital Input Value. Irrespective of whether the GPIO1 is set for GPI (DIR1 = 1) or GPO (DIR1 = 0), DI1 reflects the state of GPIO1 . 0 = input logic-low 1 = input logic-high		SYSRST = 1	R
0	1	DIR1	GPIO1 Direction. 0 = General-purpose output (GPO) 1 = General-purpose input (GPI)		SYSRST = 1	R/W

9.2.5 CNFG_GPIO2

Register Name	CNFG_GPIO2
I²C Slave Address	0x48
Register Address	0x52
Reset Value (HEX)	0xF3
Reset Value (BIN)	0b11110011
Reset Condition	SYSRST = 1
Access Type	Mixed
Register Type	Mixed

Bit	Default	Bit Name	Description		Reset	Access Type
7	1	RM_GPIO2	GPIO2 Rising Interrupt Mask 0 = Unmasked. If R_GPIO2 goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to R_GPIO2.		SYSRST = 1	R/W
6	1	FM_GPIO2	GPIO2 Falling Interrupt Mask 0 = Unmasked. If F_GPIO2 goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to F_GPIO2.		SYSRST = 1	R/W
5	1	WK_EN2	General-Purpose Input Wakeup Enable		SYSRST = 1	R/W
4	1	DBEN_GPIO2	General-Purpose Input Debounce Timer Enable 0 = no debounce 1 = debounce time set by DB_CNFG[1:0]		SYSRST = 1	R/W
3	0	DO2	General-Purpose Output Data Output When set for GPO (DIR2 = 0): 0 = GPIO2 is output is logic-low 1 = GPIO2 is output logic-high when set as push-pull output (DRV2 = 1). GPIO2 is high-impedance when set as a and open-drain output (DRV2 = 0).	When set for GPI (DIR2 = 1): DO2 writes are don't care.	SYSRST = 1	R/W
2	0	DRV2	General-Purpose Output Driver Type When set for GPO (DIR2 = 0): 0 = open-drain 1 = Push-Pull	When set for GPI (DIR2 = 1): DRV2 is a don't care when GPI.	SYSRST = 1	R/W
1	1	DI2	GPIO2 Digital Input Value. Irrespective of whether the GPIO2 is set for GPI (DIR2 = 1) or GPO (DIR2 = 0), DI2 reflects the state of GPIO2 . 0 = input logic-low 1 = input logic-high		SYSRST = 1	R
0	1	DIR2	GPIO2 Direction. 0 = General-purpose output (GPO) 1 = General-purpose input (GPI)		SYSRST = 1	R/W

9.2.6 CNFG_GPIO3

Register Name	CNFG_GPIO3
I²C Slave Address	0x48
Register Address	0x53
Reset Value (HEX)	0xF3
Reset Value (BIN)	0b11110011
Reset Condition	SYSRST = 1
Access Type	Mixed
Register Type	Mixed

Bit	Default	Bit Name	Description		Reset	Access Type
7	1	RM_GPIO3	GPIO3 Rising Interrupt Mask 0 = Unmasked. If R_GPIO3 goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to R_GPIO3.		SYSRST = 1	R/W
6	1	FM_GPIO3	GPIO3 Falling Interrupt Mask 0 = Unmasked. If F_GPIO3 goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to F_GPIO3.		SYSRST = 1	R/W
5	1	WK_EN3	General-Purpose Input Wakeup Enable		SYSRST = 1	R/W
4	1	DBEN_GPIO3	General-Purpose Input Debounce Timer Enable 0 = no debounce 1 = debounce time set by DB_CNFG[1:0]		SYSRST = 1	R/W
3	0	DO3	General-Purpose Output Data Output When set for GPO (DIR3 = 0): 0 = GPIO3 is output is logic-low 1 = GPIO3 is output logic-high when set as push-pull output (DRV3 = 1). GPIO3 is high-impedance when set as a and open-drain output (DRV3 = 0).	When set for GPI (DIR3 = 1): DO3 writes are don't care.	SYSRST = 1	R/W
2	0	DRV3	General-Purpose Output Driver Type When set for GPO (DIR3 = 0): 0 = open-drain 1 = Push-Pull	When set for GPI (DIR3 = 1): DRV3 is a don't care when GPI.	SYSRST = 1	R/W
1	1	DI3	GPIO3 Digital Input Value. Irrespective of whether the GPIO3 is set for GPI (DIR3 = 1) or GPO (DIR3 = 0), DI3 reflects the state of GPIO3 . 0 = input logic-low 1 = input logic-high		SYSRST = 1	R
0	1	DIR3	GPIO3 Direction. 0 = General-purpose output (GPO) 1 = General-purpose input (GPI)		SYSRST = 1	R/W

9.2.7 CNFG_GPIO4

Register Name	CNFG_GPIO4
I²C Slave Address	0x48
Register Address	0x54
Reset Value (HEX)	0xF3
Reset Value (BIN)	0b11110011
Reset Condition	SYSRST = 1
Access Type	Mixed
Register Type	Mixed

Bit	Default	Bit Name	Description		Reset	Access Type
7	1	RM_GPIO4	GPIO4 Rising Interrupt Mask 0 = Unmasked. If R_GPIO4 goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to R_GPIO4.		SYSRST = 1	R/W
6	1	FM_GPIO4	GPIO4 Falling Interrupt Mask 0 = Unmasked. If F_GPIO4 goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to F_GPIO4.		SYSRST = 1	R/W
5	1	WK_EN4	General-Purpose Input Wakeup Enable		SYSRST = 1	R/W
4	1	DBEN_GPIO4	General-Purpose Input Debounce Timer Enable 0 = no debounce 1 = debounce time set by DB_CNFG[1:0]		SYSRST = 1	R/W
3	0	DO4	General-Purpose Output Data Output When set for GPO (DIR4 = 0): 0 = GPIO4 is output is logic-low 1 = GPIO4 is output logic-high when set as push-pull output (DRV4 = 1). GPIO4 is high-impedance when set as a and open-drain output (DRV4 = 0).	When set for GPI (DIR4 = 1): DO4 writes are don't care.	SYSRST = 1	R/W
2	0	DRV4	General-Purpose Output Driver Type When set for GPO (DIR4 = 0): 0 = open-drain 1 = Push-Pull	When set for GPI (DIR4 = 1): DRV4 is a don't care when GPI.	SYSRST = 1	R/W
1	1	DI4	GPIO4 Digital Input Value. Irrespective of whether the GPIO4 is set for GPI (DIR4 = 1) or GPO (DIR4 = 0), DI4 reflects the state of GPIO4 . 0 = input logic-low 1 = input logic-high		SYSRST = 1	R
0	1	DIR4	GPIO4 Direction. 0 = General-purpose output (GPO) 1 = General-purpose input (GPI)		SYSRST = 1	R/W

9.2.8 CNFG_GPIO5

Register Name	CNFG_GPIO5
I²C Slave Address	0x48
Register Address	0x55
Reset Value (HEX)	0xF3
Reset Value (BIN)	0b11110011
Reset Condition	SYSRST = 1
Access Type	Mixed
Register Type	Mixed

Bit	Default	Bit Name	Description		Reset	Access Type
7	1	RM_GPIO5	GPIO5 Rising Interrupt Mask 0 = Unmasked. If R_GPIO5 goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to R_GPIO5.		SYSRST = 1	R/W
6	1	FM_GPIO5	GPIO5 Falling Interrupt Mask 0 = Unmasked. If F_GPIO5 goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to F_GPIO5.		SYSRST = 1	R/W
5	1	WK_EN5	General-Purpose Input Wakeup Enable		SYSRST = 1	R/W
4	1	DBEN_GPIO5	General-Purpose Input Debounce Timer Enable 0 = no debounce 1 = debounce time set by DB_CNFG[1:0]		SYSRST = 1	R/W
3	0	DO5	General-Purpose Output Data Output When set for GPO (DIR5 = 0): 0 = GPIO5 is output is logic-low 1 = GPIO5 is output logic-high when set as push-pull output (DRV5 = 1). GPIO5 is high-impedance when set as a and open-drain output (DRV5 = 0).	When set for GPI (DIR5 = 1): DO5 writes are don't care.	SYSRST = 1	R/W
2	0	DRV5	General-Purpose Output Driver Type When set for GPO (DIR5 = 0): 0 = open-drain 1 = Push-Pull	When set for GPI (DIR5 = 1): DRV5 is a don't care when GPI.	SYSRST = 1	R/W
1	1	DI5	GPIO5 Digital Input Value. Irrespective of whether the GPIO5 is set for GPI (DIR5 = 1) or GPO (DIR5 = 0), DI5 reflects the state of GPIO5 . 0 = input logic-low 1 = input logic-high		SYSRST = 1	R
0	1	DIR5	GPIO5 Direction. 0 = General-purpose output (GPO) 1 = General-purpose input (GPI)		SYSRST = 1	R/W

9.2.9 CNFG_GPIO6

Register Name	CNFG_GPIO6
I²C Slave Address	0x48
Register Address	0x56
Reset Value (HEX)	0xF3
Reset Value (BIN)	0b11110011
Reset Condition	SYSRST = 1
Access Type	Mixed
Register Type	Mixed

Bit	Default	Bit Name	Description		Reset	Access Type
7	1	RM_GPIO6	GPIO6 Rising Interrupt Mask 0 = Unmasked. If R_GPIO6 goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to R_GPIO6.		SYSRST = 1	R/W
6	1	FM_GPIO6	GPIO6 Falling Interrupt Mask 0 = Unmasked. If F_GPIO6 goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to F_GPIO6.		SYSRST = 1	R/W
5	1	WK_EN6	General-Purpose Input Wakeup Enable		SYSRST = 1	R/W
4	1	DBEN_GPIO6	General Purpose Input Debounce Timer Enable 0 = no debounce 1 = debounce time set by DB_CNFG[1:0]		SYSRST = 1	R/W
3	0	DO6	General-Purpose Output Data Output When set for GPO (DIR6 = 0): 0 = GPIO6 is output is logic-low 1 = GPIO6 is output logic-high when set as push-pull output (DRV6 = 1). GPIO6 is high-impedance when set as a and open-drain output (DRV6 = 0).	When set for GPI (DIR6 = 1): DO6 writes are don't care.	SYSRST = 1	R/W
2	0	DRV6	General-Purpose Output Driver Type When set for GPO (DIR6 = 0): 0 = open-drain 1 = Push-Pull	When set for GPI (DIR6 = 1): DRV6 is a don't care when GPI.	SYSRST = 1	R/W
1	1	DI6	GPIO6 Digital Input Value. Irrespective of whether the GPIO6 is set for GPI (DIR6 = 1) or GPO (DIR6 = 0), DI6 reflects the state of GPIO6 . 0 = input logic-low 1 = input logic-high		SYSRST = 1	R
0	1	DIR6	GPIO6 Direction. 0 = General-purpose output (GPO) 1 = General-purpose input (GPI)		SYSRST = 1	R/W

9.2.10 CNFG_GPIO7

Register Name	CNFG_GPIO7
I²C Slave Address	0x48
Register Address	0x57
Reset Value (HEX)	0xF3
Reset Value (BIN)	0b11110011
Reset Condition	SYSRST = 1
Access Type	Mixed
Register Type	Mixed

Bit	Default	Bit Name	Description		Reset	Access Type
7	1	RM_GPIO7	GPIO7 Rising Interrupt Mask 0 = Unmasked. If R_GPIO7 goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to R_GPIO7.		SYSRST = 1	R/W
6	1	FM_GPIO7	GPIO7 Falling Interrupt Mask 0 = Unmasked. If F_GPIO7 goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to F_GPIO7.		SYSRST = 1	R/W
5	1	WK_EN7	General-Purpose Input Wakeup Enable		SYSRST = 1	R/W
4	1	DBEN_GPIO7	General Purpose Input Debounce Timer Enable 0 = no debounce 1 = debounce time set by DB_CNFG[1:0]		SYSRST = 1	R/W
3	0	DO7	General-Purpose Output Data Output When set for GPO (DIR7 = 0): 0 = GPIO7 is output is logic-low 1 = GPIO7 is output logic-high when set as push-pull output (DRV7 = 1). GPIO7 is high-impedance when set as a and open-drain output (DRV7 = 0).	When set for GPI (DIR7 = 1): DO7 writes are don't care.	SYSRST = 1	R/W
2	0	DRV7	General-Purpose Output Driver Type When set for GPO (DIR7 = 0): 0 = open-drain 1 = Push-Pull	When set for GPI (DIR7 = 1): DRV7 is a don't care when GPI.	SYSRST = 1	R/W
1	1	DI7	GPIO7 Digital Input Value. Irrespective of whether the GPIO7 is set for GPI (DIR7 = 1) or GPO (DIR7 = 0), DI7 reflects the state of GPIO7 . 0 = input logic-low 1 = input logic-high		SYSRST = 1	R
0	1	DIR7	GPIO7 Direction. 0 = General-purpose output (GPO) 1 = General-purpose input (GPI)		SYSRST = 1	R/W

9.2.11 MR_GPIO_INC

Register Name	MR_GPIO_INC
I²C Slave Address	0x48
Register Address	0x58
Reset Value (HEX)	0x05
Reset Value (BIN)	0b00000101
Reset Condition	SYSRST = 1
Access Type	R/W
Register Type	Mixed

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	MR_INC_GPI7	GPI7 Manual Reset Include	SYSRST = 1	R/W
6	0	MR_INC_GPI6	GPI6 Manual Reset Include	SYSRST = 1	R/W
5	0	MR_INC_GPI5	GPI5 Manual Reset Include	SYSRST = 1	R/W
4	0	MR_INC_GPI4	GPI4 Manual Reset Include	SYSRST = 1	R/W
3	0	MR_INC_GPI3	GPI3 Manual Reset Include	SYSRST = 1	R/W
2	1	MR_INC_GPI2	GPI2 Manual Reset Include	SYSRST = 1	R/W
1	0	MR_INC_GPI1	GPI1 Manual Reset Include	SYSRST = 1	R/W
0	1	MR_INC_GPI0	GPI0 Manual Reset Include	SYSRST = 1	R/W

9.3 Register Descriptions: Charger

9.3.1 INT_CHG

Register Name	INT_CHG
I²C Slave Address	0x48
Register Address	0x01
Reset Value (HEX)	0x00
Reset Value (BIN)	0b00000000
Reset Condition	SYSRST = 1
Access Type	RC
Register Type	Interrupt

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	RESERVED	Reserved. Unutilized bit. Write to 0. Reads are don't care.	SYSRST = 1	RC
6	0	SYS_CNFG_I	System voltage configuration error interrupt 0 = The bit combination in CHG_CV has not been forced to change since the last time this bit was read 1 = The bit combination in CHG_CV has been forced to change to ensure VSYS-REG = VFAST-CHG + 200mV since the last time this bit was read	SYSRST = 1	RC
5	0	SYS_CTRL_I	Minimum System Voltage Regulation-loop related interrupt. This interrupt signals a change in the status bit VSYS_MIN_STAT. 0 = The minimum system voltage regulation loop has not engaged since the last time this bit was read 1 = The minimum system voltage regulation loop has engaged since the last time this bit was read	SYSRST = 1	RC
4	0	CHGIN_CTRL_I	CHGIN control-loop related interrupt. This bit asserts when the input reaches current limit (ICHGIN-LIM) or VCHGIN falls below VCHGIN_MIN 0 = Neither the VCHGIN_MIN_STAT nor the ICHGIN_LIM_STAT bits have changed since the last time this bit was read 1 = The VCHGIN_MIN_STAT or ICHGIN_LIM_STAT bits have changed since the last time this bit was read	SYSRST = 1	RC
3	0	TJ_REG_I	Die junction temperature regulation interrupt. This bit asserts when the die temperature (TJ) exceeds TJ-REG. This interrupt signals a change in the status bit TJ_REG_STAT. 0 = The die temperature has not exceeded TJ-REG since the last time this bit was read 1 = The die temperature has exceeded TJ-REG since the last time this bit was read	SYSRST = 1	RC
2	0	CHGIN_I	CHGIN related interrupt 0 = The bits in CHGIN_DTLS have not changed since the last time this bit was read 1 = The bits in CHGIN_DTLS have changed since the last time this bit was read	SYSRST = 1	RC
1	0	CHG_I	Charger related interrupt 0 = The bits in CHG_DTLS have not changed since the last time this bit was read 1 = The bits in CHG_DTLS have changed since the last time this bit was read	SYSRST = 1	RC
0	0	THM_I	Thermistor related interrupt 0 = The bits in THM_DTLS have not changed since the last time this bit was read 1 = The bits in THM_DTLS have changed since the last time this bit was read	SYSRST = 1	RC

9.3.2 INT_M_CHG

Register Name	INT_M_CHG
I²C Slave Address	0x48
Register Address	0x09
Reset Value (HEX)	0xFF
Reset Value (BIN)	0b11111111
Reset Condition	SYSRST = 1
Access Type	R/W
Register Type	Interrupt Mask

Bit	Default	Bit Name	Description	Reset	Access Type
7	1	RESERVED	Reserved. Unutilized bit. Write to 0. Reads are don't care.	SYSRST = 1	R/W
6	1	SYS_CNFG_M	Setting this bit prevents the SYS_CNFG_I bit from causing hardware IRQs 0 = SYS_CNFG_I is not masked 1 = SYS_CNFG_I is masked	SYSRST = 1	R/W
5	1	SYS_CTRL_M	Setting this bit prevents the SYS_CTRL_I bit from causing hardware IRQs 0 = SYS_CTRL_I is not masked 1 = SYS_CTRL_I is masked	SYSRST = 1	R/W
4	1	CHGIN_CTRL_M	Setting this bit prevents the CHGIN_CTRL_I bit from causing hardware IRQs 0 = CHGIN_CTRL_I is not masked 1 = CHGIN_CTRL_I is masked	SYSRST = 1	R/W
3	1	TJ_REG_M	Setting this bit prevents the TJREG_I bit from causing hardware IRQs 0 = TJREG_I is not masked 1 = TJREG_I is masked	SYSRST = 1	R/W
2	1	CHGIN_M	Setting this bit prevents the CHGIN_I bit from causing hardware IRQs 0 = CHGIN_I is not masked 1 = CHGIN_I is masked	SYSRST = 1	R/W
1	1	CHG_M	Setting this bit prevents the CHG_I bit from causing hardware IRQs 0 = CHG_I is not masked 1 = CHG_I is masked	SYSRST = 1	R/W
0	1	THM_M	Setting this bit prevents the THM_I bit from causing hardware IRQs 0 = THM_I is not masked 1 = THM_I is masked	SYSRST = 1	R/W

9.3.3 STAT_CHG_A

Register Name	STAT_CHG_A
I²C Slave Address	0x48
Register Address	0x04
Reset Value (HEX)	0x00
Reset Value (BIN)	0b00000000
Reset Condition	CHGPOK
Access Type	R
Register Type	Status

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	RESERVED	Reserved. Unutilized bit. Write to 0. Reads are don't care.	CHGPOK	R
6	0	VCHGIN_MIN_STAT	Minimum Input Voltage Regulation Loop Status 0 = The minimum CHGIN voltage regulation loop is not engaged 1 = The minimum CHGIN voltage regulation loop has engaged to regulate VCHGIN >= VCHGIN-MIN	CHGPOK	R
5	0	ICHGIN_LIM_STAT	Input Current Limit Loop Status 0 = The CHGIN current limit loop is not engaged 1 = The CHGIN current limit loop has engaged to regulate ICHGIN <= ICHGIN-LIM	CHGPOK	R
4	0	VSYS_MIN_STAT	Minimum System Voltage Regulation Loop Status 0 = The minimum system voltage regulation loop is not engaged 1 = The minimum system voltage regulation loop is engaged to regulate VSYS >= VSYS-MIN	CHGPOK	R
3	0	TJ_REG_STAT	Maximum Junction Temperature Regulation Loop Status 0 = The maximum junction temperature regulation loop is not engaged 1 = The maximum junction temperature regulation loop has engaged to regulate the junction temperature less than TJ-REG	CHGPOK	R
2	0	THM_DTLS[2:0]	Battery Temperature Details 0b000 = Thermistor is disabled (THM_EN = 0) 0b001 = Battery is cold as programmed by THM_COLD[1:0] If thermistor and charger are enabled while the battery is cold, a battery temperature fault occurs. 0b010 = Battery is cool as programmed by THM_COOL[1:0] 0b011 = Battery is warm as programed by THM_WARM[1:0] 0b100 = Battery is hot as programmed by THM_HOT[1:0]. If thermistor and charger are enabled while the battery is hot, a battery temperature fault occurs. 0b101 = Battery is in the normal temperature region as programmed by the THM_CONTROL register 0b110-0b111 = reserved	CHGPOK	R
1	0			CHGPOK	R
0	0			CHGPOK	R

9.3.4 STAT_CHG_B

Register Name	STAT_CHG_B
I²C Slave Address	0x48
Register Address	0x05
Reset Value (HEX)	0x00
Reset Value (BIN)	0b00000000
Reset Condition	CHGPOK
Access Type	R
Register Type	Status

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	CHG_DTLS[3:0]	Charger Details 0b0000 = Charger is off (CHG_EN = 0 or charger input is invalid or battery is not low by Vrestart) 0b0001 = Charger is in prequalification mode 0b0010 = Charger is in fast-charge constant-current (CC) mode 0b0011 = Charger is in JEITA modified fast-charge constant-current mode 0b0100 = Charger is in fast-charge constant-voltage (CV) mode 0b0101 = Charger is in JEITA modified fast-charge constant-voltage mode 0b0110 = Charger is in top-off mode 0b0111 = Charger is in JEITA modified top-off mode 0b1000 = Charger is done 0b1001 = Charger is JEITA modified done (done was entered through the JEITA-modified fast-charge states) 0b1010 = Charger is suspended due to a prequalification timer fault 0b1011 = Charger is suspended due to a fast-charge timer fault 0b1100 = Charger is suspended due to a battery temperature fault 0b1101-0b1111 = reserved	CHGPOK	R
6	0			CHGPOK	R
5	0			CHGPOK	R
4	0			CHGPOK	R
3	0	CHGIN_DTLS[1:0]	CHGIN Status Details 0b00 = The CHGIN input voltage is below the UVLO threshold (VCHGIN < VUVLO) 0b01 = The CHGIN input voltage is above the OVP threshold (VCHGIN > VOVP) 0b10 = The CHGIN input is being debounced (no power accepted from CHGIN during debounce) 0b11 = The CHGIN input is okay and debounced	CHGPOK	R
2	0			CHGPOK	R
1	0	CHG	Quick Charger Status 0 = Charging is not happening 1 = Charging is happening	CHGPOK	R
0	0	TIME_SUS	Time Suspend Indicator 0 = The charger's timers are either not active, or not suspended 1 = The charger's active timer is suspended due to one of three reasons: the charge current has dropped below 20% of IFAST-CHG while the charger state machine is in FAST CHARGE CC mode, the charger is in SUPPLIMENT mode, or the charger state machine is in BATTERY TEMPERATURE FAULT mode.	CHGPOK	R

9.3.5 CNFG_CHG_A

Register Name	CNFG_CHG_A
I²C Slave Address	0x48
Register Address	0x18
Reset Value (HEX)	0x0F
Reset Value (BIN)	0b00001111
Reset Condition	SYSRST = 1
Access Type	R/W
Register Type	Configuration

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	THM_HOT[1:0]	Sets the VHOT JEITA Temperature Threshold 0b00 = VHOT = 0.411V 0b01 = VHOT = 0.367V 0b10 = VHOT = 0.327V 0b11 = VHOT = 0.291V	SYSRST = 1	R/W
6	0			SYSRST = 1	R/W
5	0	THM_WARM[1:0]	Sets the VWARM JEITA Temperature Threshold 0b00 = VWARM = 0.511V 0b01 = VWARM = 0.459V 0b10 = VWARM = 0.411V 0b11 = VWARM = 0.367V	SYSRST = 1	R/W
4	0			SYSRST = 1	R/W
3	1	THM_COOL[1:0]	Sets the VCOOL JEITA Temperature Threshold 0b00 = VCOOL = 0.923V 0b01 = VCOOL = 0.867V 0b10 = VCOOL = 0.807V 0b11 = VCOOL = 0.747V	SYSRST = 1	R/W
2	1			SYSRST = 1	R/W
1	1	THM_COLD[1:0]	Sets the VCOLD JEITA Temperature Threshold 0b00 = VCOLD = 1.024V 0b01 = VCOLD = 0.976V 0b10 = VCOLD = 0.923V 0b11 = VCOLD = 0.867V	SYSRST = 1	R/W
0	1			SYSRST = 1	R/W

9.3.6 CNFG_CHG_B

Register Name	CNFG_CHG_B
I²C Slave Address	0x48
Register Address	0x19
Reset Value (HEX)	OTP
Reset Value (BIN)	0b0000000x
Reset Condition	Mixed
Access Type	R/W
Register Type	Configuration

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	VCHGIN_MIN[2:0]	Minimum CHGIN regulation voltage ($V_{CHGIN-MIN}$)	SYSRST = 1	R/W
6	0		0b000 = 4.0V 0b010 = 4.2V 0b100 = 4.4V 0b110 = 4.6V	SYSRST = 1	R/W
5	0		0b001 = 4.1V 0b011 = 4.3V 0b101 = 4.5V 0b111 = 4.7V	SYSRST = 1	R/W
4	0	ICHGIN_LIM[2:0]	CHGIN Input Current Limit ($I_{CHGIN-LIM}$)	CHGPOK	R/W
3	0		0b000 = 95mA 0b001 = 190mA 0b010 = 285mA 0b011 = 380mA 0b100 = 475mA	CHGPOK	R/W
2	0		0b101 to 0b111 = Reserved values that result in 475mA. If 475mA is desired, please use the 0b100 setting.	CHGPOK	R/W
1	0	I_PQ	Sets the prequalification charge current (IPQ) as a percentage of IFAST-CHG 0 = 10% 1 = 20%	SYSRST = 1	R/W
0	x	CHG_EN	Charger Enable 0 = the battery charger is disabled 1 = the battery charger is enabled	SYSRST = 1	R/W

9.3.7 CNFG_CHG_C

Register Name	CNFG_CHG_C
I²C Slave Address	0x48
Register Address	0x1A
Reset Value (HEX)	0xF8
Reset Value (BIN)	0b11111000
Reset Condition	SYSRST = 1
Access Type	R/W
Register Type	Configuration

Bit	Default	Bit Name	Description	Reset	Access Type
7	1	CHG_PQ[2:0]	Battery prequalification voltage threshold (V_{PQ}) 0b000 = 2.3V 0b010 = 2.5V 0b100 = 2.7V 0b110 = 2.9V 0b001 = 2.4V 0b011 = 2.6V 0b101 = 2.8V 0b111 = 3.0V	SYSRST = 1	R/W
6	1			SYSRST = 1	R/W
5	1			SYSRST = 1	R/W
4	1	I_TERM[1:0]	Charger Termination Current (I_{TERM}). I_TERM[1:0] sets the charger termination current as a percentage of the fast charge current $I_{FAST-CHG}$. 00 = 5% 01 = 7.5% 10 = 10% 11 = 15%	SYSRST = 1	R/W
3	1			SYSRST = 1	R/W
2	0	T_TOPOFF[2:0]	Top-off timer value (t_{TO}) 0b000 = 0 minutes 0b010 = 10 minutes 0b100 = 20 minutes 0b110 = 30 minutes 0b001 = 5 minutes 0b011 = 15 minutes 0b101 = 25 minutes 0b111 = 35 minutes	SYSRST = 1	R/W
1	0			SYSRST = 1	R/W
0	0			SYSRST = 1	R/W

9.3.8 CNFG_CHG_D

Register Name	CNFG_CHG_D
I²C Slave Address	0x48
Register Address	0x1B
Reset Value (HEX)	0x10
Reset Value (BIN)	0b00010000
Reset Condition	SYSRST = 1
Access Type	R/W
Register Type	Configuration

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	TJ_REG[2:0]	Sets the die junction temperature regulation point, T_{J_REG}. 0b000 = 60°C 0b010 = 80°C 0b100 = 100°C 0b110 = 100°C 0b001 = 70°C 0b011 = 90°C 0b101 = 100°C 0b111 = 100°C	SYSRST = 1	R/W
6	0			SYSRST = 1	R/W
5	0			SYSRST = 1	R/W
4	1	VSYS_REG[4:0]	System Voltage Regulation (V_{SYS_REG}) This 5-bit configuration is a linear transfer function that starts at 4.1V and ends at 4.8V, with 25mV increments. See the *VSYS_REG Code Table* for a complete table of values. Program VSYS_REG to at least 200mV above the higher of CHG_CV and CHG_CV_JEITA. See the *Managing VSYS_REG, CHG_CV, and CHG_CV_JEITA* section of this programmer's guide for more information.	SYSRST = 1	R/W
3	0			SYSRST = 1	R/W
2	0			SYSRST = 1	R/W
1	0			SYSRST = 1	R/W
0	0			SYSRST = 1	R/W

9.3.9 VSYS_REG Code Table

0x00=0b00000=4.100V	0x10=0b10000=4.500V
0x01=0b00001=4.125V	0x11=0b10001=4.525V
0x02=0b00010=4.150V	0x12=0b10010=4.550V
0x03=0b00011=4.175V	0x13=0b10011=4.575V
0x04=0b00100=4.200V	0x14=0b10100=4.600V
0x05=0b00101=4.225V	0x15=0b10101=4.625V
0x06=0b00110=4.250V	0x16=0b10110=4.650V
0x07=0b00111=4.275V	0x17=0b10111=4.675V
0x08=0b01000=4.300V	0x18=0b11000=4.700V
0x09=0b01001=4.325V	0x19=0b11001=4.725V
0x0A=0b01010=4.350V	0x1A=0b11010=4.750V
0x0B=0b01011=4.375V	0x1B=0b11011=4.775V
0x0C=0b01100=4.400V	0x1C=0b11100=4.800V
0x0D=0b01101=4.425V	0x1D=0b11101=4.800V
0x0E=0b01110=4.450V	0x1E=0b11110=4.800V
0x0F=0b01111=4.475V	0x1F=0b11111=4.800V

See the Managing VSYS_REG, CHG_CV, and CHG_CV_JEITA section of the Programmer's Guide for more information.

9.3.10 CNFG_CHG_E

Register Name	CNFG_CHG_E
I²C Slave Address	0x48
Register Address	0x1C
Reset Value (HEX)	0x05
Reset Value (BIN)	0b00000101
Reset Condition	SYSRST = 1
Access Type	R/W
Register Type	Configuration

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	CHG_CC[5:0]	Sets the fast-charge constant current value, $I_{FAST-CHG}$. This 6-bit configuration is a linear transfer function that starts at 7.5mA and ends at 300mA, with 7.5mA increments. See the *CHG_CC and CHG_CC_JEITA Code Table* for a complete table of values.	SYSRST = 1	R/W
6	0			SYSRST = 1	R/W
5	0			SYSRST = 1	R/W
4	0			SYSRST = 1	R/W
3	0			SYSRST = 1	R/W
2	1			SYSRST = 1	R/W
1	0	T_FAST_CHG[1:0]	Sets the fast-charge safety timer, t_{FC}. 0b00 = timer disabled 0b01 = 3 hours 0b10 = 5 hours 0b11 = 7 hours	SYSRST = 1	R/W
0	1			SYSRST = 1	R/W

9.3.11 CHG_CC and CHG_CC_JEITA Code Table

0x00=0b000000=7.5mA	0x10=0b010000=127.5mA	0x20=0b100000=247.5mA	0x30=0b110000=300.0mA
0x01=0b000001=15.0mA	0x11=0b010001=135.0mA	0x21=0b100001=255.0mA	0x31=0b110001=300.0mA
0x02=0b000010=22.5mA	0x12=0b010010=142.5mA	0x22=0b100010=262.5mA	0x32=0b110010=300.0mA
0x03=0b000011=30.0mA	0x13=0b010011=150.0mA	0x23=0b100011=270.0mA	0x33=0b110011=300.0mA
0x04=0b000100=37.5mA	0x14=0b010100=157.5mA	0x24=0b100100=277.5mA	0x34=0b110100=300.0mA
0x05=0b000101=45.0mA	0x15=0b010101=165.0mA	0x25=0b100101=285.0mA	0x35=0b110101=300.0mA
0x06=0b000110=52.5mA	0x16=0b010110=172.5mA	0x26=0b100110=292.5mA	0x36=0b110110=300.0mA
0x07=0b000111=60.0mA	0x17=0b010111=180.0mA	0x27=0b100111=300.0mA	0x37=0b110111=300.0mA
0x08=0b001000=67.5mA	0x18=0b011000=187.5mA	0x28=0b101000=300.0mA	0x38=0b111000=300.0mA
0x09=0b001001=75.0mA	0x19=0b011001=195.0mA	0x29=0b101001=300.0mA	0x39=0b111001=300.0mA
0x0A=0b001010=82.5mA	0x1A=0b011010=202.5mA	0x2A=0b101010=300.0mA	0x3A=0b111010=300.0mA
0x0B=0b001011=90.0mA	0x1B=0b011011=210.0mA	0x2B=0b101011=300.0mA	0x3B=0b111011=300.0mA
0x0C=0b001100=97.5mA	0x1C=0b011100=217.5mA	0x2C=0b101100=300.0mA	0x3C=0b111100=300.0mA
0x0D=0b001101=105.0mA	0x1D=0b011101=225.0mA	0x2D=0b101101=300.0mA	0x3D=0b111101=300.0mA
0x0E=0b001110=112.5mA	0x1E=0b011110=232.5mA	0x2E=0b101110=300.0mA	0x3E=0b111110=300.0mA
0x0F=0b001111=120.0mA	0x1F=0b011111=240.0mA	0x2F=0b101111=300.0mA	0x3F=0b111111=300.0mA

9.3.12 CNFG_CHG_F

Register Name	CNFG_CHG_F
I²C Slave Address	0x48
Register Address	0x1D
Reset Value (HEX)	0x04
Reset Value (BIN)	0b00000100
Reset Condition	SYSRST = 1
Access Type	R/W
Register Type	Configuration

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	CHG_CC_JEITA[5:0]	Sets $I_{FAST-CHG\_JEITA}$ for when the battery is either cool or warm as defined by the TCOOL and TWARM temperature thresholds. This register is a don't care if the battery temperature is normal. This 6-bit configuration is a linear transfer function that starts at 7.5mA and ends at 300mA, with 7.5mA increments. See the *CHG_CC and CHG_CC_JEITA Code Table* for a complete table of values.	SYSRST = 1	R/W
6	0			SYSRST = 1	R/W
5	0			SYSRST = 1	R/W
4	0			SYSRST = 1	R/W
3	0			SYSRST = 1	R/W
2	1			SYSRST = 1	R/W
1	0	THM_EN	Thermistor enable bit 0 = The charger does not enable the thermistor bias and battery temperature is ignored by charger logic 1 = The charger enables the thermistor and continuously monitors battery temperature	SYSRST = 1	R/W
0	0	RESERVED	Reserved. This bit is reserved. Writes to this bit should be 0.	SYSRST = 1	R/W

9.3.13 CNFG_CHG_G

Register Name	CNFG_CHG_G
I²C Slave Address	0x48
Register Address	0x1E
Reset Value (HEX)	0x00
Reset Value (BIN)	0b00000000
Reset Condition	Mixed
Access Type	R/W
Register Type	Configuration

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	CHG_CV[5:0]	Sets fast-charge battery regulation voltage, $V_{FAST-CHG}$. This 6-bit configuration is a linear transfer function that starts at 3.6V and ends at 4.6V, with 25mV increments. See the *CHG_CV and CHG_CV_JEITA Code Table* for a complete table of values. Program VSYS_REG to at least 200mV above the higher of CHG_CV and CHG_CV_JEITA. See the *Managing VSYS_REG, CHG_CV, and CHG_CV_JEITA* section of this programmer's guide for more information.	SYSRST = 1	R/W
6	0			SYSRST = 1	R/W
5	0			SYSRST = 1	R/W
4	0			SYSRST = 1	R/W
3	0			SYSRST = 1	R/W
2	0			SYSRST = 1	R/W
1	0	USBS	Setting this bit places CHGIN in USB suspend mode 0 = CHGIN is not suspended and can draw current from an adapter source. 1 = CHGIN is suspended and can draw no current from an adapter source. Note: USBS = 1 results in CHGIN_I interrupt **and** CHGIN_DTLS = 0b00.	CHGPOR = 1	R/W
0	0	RESERVED	Reserved. Unutilized bit. Write to 0. Reads are don't care.	CHGPOR = 1	R/W

9.3.14 CHG_CV and CHG_CV_JEITA Code Table

0x00=0b000000=3.600V	0x10=0b010000=4.000V	0x20=0b100000=4.400V	0x30=0b110000=4.600V
0x01=0b000001=3.625V	0x11=0b010001=4.025V	0x21=0b100001=4.425V	0x31=0b110001=4.600V
0x02=0b000010=3.650V	0x12=0b010010=4.050V	0x22=0b100010=4.450V	0x32=0b110010=4.600V
0x03=0b000011=3.675V	0x13=0b010011=4.075V	0x23=0b100011=4.475V	0x33=0b110011=4.600V
0x04=0b000100=3.700V	0x14=0b010100=4.100V	0x24=0b100100=4.500V	0x34=0b110100=4.600V
0x05=0b000101=3.725V	0x15=0b010101=4.125V	0x25=0b100101=4.525V	0x35=0b110101=4.600V
0x06=0b000110=3.750V	0x16=0b010110=4.150V	0x26=0b100110=4.550V	0x36=0b110110=4.600V
0x07=0b000111=3.775V	0x17=0b010111=4.175V	0x27=0b100111=4.575V	0x37=0b110111=4.600V
0x08=0b001000=3.800V	0x18=0b011000=4.200V	0x28=0b101000=4.600V	0x38=0b111000=4.600V
0x09=0b001001=3.825V	0x19=0b011001=4.225V	0x29=0b101001=4.600V	0x39=0b111001=4.600V
0x0A=0b001010=3.850V	0x1A=0b011010=4.250V	0x2A=0b101010=4.600V	0x3A=0b111010=4.600V
0x0B=0b001011=3.875V	0x1B=0b011011=4.275V	0x2B=0b101011=4.600V	0x3B=0b111011=4.600V
0x0C=0b001100=3.900V	0x1C=0b011100=4.300V	0x2C=0b101100=4.600V	0x3C=0b111100=4.600V
0x0D=0b001101=3.925V	0x1D=0b011101=4.325V	0x2D=0b101101=4.600V	0x3D=0b111101=4.600V
0x0E=0b001110=3.950V	0x1E=0b011110=4.350V	0x2E=0b101110=4.600V	0x3E=0b111110=4.600V
0x0F=0b001111=3.975V	0x1F=0b011111=4.375V	0x2F=0b101111=4.600V	0x3F=0b111111=4.600V

See the Managing VSYS_REG, CHG_CV, and CHG_CV_JEITA *section of this programmer's guide for more information.*

9.3.15 CNFG_CHG_H

Register Name	CNFG_CHG_H
I²C Slave Address	0x48
Register Address	0x1F
Reset Value (HEX)	0x00
Reset Value (BIN)	0b00000000
Reset Condition	SYSRST = 1
Access Type	R/W
Register Type	Configuration

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	CHG_CV_JEITA[5:0]	Sets the modified $V_{FAST-CHG}$ for when the battery is either cool or warm as defined by the TCOOL and TWARM temperature thresholds. This register is a don't care if the battery temperature is normal. This 6-bit configuration is a linear transfer function that starts at 3.6V and ends at 4.6V, with 25mV increments. See the *CHG_CV and CHG_CV_JEITA Code Table* for a complete table of values. Program VSYS_REG to at least 200mV above the higher of CHG_CV and CHG_CV_JEITA. See the *Managing VSYS_REG, CHG_CV, and CHG_CV_JEITA* section of this programmer's guide for more information.	SYSRST = 1	R/W
6	0			SYSRST = 1	R/W
5	0			SYSRST = 1	R/W
4	0			SYSRST = 1	R/W
3	0			SYSRST = 1	R/W
2	0			SYSRST = 1	R/W
1	0	RESERVED	Reserved. Unutilized bit. Write to 0. Reads are don't care.	SYSRST = 1	R/W
0	0	RESERVED	Reserved. Unutilized bit. Write to 0. Reads are don't care.	SYSRST = 1	R/W

9.3.16 CNFG_CHG_I

Register Name	CNFG_CHG_I
I²C Slave Address	0x48
Register Address	0x20
Reset Value (HEX)	0xF0
Reset Value (BIN)	0b11110000
Reset Condition	SYSRST = 1
Access Type	R/W
Register Type	Configuration

Bit	Default	Bit Name	Description	Reset	Access Type
7	1	IMON_DISCHG_SCALE[3:0]	Selects the battery discharge current full-scale current value This 4-bit configuration starts at 7.5mA and ends at 300mA. See the *IMON_DISCHG_SCALE Code Table* for a complete table of values.	SYSRST = 1	R/W
6	1			SYSRST = 1	R/W
5	1			SYSRST = 1	R/W
4	1			SYSRST = 1	R/W
3	0	MUX_SEL[3:0]	Selects the analog channel to connect to AMUX: Note that for the AMUX to operate the on/off controller must be in either its "On via Software" or "On via On/Off Controller" state. 0b0000 = Multiplexer is disabled and AMUX is high-impedance. 0b0001 = CHGIN voltage monitor. 0b0010 = CHGIN current monitor. 0b0011 = BATT voltage monitor. 0b0100 = BATT charge current monitor. Valid only while battery charging is happening (CHG = 1). 0b0101 = BATT discharge current monitor normal measurement. 0b0110 = BATT discharge current monitor nulling measurement. 0b0111 = THM voltage monitor 0b1000 = TBIAS voltage monitor 0b1001 = AGND voltage monitor (through 100Ω pulldown resistor) 0b1010-0b1111 = SYS voltage monitor Note that the multiplexer consumes current unless it is in the 0b0000 state. When measurements are not needed, make sure to configure MUX_SEL[3:0] = 0b0000.	SYSRST = 1	R/W
2	0			SYSRST = 1	R/W
1	0			SYSRST = 1	R/W
0	0			SYSRST = 1	R/W

9.3.17 IMON_DISCHG_SCALE Code Table

0x00=0b0000=8.2mA	0x08=0b1000=251.2mA
0x01=0b0001=40.5mA	0x09=0b1001=279.3mA
0x02=0b0010=72.3mA	0x0A=0b1010=300.0mA
0x03=0b0011=103.4mA	0x0B=0b1011=300.0mA
0x04=0b0100=134.1mA	0x0C=0b1100=300.0mA
0x05=0b0101=164.1mA	0x0D=0b1101=300.0mA
0x06=0b0110=193.7mA	0x0E=0b1110=300.0mA
0x07=0b0111=222.7mA	0x0F=0b1111=300.0mA

9.4 Register Descriptions: LDO

9.4.1 CNFG_LDO_A

Register Name	CNFG_LDO_A
I²C Slave Address	0x48
Register Address	0x38
Reset Value (HEX)	OTP
Reset Value (BIN)	0b1xxxxxxx
Reset Condition	SYSRST = 1
Access Type	R/W
Register Type	Configuration

Bit	Default	Bit Name	Description	Reset	Access Type
7	1	RESERVED	Reserved. Unutilized bit. Write to 1. Reads are don't care.	SYSRST = 1	R/W
6	x	TV_LDO[6:0]	LDO Target Output Voltage This 7-bit configuration is a linear transfer function that starts at 3.7125V and ends at 5.3000V, with 12.5mV increments. See the *TV_LDO Code Table* for a complete table of values.	SYSRST = 1	R/W
5	x			SYSRST = 1	R/W
4	x			SYSRST = 1	R/W
3	x			SYSRST = 1	R/W
2	x			SYSRST = 1	R/W
1	x			SYSRST = 1	R/W
0	x			SYSRST = 1	R/W

9.4.2 TV_LDO Code Table

0x00 = 0b0000000 = 3.7125	0x20 = 0b0100000 = 4.1125	0x40 = 0b1000000 = 4.5125	0x60 = 0b1100000 = 4.9125
0x01 = 0b0000001 = 3.7250	0x21 = 0b0100001 = 4.1250	0x41 = 0b1000001 = 4.5250	0x61 = 0b1100001 = 4.9250
0x02 = 0b0000010 = 3.7375	0x22 = 0b0100010 = 4.1375	0x42 = 0b1000010 = 4.5375	0x62 = 0b1100010 = 4.9375
0x03 = 0b0000011 = 3.7500	0x23 = 0b0100011 = 4.1500	0x43 = 0b1000011 = 4.5500	0x63 = 0b1100011 = 4.9500
0x04 = 0b0000100 = 3.7625	0x24 = 0b0100100 = 4.1625	0x44 = 0b1000100 = 4.5625	0x64 = 0b1100100 = 4.9625
0x05 = 0b0000101 = 3.7750	0x25 = 0b0100101 = 4.1750	0x45 = 0b1000101 = 4.5750	0x65 = 0b1100101 = 4.9750
0x06 = 0b0000110 = 3.7875	0x26 = 0b0100110 = 4.1875	0x46 = 0b1000110 = 4.5875	0x66 = 0b1100110 = 4.9875
0x07 = 0b0000111 = 3.8000	0x27 = 0b0100111 = 4.2000	0x47 = 0b1000111 = 4.6000	0x67 = 0b1100111 = 5.0000
0x08 = 0b0001000 = 3.8125	0x28 = 0b0101000 = 4.2125	0x48 = 0b1001000 = 4.6125	0x68 = 0b1101000 = 5.0125
0x09 = 0b0001001 = 3.8250	0x29 = 0b0101001 = 4.2250	0x49 = 0b1001001 = 4.6250	0x69 = 0b1101001 = 5.0250
0x0A = 0b0001010 = 3.8375	0x2A = 0b0101010 = 4.2375	0x4A = 0b1001010 = 4.6375	0x6A = 0b1101010 = 5.0375
0x0B = 0b0001011 = 3.8500	0x2B = 0b0101011 = 4.2500	0x4B = 0b1001011 = 4.6500	0x6B = 0b1101011 = 5.0500
0x0C = 0b0001100 = 3.8625	0x2C = 0b0101100 = 4.2625	0x4C = 0b1001100 = 4.6625	0x6C = 0b1101100 = 5.0625
0x0D = 0b0001101 = 3.8750	0x2D = 0b0101101 = 4.2750	0x4D = 0b1001101 = 4.6750	0x6D = 0b1101101 = 5.0750
0x0E = 0b0001110 = 3.8875	0x2E = 0b0101110 = 4.2875	0x4E = 0b1001110 = 4.6875	0x6E = 0b1101110 = 5.0875
0x0F = 0b0001111 = 3.9000	0x2F = 0b0101111 = 4.3000	0x4F = 0b1001111 = 4.7000	0x6F = 0b1101111 = 5.1000
0x10 = 0b0010000 = 3.9125	0x30 = 0b0110000 = 4.3125	0x50 = 0b1010000 = 4.7125	0x70 = 0b1110000 = 5.1125
0x11 = 0b0010001 = 3.9250	0x31 = 0b0110001 = 4.3250	0x51 = 0b1010001 = 4.7250	0x71 = 0b1110001 = 5.1250
0x12 = 0b0010010 = 3.9375	0x32 = 0b0110010 = 4.3375	0x52 = 0b1010010 = 4.7375	0x72 = 0b1110010 = 5.1375
0x13 = 0b0010011 = 3.9500	0x33 = 0b0110011 = 4.3500	0x53 = 0b1010011 = 4.7500	0x73 = 0b1110011 = 5.1500
0x14 = 0b0010100 = 3.9625	0x34 = 0b0110100 = 4.3625	0x54 = 0b1010100 = 4.7625	0x74 = 0b1110100 = 5.1625
0x15 = 0b0010101 = 3.9750	0x35 = 0b0110101 = 4.3750	0x55 = 0b1010101 = 4.7750	0x75 = 0b1110101 = 5.1750
0x16 = 0b0010110 = 3.9875	0x36 = 0b0110110 = 4.3875	0x56 = 0b1010110 = 4.7875	0x76 = 0b1110110 = 5.1875
0x17 = 0b0010111 = 4.0000	0x37 = 0b0110111 = 4.4000	0x57 = 0b1010111 = 4.8000	0x77 = 0b1110111 = 5.2000
0x18 = 0b0011000 = 4.0125	0x38 = 0b0111000 = 4.4125	0x58 = 0b1011000 = 4.8125	0x78 = 0b1111000 = 5.2125
0x19 = 0b0011001 = 4.0250	0x39 = 0b0111001 = 4.4250	0x59 = 0b1011001 = 4.8250	0x79 = 0b1111001 = 5.2250
0x1A = 0b0011010 = 4.0375	0x3A = 0b0111010 = 4.4375	0x5A = 0b1011010 = 4.8375	0x7A = 0b1111010 = 5.2375
0x1B = 0b0011011 = 4.0500	0x3B = 0b0111011 = 4.4500	0x5B = 0b1011011 = 4.8500	0x7B = 0b1111011 = 5.2500
0x1C = 0b0011100 = 4.0625	0x3C = 0b0111100 = 4.4625	0x5C = 0b1011100 = 4.8625	0x7C = 0b1111100 = 5.2625
0x1D = 0b0011101 = 4.0750	0x3D = 0b0111101 = 4.4750	0x5D = 0b1011101 = 4.8750	0x7D = 0b1111101 = 5.2750
0x1E = 0b0011110 = 4.0875	0x3E = 0b0111110 = 4.4875	0x5E = 0b1011110 = 4.8875	0x7E = 0b1111110 = 5.2875
0x1F = 0b0011111 = 4.1000	0x3F = 0b0111111 = 4.5000	0x5F = 0b1011111 = 4.9000	0x7F = 0b1111111 = 5.3000

9.4.3 CNFG_LDO_B

Register Name	CNFG_LDO_B
I²C Slave Address	0x48
Register Address	0x39
Reset Value (HEX)	OTP
Reset Value (BIN)	0b0000xxxx
Reset Condition	SYSRST = 1
Access Type	R/W
Register Type	Configuration

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	SYSRST = 1	R/W
6	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	SYSRST = 1	R/W
5	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	SYSRST = 1	R/W
4	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	SYSRST = 1	R/W
3	x	ADE_LDO	LDO Active-Discharge Enable 0 = The active discharge function is disabled. When LDO is disabled, it's discharge rate is a function of the output capacitance and the external load. 1 = The active discharge function is enabled. When LDO is disabled, an internal resistor (R_{AD_LDO}) is activated from LDO to GND to help the output voltage discharge. The output voltage discharge rate is a function of the output capacitance, the external loading, and the internal R_{AD_LDO} load.	SYSRST = 1	R/W
2	x	EN_LDO[2:0]	Enable Control for LDO 0b000 = LDO powers-up and powers-down in FPS slot 0 0b001 = LDO powers-up and powers-down in FPS slot 1 0b010 = LDO powers-up and powers-down in FPS slot 2 0b011 = LDO powers-up and powers-down in FPS slot 3 0b100 = LDO is off irrespective of FPS 0b101 = same as 0b100 0b110 = LDO is on irrespective of FPS whenever the on/off controller is in its "On via Software" or "On via On/Off Controller" states. 0b111 = same as 0b110	SYSRST = 1	R/W
1	x			SYSRST = 1	R/W
0	x			SYSRST = 1	R/W

9.5 Register Descriptions: SIMO Buck Boost

9.5.1 CNFG_SBB_TOP

Register Name	CNFG_SBB_TOP
I²C Slave Address	function of ADDR OTP bit
Register Address	0x28
Reset Value (HEX)	OTP
Reset Value (BIN)	0bxxxxxxxx
Reset Condition	SYSRST = 1
Access Type	R/W
Register Type	Configuration

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	RESERVED	Reserved. Unutilized bit. Write to 0. Reads are don't care.	SYSRST = 1	R/W
6	x	MRT_OTP	Manual Reset Debounce Time 0 = 16s 1 = 8s	SYSRST = 1	R/W
5	x	GPIO_MRT[1:0]	GPIO Manual Reset Debounce Time 0b00 = 10.0s 0b01 = 5.0s 0b10 = 2.5s 0b11 = 1.25s	SYSRST = 1	R/W
4					
3	x	CNFG_SBB[1:0]	SIMO Buck-Boost Sample Clock Configuration 0b00 = Normal operation. Default sample clocks. Elements are sampled at 625Hz. 0b01 = Force hold mode for all clocks. This setting is for debugging purposes. If in hold mode for long periods of time (>10ms) then hold caps start to droop. 0b10 = Force sample mode for all clocks. This setting could potentially be used by a production device for higher performance. It has good performance at the cost of higher current. 0b11 = Sample clocks normal. Force feedback comparators into the SLOW mode. This setting could potentially be used by a production device if the SBBx loads are all very small (i.e., <30mA). By forcing the SLOW mode, performance is degraded but we also save Iq.	SYSRST = 1	R/W
2	x			SYSRST = 1	R/W
1	x	DRV_SBB[1:0]	SIMO Buck-Boost (all channels) Drive Strength Trim. The ideal value of this register should be determined experimentally for each platform. The 0b01 setting is the best setting for a PCB layout that is comparable to maxim's own EVKIT and represents a balance between efficiency and EMI. The faster setting can result in higher efficiency but generally requires a tighter EVKIT layout or shielding to avoid addition EMI. Slower settings allow for controlling EMI in non-ideal setting (i.e., contained layout, antenna adjacent to device, etc.). This setting is intended to be set once by the initialization code within a system. 0b00 = fastest transition time 0b01 = a little slower than 0b00 0b10 = a little slower than 0b01 0b11 = a little slower than 0b10	SYSRST = 1	R/W
0	x			SYSRST = 1	R/W

9.5.2 CNFG_SBB0_A

Register Name	CNFG_SBB0_A
I²C Slave Address	function of ADDR OTP bit
Register Address	0x29
Reset Value (HEX)	OTP
Reset Value (BIN)	0bxxxxxxxx
Reset Condition	SYSRST = 1
Access Type	R/W
Register Type	Configuration

Bit	Default	Bit Name	Description	Reset	Access Type
7	x	IP_SBB0[1:0]	SIMO Buck-Boost Channel 1 Peak Current Limit 0b00 = 1.000A 0b01 = 0.866A 0b10 = 0.707A 0b11 = 0.500A	SYSRST = 1	R/W
6	x			SYSRST = 1	R/W
5	x	TV_SBB0[5:0]	SIMO Buck-Boost Channel 0 Target Output Voltage The 6-bit adjustment range is from 2.35V to 5.5V in 50mV increments, but the LSB and MSB locations are not standard. See the *TV_SBB0 Code Table* for a complete table of values.	SYSRST = 1	R/W
4	x			SYSRST = 1	R/W
3	x			SYSRST = 1	R/W
2	x			SYSRST = 1	R/W
1	x			SYSRST = 1	R/W
0	x			SYSRST = 1	R/W

9.5.3 TV_SBB0 Code Table

0x00 = 0b000000 = 2.35	0x10 = 0b010000 = 3.15	0x20 = 0b100000 = 3.95	0x30 = 0b110000 = 4.75
0x01 = 0b000001 = 2.40	0x11 = 0b010001 = 3.20	0x21 = 0b100001 = 4.00	0x31 = 0b110001 = 4.80
0x02 = 0b000010 = 2.45	0x12 = 0b010010 = 3.25	0x22 = 0b100010 = 4.05	0x32 = 0b110010 = 4.85
0x03 = 0b000011 = 2.50	0x13 = 0b010011 = 3.30	0x23 = 0b100011 = 4.10	0x33 = 0b110011 = 4.90
0x04 = 0b000100 = 2.55	0x14 = 0b010100 = 3.35	0x24 = 0b100100 = 4.15	0x34 = 0b110100 = 4.95
0x05 = 0b000101 = 2.60	0x15 = 0b010101 = 3.40	0x25 = 0b100101 = 4.20	0x35 = 0b110101 = 5.00
0x06 = 0b000110 = 2.65	0x16 = 0b010110 = 3.45	0x26 = 0b100110 = 4.25	0x36 = 0b110110 = 5.05
0x07 = 0b000111 = 2.70	0x17 = 0b010111 = 3.50	0x27 = 0b100111 = 4.30	0x37 = 0b110111 = 5.10
0x08 = 0b001000 = 2.75	0x18 = 0b011000 = 3.55	0x28 = 0b101000 = 4.35	0x38 = 0b111000 = 5.15
0x09 = 0b001001 = 2.80	0x19 = 0b011001 = 3.60	0x29 = 0b101001 = 4.40	0x39 = 0b111001 = 5.20
0x0A = 0b001010 = 2.85	0x1A = 0b011010 = 3.65	0x2A = 0b101010 = 4.45	0x3A = 0b111010 = 5.25
0x0B = 0b001011 = 2.90	0x1B = 0b011011 = 3.70	0x2B = 0b101011 = 4.50	0x3B = 0b111011 = 5.30
0x0C = 0b001100 = 2.95	0x1C = 0b011100 = 3.75	0x2C = 0b101100 = 4.55	0x3C = 0b111100 = 5.35
0x0D = 0b001101 = 3.00	0x1D = 0b011101 = 3.80	0x2D = 0b101101 = 4.60	0x3D = 0b111101 = 5.40
0x0E = 0b001110 = 3.05	0x1E = 0b011110 = 3.85	0x2E = 0b101110 = 4.65	0x3E = 0b111110 = 5.45
0x0F = 0b001111 = 3.10	0x1F = 0b011111 = 3.90	0x2F = 0b101111 = 4.70	0x3F = 0b111111 = 5.50

9.5.4 CNFG_SBB0_B

Register Name	CNFG_SBB0_B
I²C Slave Address	function of ADDR OTP bit
Register Address	0x2A
Reset Value (HEX)	OTP
Reset Value (BIN)	0b0000xxxx
Reset Condition	SYSRST = 1
Access Type	R/W
Register Type	Configuration

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	RESERVED	Reserved. Unutilized bit. Write to 0. Reads are don't care.	SYSRST = 1	R/W
6	1	EN_FHC	Enables the fixed headroom controller	SYSRST = 1	R/W
5	0	V_HDRM[1:0]	Fixed Headroom Controller Voltage 0b00 = 150mV 0b01 = 175mV 0b10 = 200mV 0b11 = 225mV	SYSRST = 1	R/W
4	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	SYSRST = 1	R/W
3	x	ADE_SBB0	SIMO Buck-Boost Channel 0 Active-Discharge Enable 0 = The active discharge function is disabled. When SBB0 is disabled, it's discharge rate is a function of the output capacitance and the external load. 1 = The active discharge function is enabled. When SBB0 is disabled, an internal resistor (R_{AD_SBB0}) is activated from SBB0 to PGND to help the output voltage discharge. The output voltage discharge rate is a function of the output capacitance, the external loading, and the internal R_{AD_SBB0} load.	SYSRST = 1	R/W
2	x	EN_SBB0[2:0]	Enable Control for SIMO Buck-Boost Channel 0. 0b000 = SBB0 powers-up and powers-down in FPS slot 0 0b001 = SBB0 powers-up and powers-down in FPS slot 1 0b010 = SBB0 powers-up and powers-down in FPS slot 2 0b011 = SBB0 powers-up and powers-down in FPS slot 3 0b100 = SBB0 is off irrespective of FPS 0b101 = same as 0b100 0b110 = SBB0 is on irrespective of FPS whenever the on/off controller is in its "On via Software" or "On via On/Off Controller" states. 0b111 = same as 0b110	SYSRST = 1	R/W
1	x			SYSRST = 1	R/W
0	x			SYSRST = 1	R/W

9.5.5 CNFG_SBB1_A

Register Name	CNFG_SBB1_A
I²C Slave Address	function of ADDR OTP bit
Register Address	0x2B
Reset Value (HEX)	OTP
Reset Value (BIN)	0bxxxxxxxx
Reset Condition	SYSRST = 1
Access Type	R/W
Register Type	Configuration

Bit	Default	Bit Name	Description	Reset	Access Type
7	x	IP_SBB1[1:0]	SIMO Buck-Boost Channel 1 Peak Current Limit 0b00 = 1.000A 0b01 = 0.866A 0b10 = 0.707A 0b11 = 0.500A	SYSRST = 1	R/W
6	x			SYSRST = 1	R/W
5	x	TV_SBB1[5:0]	SIMO Buck-Boost Channel 1 Target Output Voltage This 6-bit configuration is a linear transfer function that starts at 1.4125V to 2.2V in 12.5mV increments. See the *TV_SBB1 Code Table* for a complete table of values.	SYSRST = 1	R/W
4	x			SYSRST = 1	R/W
3	x			SYSRST = 1	R/W
2	x			SYSRST = 1	R/W
1	x			SYSRST = 1	R/W
0	x			SYSRST = 1	R/W

9.5.6 TV_SBB1 Code Table

0x00 = 0b000000 = 1.4125	0x10 = 0b010000 = 1.6125	0x20 = 0b100000 = 1.8125	0x30 = 0b110000 = 2.0125
0x01 = 0b000001 = 1.4250	0x11 = 0b010001 = 1.6250	0x21 = 0b100001 = 1.8250	0x31 = 0b110001 = 2.0250
0x02 = 0b000010 = 1.4375	0x12 = 0b010010 = 1.6375	0x22 = 0b100010 = 1.8375	0x32 = 0b110010 = 2.0375
0x03 = 0b000011 = 1.4500	0x13 = 0b010011 = 1.6500	0x23 = 0b100011 = 1.8500	0x33 = 0b110011 = 2.0500
0x04 = 0b000100 = 1.4625	0x14 = 0b010100 = 1.6625	0x24 = 0b100100 = 1.8625	0x34 = 0b110100 = 2.0625
0x05 = 0b000101 = 1.4750	0x15 = 0b010101 = 1.6750	0x25 = 0b100101 = 1.8750	0x35 = 0b110101 = 2.0750
0x06 = 0b000110 = 1.4875	0x16 = 0b010110 = 1.6875	0x26 = 0b100110 = 1.8875	0x36 = 0b110110 = 2.0875
0x07 = 0b000111 = 1.5000	0x17 = 0b010111 = 1.7000	0x27 = 0b100111 = 1.9000	0x37 = 0b110111 = 2.1000
0x08 = 0b001000 = 1.5125	0x18 = 0b011000 = 1.7125	0x28 = 0b101000 = 1.9125	0x38 = 0b111000 = 2.1125
0x09 = 0b001001 = 1.5250	0x19 = 0b011001 = 1.7250	0x29 = 0b101001 = 1.9250	0x39 = 0b111001 = 2.1250
0x0A = 0b001010 = 1.5375	0x1A = 0b011010 = 1.7375	0x2A = 0b101010 = 1.9375	0x3A = 0b111010 = 2.1375
0x0B = 0b001011 = 1.5500	0x1B = 0b011011 = 1.7500	0x2B = 0b101011 = 1.9500	0x3B = 0b111011 = 2.1500
0x0C = 0b001100 = 1.5625	0x1C = 0b011100 = 1.7625	0x2C = 0b101100 = 1.9625	0x3C = 0b111100 = 2.1625
0x0D = 0b001101 = 1.5750	0x1D = 0b011101 = 1.7750	0x2D = 0b101101 = 1.9750	0x3D = 0b111101 = 2.1750
0x0E = 0b001110 = 1.5875	0x1E = 0b011110 = 1.7875	0x2E = 0b101110 = 1.9875	0x3E = 0b111110 = 2.1875
0x0F = 0b001111 = 1.6000	0x1F = 0b011111 = 1.8000	0x2F = 0b101111 = 2.0000	0x3F = 0b111111 = 2.2000

9.5.7 CNFG_SBB1_B

Register Name	CNFG_SBB1_B
I²C Slave Address	function of ADDR OTP bit
Register Address	0x2C
Reset Value (HEX)	OTP
Reset Value (BIN)	0b0000xxxx
Reset Condition	SYSRST = 1
Access Type	R/W
Register Type	Configuration

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	SYSRST = 1	R/W
6	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	SYSRST = 1	R/W
5	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	SYSRST = 1	R/W
4	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	SYSRST = 1	R/W
3	x	ADE_SBB1	SIMO Buck-Boost Channel 1 Active-Discharge Enable 0 = The active discharge function is disabled. When SBB1 is disabled, it's discharge rate is a function of the output capacitance and the external load. 1 = The active discharge function is enabled. When SBB1 is disabled, an internal resistor (R_{AD_SBB1}) is activated from SBB1 to PGND to help the output voltage discharge. The output voltage discharge rate is a function of the output capacitance, the external loading, and the internal R_{AD_SBB1} load.	SYSRST = 1	R/W
2	x	EN_SBB1[2:0]	Enable Control for SIMO Buck-Boost Channel 1. 0b000 = SBB1 powers up and powers down in FPS slot 0 0b001 = SBB1 powers up and powers down in FPS slot 1 0b010 = SBB1 powers up and powers down in FPS slot 2 0b011 = SBB1 powers up and powers down in FPS slot 3 0b100 = SBB1 is off irrespective of FPS 0b101 = same as 0b100 0b110 = SBB1 is on irrespective of FPS whenever the on/off controller is in its "On via Software" or "On via On/Off Controller" states. 0b111 = same as 0b110 Prior to enabling the SIMO, program the bias circuits to normal power mode (SBIA_LPM = 0). After the SIMO is enabled, the bias circuits can be programmed back to low power mode (SBIA_LPM = 1) to decrease quiescent current.	SYSRST = 1	R/W
1	x			SYSRST = 1	R/W
0	x			SYSRST = 1	R/W

9.5.8 CNFG_SBB2_A

Register Name	CNFG_SBB2_A
I²C Slave Address	function of ADDR OTP bit
Register Address	0x2D
Reset Value (HEX)	OTP
Reset Value (BIN)	0bxxxxxxxx
Reset Condition	SYSRST = 1
Access Type	R/W
Register Type	Configuration

Bit	Default	Bit Name	Description	Reset	Access Type
7	x	IP_SBB2[1:0]	SIMO Buck-Boost Channel 1 Peak Current Limit 0b00 = 1.000A 0b01 = 0.866A 0b10 = 0.707A 0b11 = 0.500A	SYSRST = 1	R/W
6	x			SYSRST = 1	R/W
5	x	TV_SBB2[5:0]	SIMO Buck-Boost Channel 2 Target Output Voltage This 6-bit configuration is a linear transfer function that starts at 0.85V, ends at 4V, with 50mV increments. See the *TV_SBB2 Code Table* for a complete table of values.	SYSRST = 1	R/W
4	x			SYSRST = 1	R/W
3	x			SYSRST = 1	R/W
2	x			SYSRST = 1	R/W
1	x			SYSRST = 1	R/W
0	x			SYSRST = 1	R/W

9.5.9 TV_SBB2 Code Table

0x00 = 0b000000 = 0.85	0x10 = 0b010000 = 1.65	0x20 = 0b100000 = 2.45	0x30 = 0b110000 = 3.25
0x01 = 0b000001 = 0.90	0x11 = 0b010001 = 1.70	0x21 = 0b100001 = 2.50	0x31 = 0b110001 = 3.30
0x02 = 0b000010 = 0.95	0x12 = 0b010010 = 1.75	0x22 = 0b100010 = 2.55	0x32 = 0b110010 = 3.35
0x03 = 0b000011 = 1.00	0x13 = 0b010011 = 1.80	0x23 = 0b100011 = 2.60	0x33 = 0b110011 = 3.40
0x04 = 0b000100 = 1.05	0x14 = 0b010100 = 1.85	0x24 = 0b100100 = 2.65	0x34 = 0b110100 = 3.45
0x05 = 0b000101 = 1.10	0x15 = 0b010101 = 1.90	0x25 = 0b100101 = 2.70	0x35 = 0b110101 = 3.50
0x06 = 0b000110 = 1.15	0x16 = 0b010110 = 1.95	0x26 = 0b100110 = 2.75	0x36 = 0b110110 = 3.55
0x07 = 0b000111 = 1.20	0x17 = 0b010111 = 2.00	0x27 = 0b100111 = 2.80	0x37 = 0b110111 = 3.60
0x08 = 0b001000 = 1.25	0x18 = 0b011000 = 2.05	0x28 = 0b101000 = 2.85	0x38 = 0b111000 = 3.65
0x09 = 0b001001 = 1.30	0x19 = 0b011001 = 2.10	0x29 = 0b101001 = 2.90	0x39 = 0b111001 = 3.70
0x0A = 0b001010 = 1.35	0x1A = 0b011010 = 2.15	0x2A = 0b101010 = 2.95	0x3A = 0b111010 = 3.75
0x0B = 0b001011 = 1.40	0x1B = 0b011011 = 2.20	0x2B = 0b101011 = 3.00	0x3B = 0b111011 = 3.80
0x0C = 0b001100 = 1.45	0x1C = 0b011100 = 2.25	0x2C = 0b101100 = 3.05	0x3C = 0b111100 = 3.85
0x0D = 0b001101 = 1.50	0x1D = 0b011101 = 2.30	0x2D = 0b101101 = 3.10	0x3D = 0b111101 = 3.90
0x0E = 0b001110 = 1.55	0x1E = 0b011110 = 2.35	0x2E = 0b101110 = 3.15	0x3E = 0b111110 = 3.95
0x0F = 0b001111 = 1.60	0x1F = 0b011111 = 2.40	0x2F = 0b101111 = 3.20	0x3F = 0b111111 = 4.00

9.5.10 CNFG_SBB2_B

Register Name	CNFG_SBB2_B
I²C Slave Address	function of ADDR OTP bit
Register Address	0x2E
Reset Value (HEX)	OTP
Reset Value (BIN)	0b0000xxxx
Reset Condition	SYSRST = 1
Access Type	R/W
Register Type	Configuration

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	SYSRST = 1	R/W
6	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	SYSRST = 1	R/W
5	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	SYSRST = 1	R/W
4	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	SYSRST = 1	R/W
3	x	ADE_SBB2	SIMO Buck-Boost Channel 2 Active-Discharge Enable 0 = The active discharge function is disabled. When SBB2 is disabled, it's discharge rate is a function of the output capacitance and the external load. 1 = The active discharge function is enabled. When SBB2 is disabled, an internal resistor (R_{AD_SBB2}) is activated from SBB2 to PGND to help the output voltage discharge. The output voltage discharge rate is a function of the output capacitance, the external loading, and the internal R_{AD_SBB2} load.	SYSRST = 1	R/W
2	x	EN_SBB2[2:0]	Enable Control for SIMO Buck-Boost Channel 2. 0b000 = SBB2 powers-up and powers-down in FPS slot 0 0b001 = SBB2 powers-up and powers-down in FPS slot 1 0b010 = SBB2 powers-up and powers-down in FPS slot 2 0b011 = SBB2 powers-up and powers-down in FPS slot 3 0b100 = SBB2 is off irrespective of FPS 0b101 = same as 0b100 0b110 = SBB2 is on irrespective of FPS whenever the on/off controller is in its "On via Software" or "On via On/Off Controller" states. 0b111 = same as 0b110 Prior to enabling the SIMO, program the bias circuits to normal power mode (SBIA_LPM = 0). After the SIMO is enabled, the bias circuits can be programmed back to low power mode (SBIA_LPM = 1) to decrease quiescent current.	SYSRST = 1	R/W
1	x			SYSRST = 1	R/W
0	x			SYSRST = 1	R/W

9.6 Register Descriptions: Current Sink

9.6.1 CNFG_CS

Register Name	CNFG_CS
I²C Slave Address	0x48
Register Address	0x40
Reset Value (HEX)	0x14
Reset Value (BIN)	0b00010100
Reset Condition	SYSRST = 1
Access Type	R/W
Register Type	Configuration

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	RESERVED	Reserved. Unutilized bit. Write to 0. Reads are don't care.	SYSRST = 1	R/W
6	0	RESERVED	Reserved. Unutilized bit. Write to 0. Reads are don't care.	SYSRST = 1	R/W
5	0	RESERVED	Reserved. Unutilized bit. Write to 0. Reads are don't care.	SYSRST = 1	R/W
4	1	CS_WD	Current Sink Watchdog Control Bit 0 = Send watchdog interrupt to top level, but do not shut down the current sink if the watchdog timer expires 1 = Send watchdog interrupt to top level, and shut down current sink if watchdog timer expires	SYSRST = 1	R/W
3	0	CS_PRE_EN	Current Sink Pre-Enable Bit 0 = The current sink bias circuitry is disabled. CS_EN pin is ignored. 1 = The current sink bias circuit is enabled. CS_EN pin is used to control the current sink.	SYSRST = 1	R/W
2	1	CS_CURR[2:0]	CS Current Control, Programmable with 3-Bit Resolution	SYSRST = 1	R/W
1	0			SYSRST = 1	R/W
0	0			SYSRST = 1	R/W

10 Revision History

REV NUMBER	REV DATE	DESCRIPTION	PAGES CHANGED
0	9/17	Initial release	—