Gleanergy Multi-Source Energy Harvesting Demo Board with Battery Chargers and Life-Extenders for Use with DC2321A Dust Demo Board – No Transducers

DESCRIPTION

The DC2509A development platform is a versatile energy harvesting demo board that is capable of accepting solar, thermal, and piezoelectric energy sources or any high impedance AC or DC source. The board contains four independent power circuits consisting of the following EH ICs:

- LTC®3106 – 300 mA, Low Voltage Buck-Boost Converter with PowerPath™ and 1.5µA Quiescent Current
- LTC3107 – Ultralow Voltage Energy Harvester and Primary Battery Life Extender
- LTC3330 – Nanopower Buck-Boost DC/DC with Energy Harvesting Battery Life Extender
- LTC3331 – Nanopower Buck-Boost DC/DC with Energy Harvesting Battery Charger
- LTC2935-2 – Ultralow Power Supervisor with Power-Fail Output Selectable Thresholds

The board is designed to connect to the DC2321A, a Dust mote wireless sensor node demo board which monitors the batteries and the status signals of each IC.

Each energy harvesting circuit on DC2509A hosts input turrets for connecting solar panels, thermoelectric generators, piezoelectric devices, or any other high impedance source.

As a backup power supply, the board holds a primary battery and a secondary battery which can be easily routed to any of the applicable ICs.

The board hosts groups of switches, jumpers, and resistors which allow its operation be configured in various ways. As a result, the system is very customizable and can be modified to meet the user's needs. This compatibility makes it a perfect evaluation tool for any low power energy harvesting system.

Please refer to the individual IC data sheets for the operation of each power management circuit. The application section of this demo manual describes the system level functionality of this board and the various ways it can be used in early design prototyping.

Design files for this circuit board are available at http://www.linear.com/demo/DC2509A

BOARD PHOTO

Figure 1. DC2509A

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BOARD LAYOUT ORGANIZATION DIAGRAM

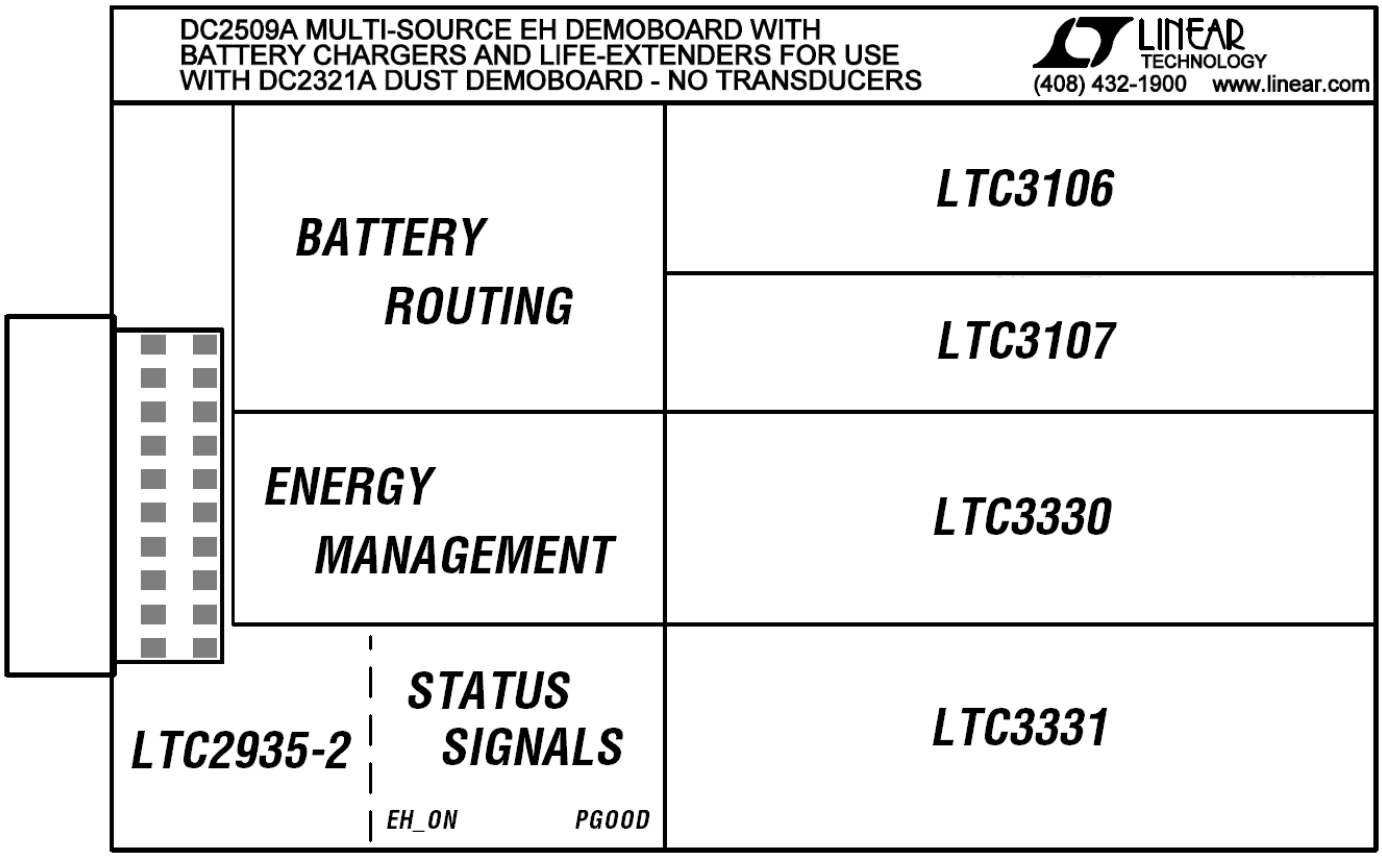

Figure 2. Board Layout Organization Diagram

SPECIFICATIONS

TYPE	PART	PARAMETER	CONDITIONS	MIN	TYPICAL/DEFAULT	MAX	UNITS	NOTES
IC	LTC3106	V_{IN}	Backup Power Source Available	0.33		6	V	
			Backup Power Source Unavailable	0.85				
		V_{OUT}		1.8	3.3	5	V	Set Using R6-R9, See Table 10
		V_{STORE}		2.07	4	4	V	Set Using R10-R13, See Table 11
	LTC3107	V_{IN}		30		500	mV	Input to Transformer
		V_{OUT}		V_{BAT} – 0.23		V_{BAT} – 0.03	V	Min = Battery Powering Load Max = EH Powering Load
	LTC3330	V_{AC1}&V_{AC2}		4		19	V	
		I_{AC1}&I_{AC2}		–50		50	mA	
		V_{OUT}		1.8	3.3	5	V	Set Using R20-R25, See Table 14
		UVLO	Rising Falling	4 3	7 6	18 17	V	Set Using R38-R45, See Table 16
		LDO_OUT		1.2	3.3	3.3	V	Set Using R26-R31, See Table 12
	LTC3331	V_{AC1}&V_{AC2}		4		19	V	
		I_{AC1}&I_{AC2}		–50		50	mA	
		V_{OUT}		1.8	3.3	5	V	Set Using R46-R51, See Table 14
		UVLO	Default Rising Default Falling	4 3	7 6	18 17	V	
		V_{FLOAT}		3.45	4.0	4.2	V	Set Using R52-R57, See Table 13
		V_{LBD}		2.04	2.70	3.20	V	See LTC3331 Data Sheet for More Information About These Levels
		$V_{LBC\_BAT\_IN}$		2.35	3.03	3.53	V	
		$V_{LBC\_BAT\_OUT}$		3.02	3.70	4.20	V	
Battery	Primary	Voltage	(Note 1)	3.08	3	3.8	V	Replace Battery Below Min Level or Modify Circuit Configuration
	Secondary	Voltage	(Note 2)	3.03	3.6	4.2	V	
Storage	Ceramic Capacitors	Energy Capacity	EHVCC = 3.3V		2.3		mJ	Between 3.3V and the Default 2.25V LTC2935-2 Falling Threshold
	Supercap	Energy Capacity			37.9		mJ	

The "Typical/Default" column shows data corresponding to the factory configuration of the board where all 0Ω resistors are in their default positions. The min/max columns show the minimum or maximum allowable levels.

Note 1: Because the output voltage of the LTC3107 is dependent on the battery voltage, $V_{OUT\_LTC3107}$ will be too low to reach the default 2.85V ground-switching threshold if the primary battery is below 3.08V. Refer to the LTC2935-2 Power Switch Circuit section to modify this threshold, or replace the battery.

Note 2: If the secondary battery voltage is below the default 3.03V BAT_IN connect threshold of the LTC3331, it cannot be connected internally to the IC to be used as a backup source. The battery can still be charged in this state if EH power is available. Alternatively, the connect threshold ($V_{LBC\_BAT\_IN}$) can be changed according to Table 13 or the battery can be replaced.

ASSEMBLY DRAWING

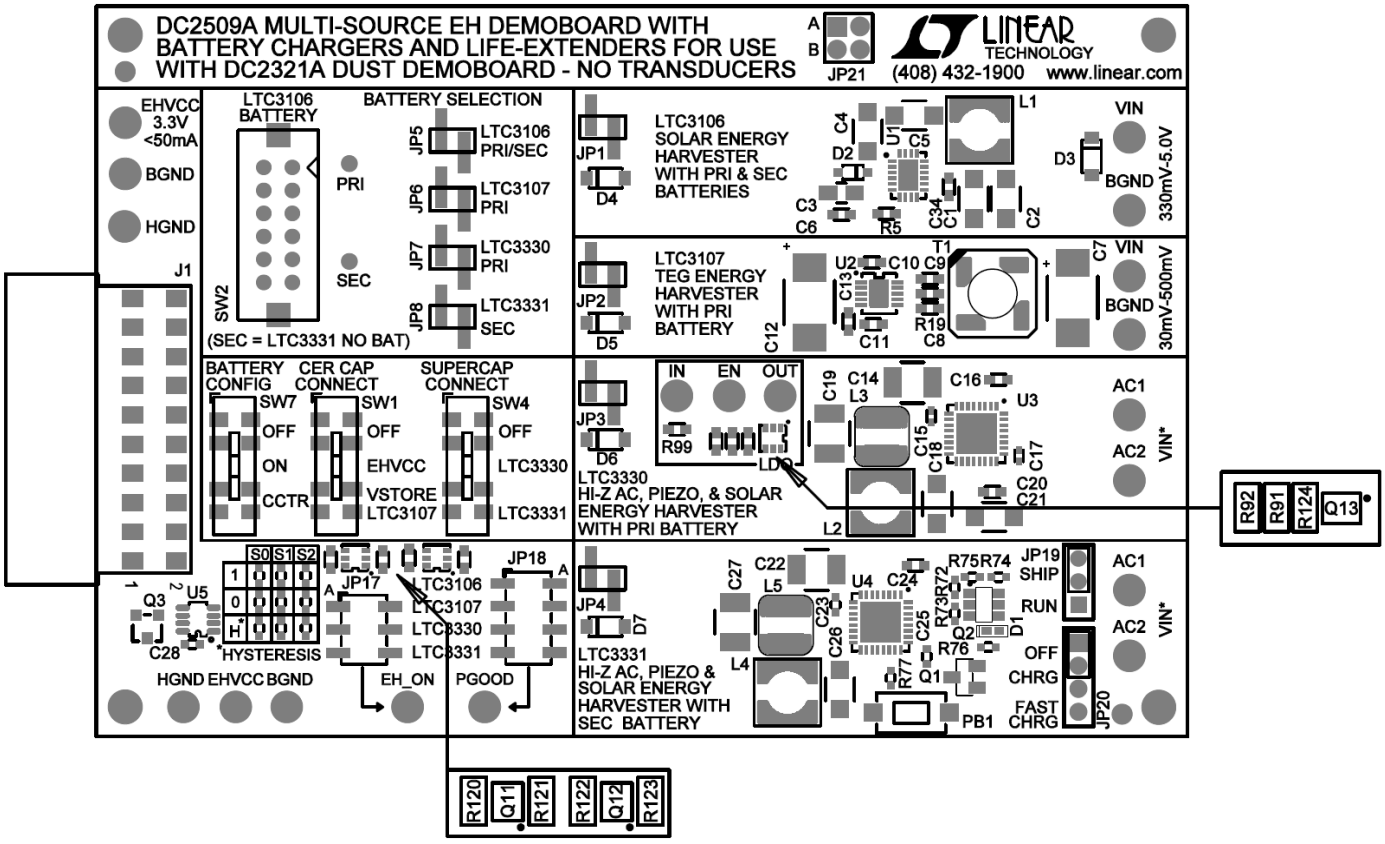

Figure 3. DC2509A Top Assembly Drawing

ASSEMBLY DRAWING

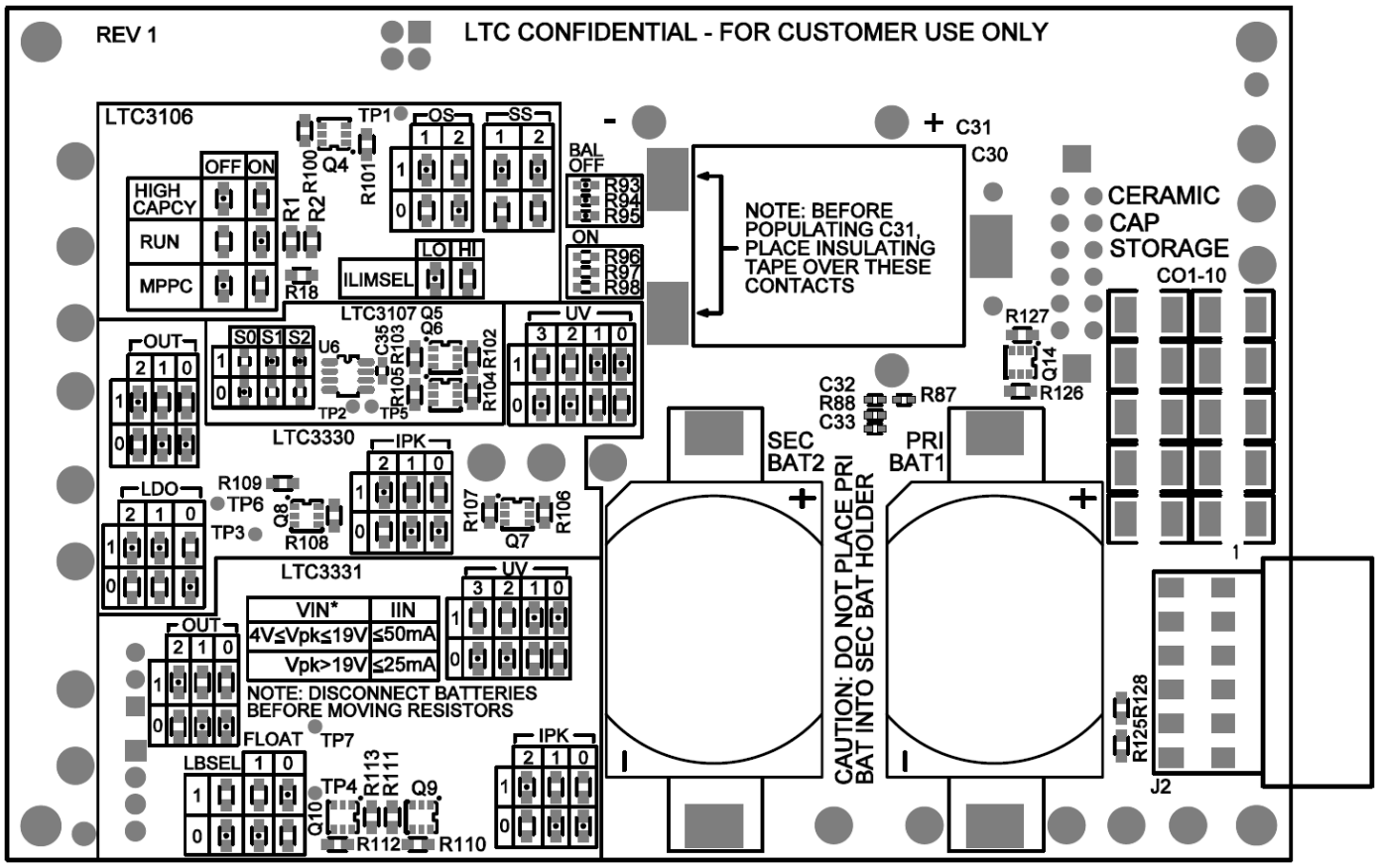

Figure 4. DC2509A Bottom Assembly Drawing

QUICK START PROCEDURE

Reference designators for jumpers and default positions for 0Ω resistors are listed on the assembly drawing. Reference designators for 0Ω resistors are listed in Figure 20.

1) All 0Ω resistors should be in their default position (see Figure 4, default resistors have dots). Verify that the jumpers and switches are also in their default setting as follows:

Table 1. Default Jumper/Switch Configuration

TYPE	REFERENCE DESIGNATOR	POSITION
JUMPER	JP1 – JP4	Shunt on JP3
	JP5 – JP8	(Not Installed)
	JP17	Shunt on JP17B
	JP18	Shunt on JP18C
	JP19	SHIP
	JP20	OFF
SWITCH	SW1	EHVCC
	SW2	PRI
	SW4	OFF
	SW7	OFF

2) This configuration ensures that the output of the LTC3330 is routed to EHVCC. As shown in Figure 5, connect VM1 to measure the EHVCC output voltage and connect PS1 and R1 to simulate a solar power source.

3) Output power from PS1 and observe that the voltage on VM1 is rising to, or regulated at, 3.3V.

4) Connect VM2 and LOAD1 as shown in Figure 5. Put PS1 into standby mode and observe the voltage on VM1 and VM2 begin to drop. As the voltage on VM1 drops past 2.25V, observe as the voltage on VM2 quickly falls to 0V.

5) Output power from PS1 and observe the voltage on VM2 quickly rise to the voltage on VM1 as VM1 rises past 2.85V.

6) Put PS1 into standby mode, then set SW7 = "ON" and install JP7 to connect the primary battery to the LTC3330. Observe as the voltage on both voltmeters quickly rises to 3.3V and regulates.

7) Output power from PS1 and observe that there is no change in output voltage as the IC switches from using battery power to using power from PS1 through its energy harvesting input.

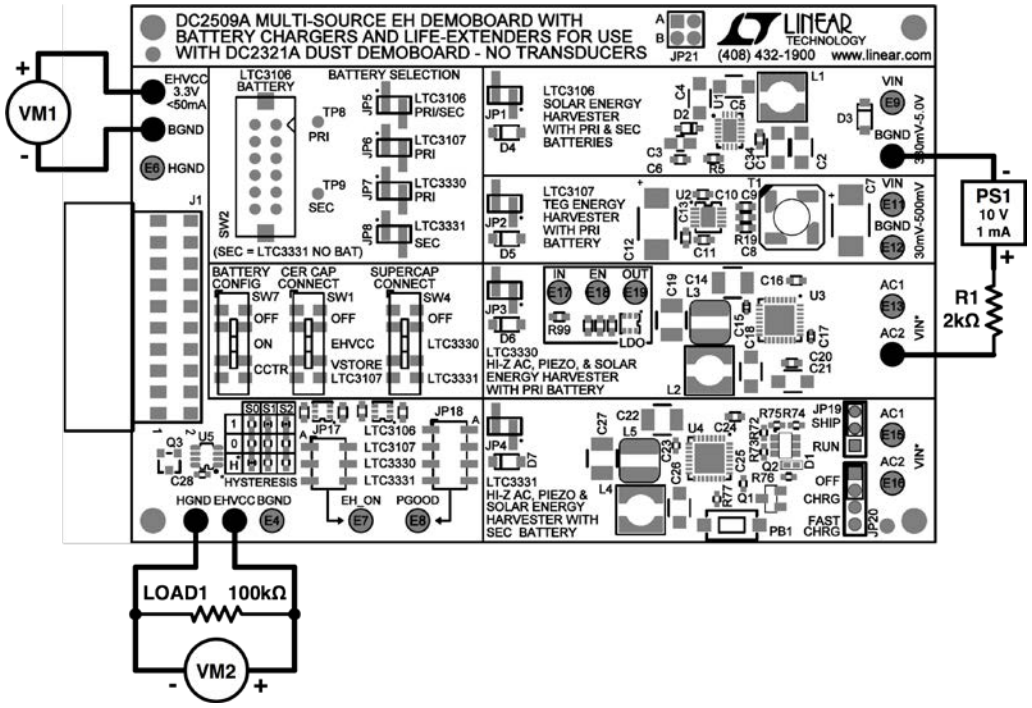

Figure 5. Setup for DC2509A Test Procedure with LTC3330

QUICK START PROCEDURE

8) Reconfigure the board according to Figure 6:
   a) Move the shunt from JP3 to JP2 in order to route the LTC3107's output to the load. Move the shunt from JP7 to JP6 in order to power the LTC3107 from the primary battery.
   b) Move the positive lead of VM2 to the shunt on JP6 in order to measure the voltage of the primary battery. Move the negative lead to BGND.
   c) Connect PS2 and R2 to the input of the LTC3107 to simulate a TEG power source.
9) Observe the voltage on VM1 and VM2. The voltage on VM1 should be approximately 230mV below the voltage of VM2.
10) Output power from PS2. Observe the voltage on VM1 rise to 30mV below the voltage on VM2 as the LTC3107 powers the load through its energy harvesting input.
11) Put PS2 into standby mode and observe the voltage on VM1 fall to approximately 230mV below the voltage of VM2 as the LTC3107 powers the load from its backup battery.

Optional Continuation with Any Transducer

The source routing flowcharts (Figure 9 to Figure 11) show how to configure the board for use with any energy harvesting transducer. A user can follow these routing guides to evaluate ICs with any transducer connected to the energy harvesting input turrets on the right side of the board.

Note: IC configurations such as the UVLO windows of the LTC3330 and LTC3331 may need to be changed for use with custom transducers. Refer to Tables 8-15.

1) Reconfigure the board according to Figure 5, but do not connect PS1 or R1.
2) Decide which transducer type to use and find the appropriate flowchart. Start at the left of the flowchart and choose settings until a box in the "Configure Demo Board" section is reached.
3) Configure all jumpers and switches listed in the appropriate box. Any jumpers or switches that are not listed in the box are irrelevant for the chosen configuration.
4) Power the energy harvesting transducer and observe the voltage on VM1 and VM2 which should be near 3.3V by default (less for LTC3107).

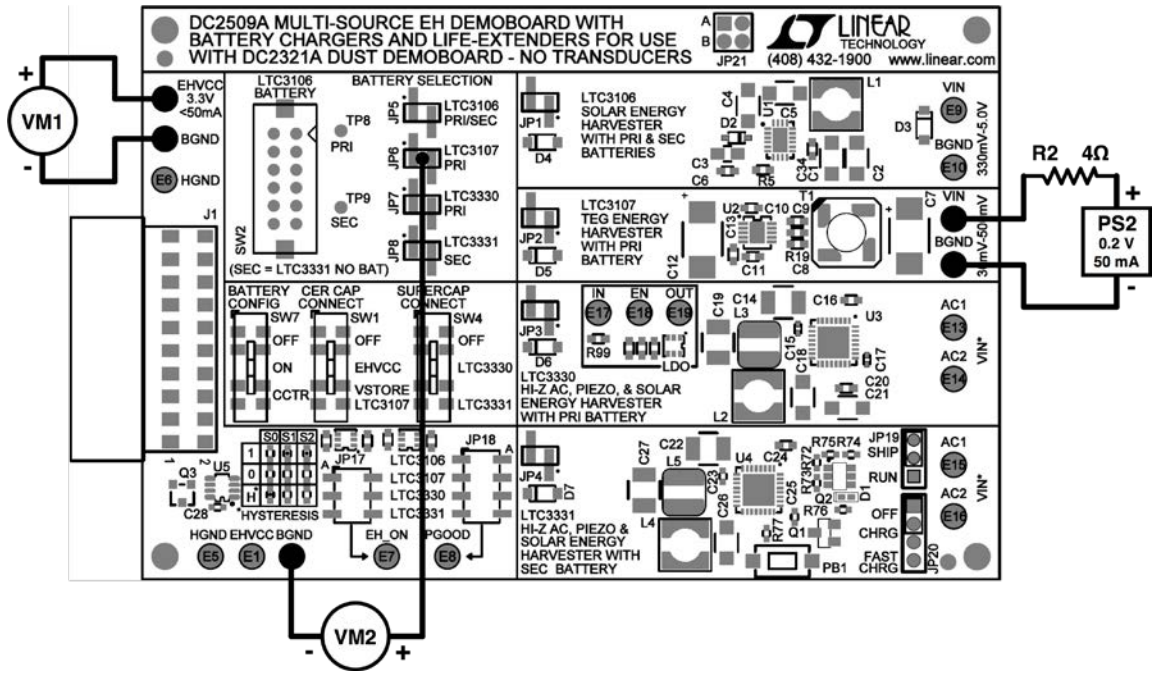

Figure 6. Setup for DC2509A Test Procedure with LTC3107

OPERATION OVERVIEW

The function of the DC2509A is to provide a low-power wireless application, such as a wireless sensor node, with an uninterrupted power supply which uses as much harvested energy as is available to extend the life of a primary or secondary battery.

The energy harvesting input turrets allow harvested energy to be routed to the input of each IC, and the batteries serve as a backup supply which can be charged or unused if energy from the transducers is sufficient to power the load.

The four energy-harvesting ICs switch between these sources, using all available harvested energy and as much backup energy as is needed to keep a regulated output.

A supercapacitor and a bank of ceramic capacitors are able to be connected to the board's output in order to store energy, smooth the output, and provide large pulses of current to the load. This helps to ensure that power remains uninterrupted for pulsed loads such as data transmission events on a wireless sensor node.

An LTC2935-2 low-power manager IC monitors the output voltage and switches the ground on the header (HGND) so that it is connected to the ground reference for the rest of the DC2509A (BGND). This completes the circuit and ensures that the load receives a quickly-rising power supply and also that energy storage is able to gather sufficient energy for the required application before the load begins taking power.

For use with the DC2321A demo application, DC2509A additionally passes buffered IC status signals through the output header. Both batteries can also be routed through coulomb counters on DC2321A and back to DC2509A to power the ICs; this allows the voltage, current, and charge of the batteries to be monitored.

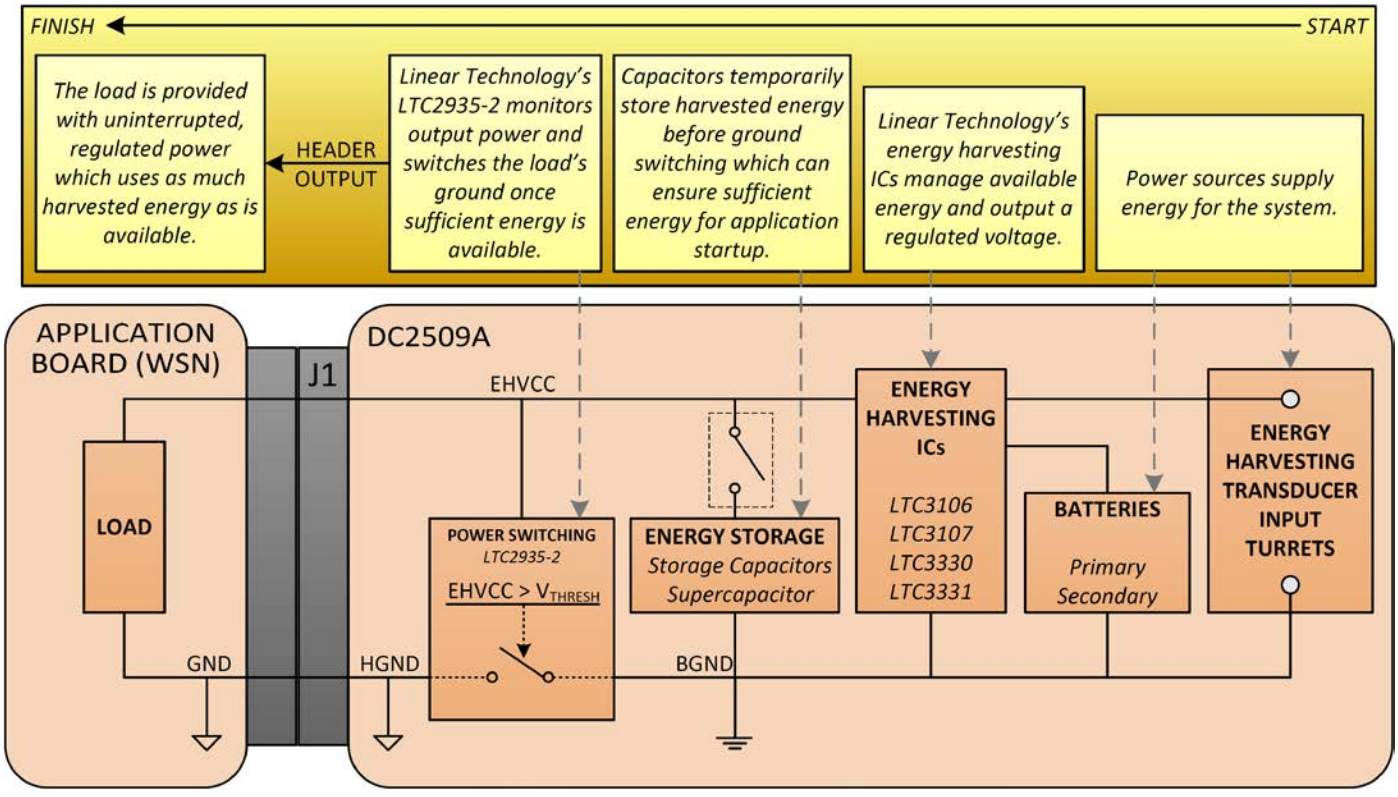

Figure 7. DC2509A Simplified Block Diagram

BLOCK DIAGRAMS

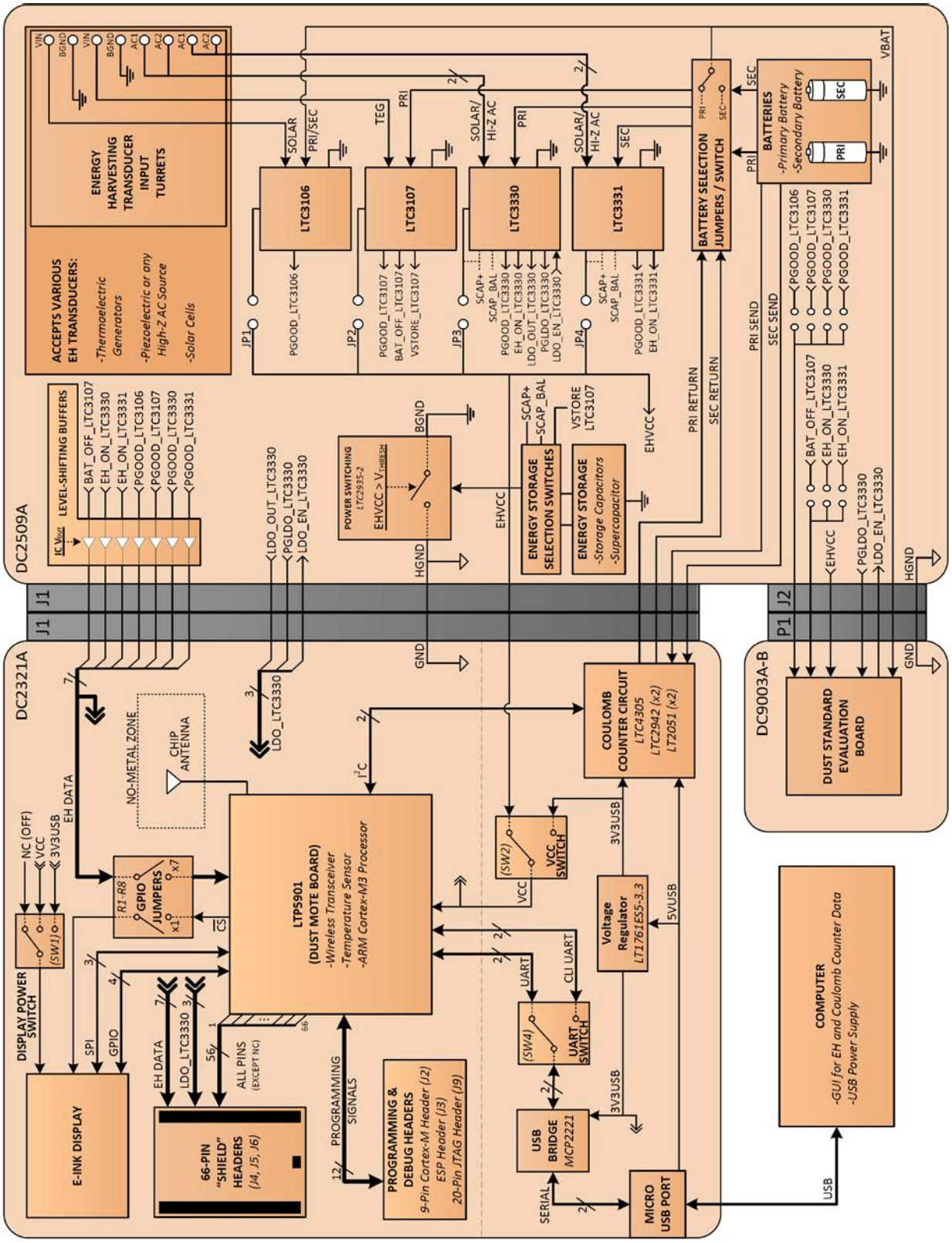

Figure 8. DC2509A Block Diagram

SOURCE ROUTING FLOWCHARTS

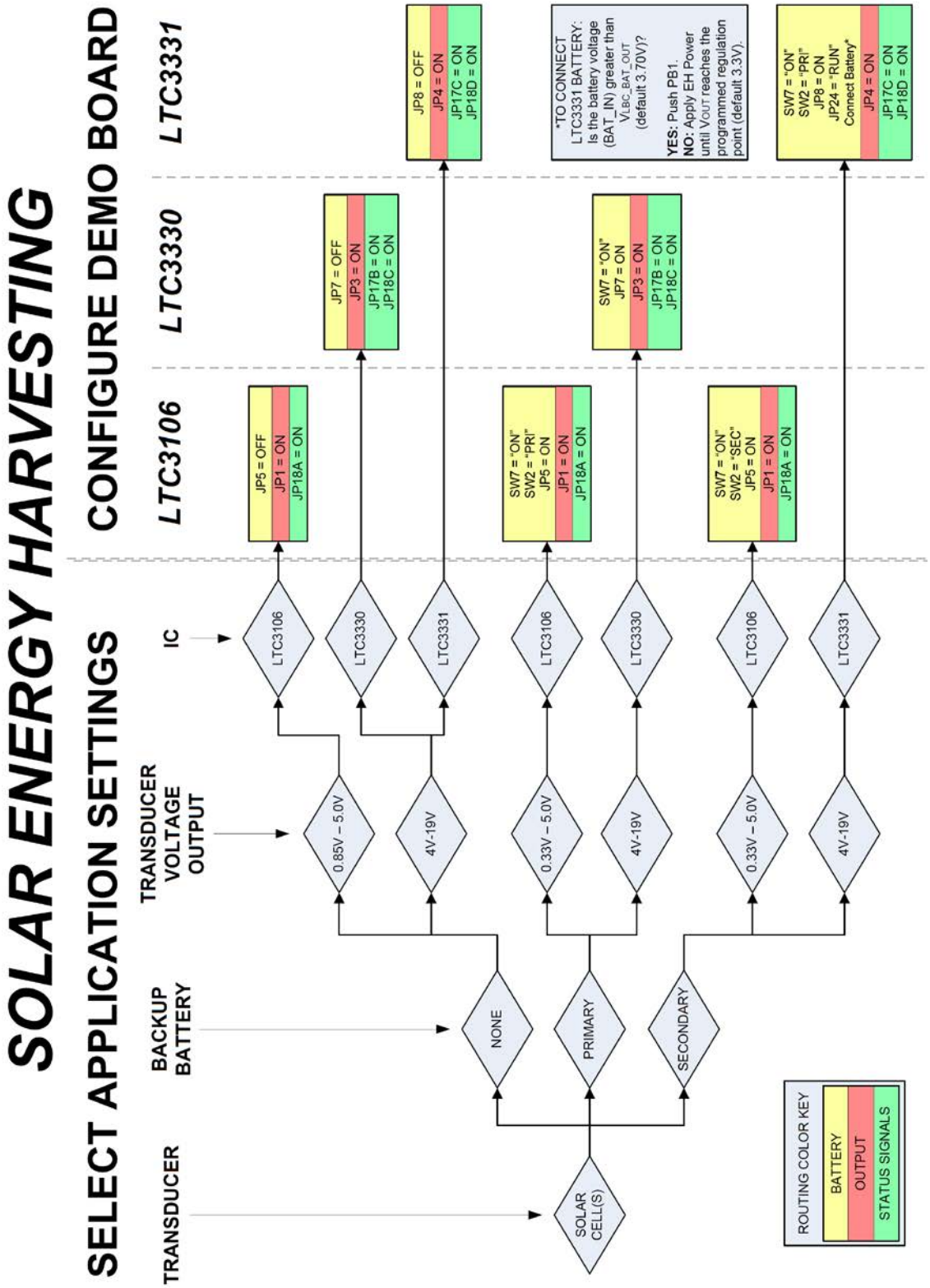

Figure 9. Solar Energy Harvesting Selection and Routing Flowchart

SOURCE ROUTING FLOWCHARTS

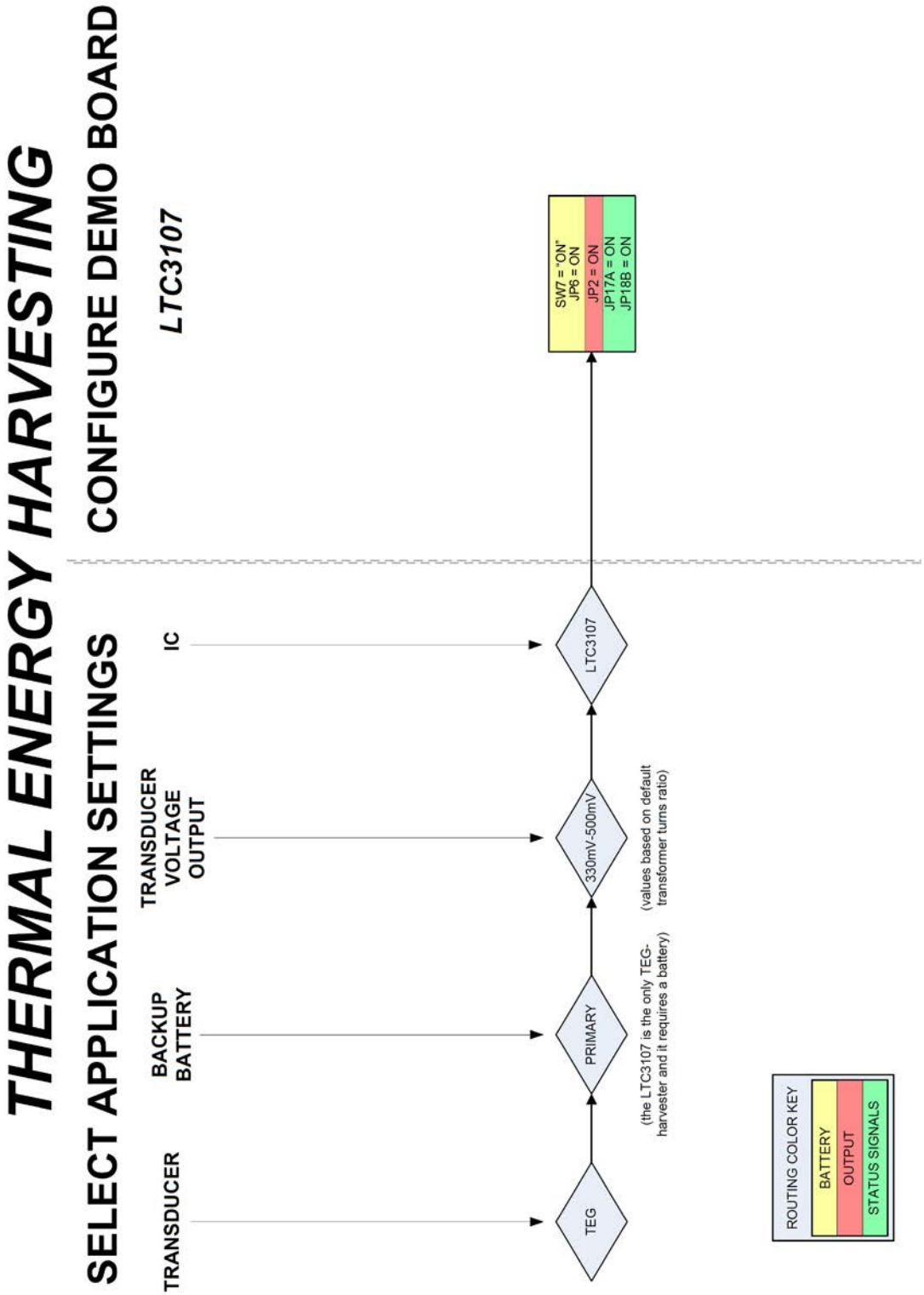

Figure 10. Thermal Energy Harvesting Selection and Routing Flowchart

SOURCE ROUTING FLOWCHARTS

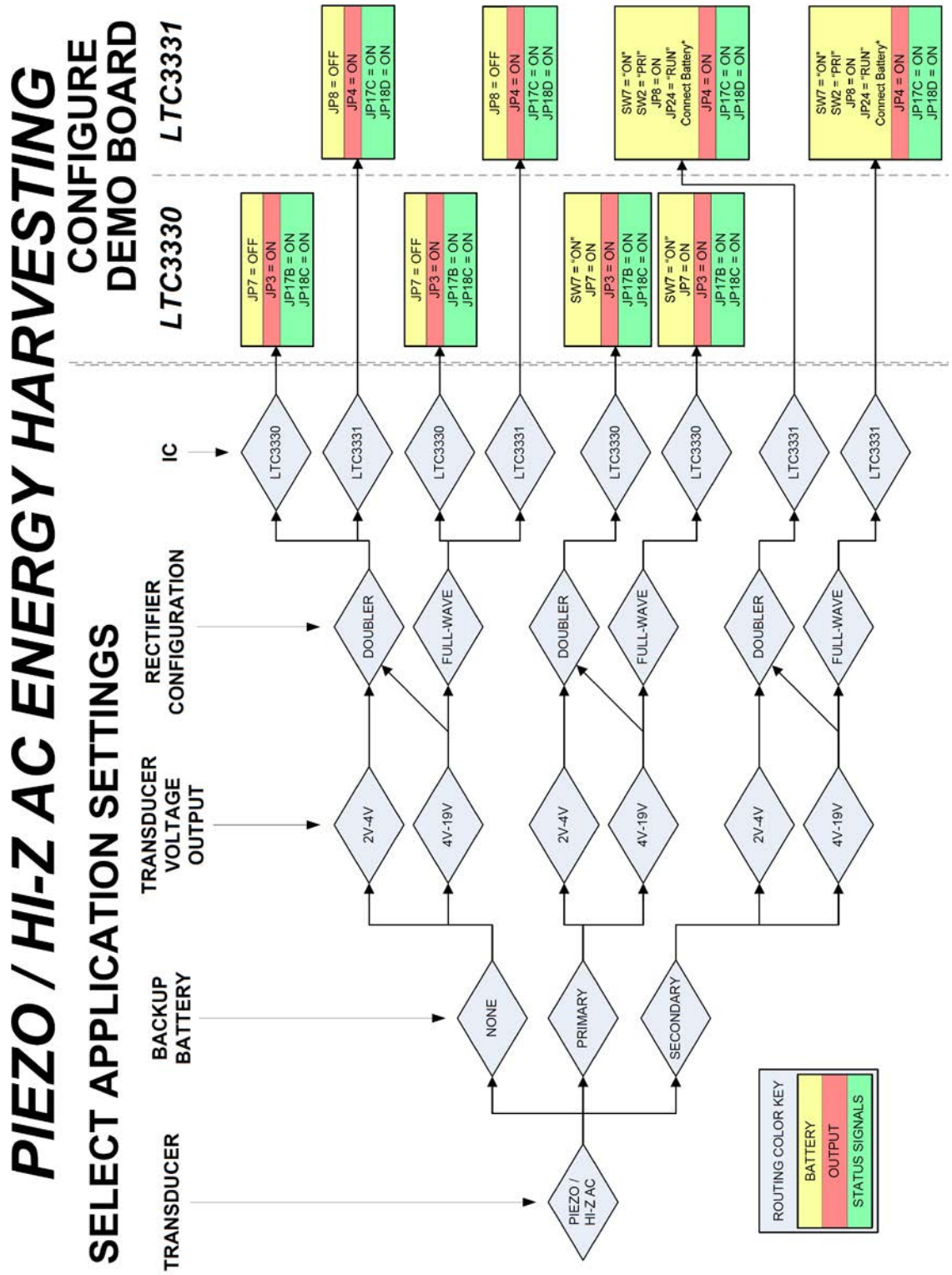

Figure 11. Piezoelectric/High-Impedance AC Energy Harvesting Selection and Routing Flowchart

BATTERY ROUTING GUIDE

Table 2 shows how to route any given power source to all applicable ICs. Applying the correct configuration for each case will ensure that the output of the source is routed to the input of the IC but, in order to route the output of the IC to the board output (EHVCC), a shunt must still be installed on the appropriate output-selection jumper (JP1-JP4). In order to monitor the status outputs of the IC using the EH_ON and PGOOD turrets, the shunts on JP17 and JP18 must also be installed accordingly.

Table 2. Battery Routing Guide

BATTERY	DESTINATION	CONFIGURATION	NOTES
Primary Battery	LTC3106	SW7 = “ON” SW2 = “PRI” JP5 = ON	The primary battery can power multiple ICs simultaneously.
	LTC3107	SW7 = “ON” JP6 = ON	
	LTC3330	SW7 = “ON” JP7 = ON	
Secondary Battery	LTC3106	SW7 = “ON” SW2 = “SEC” JP5 = ON	The secondary battery can only power one IC at a time. Using SW2, it can be connected to either the LTC3106 or the LTC3331. *To connect using PB1 or EH, the battery voltage must be above the PB1 or EH threshold, respectively (listed in Table 12). The default thresholds are 3.7V for PB1 and 3.03V for EH.
	LTC3331	SW7 = “ON” SW2 = “PRI” JP8 = ON JP19 = “RUN” Push PB1 or Apply EH*	

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Jumper Functions

JP1: Power selection jumper used to route the LTC3106 output to the load.

JP2: Power selection jumper used to route the LTC3107 output to the load.

JP3: Power selection jumper used to route the LTC3330 output to the load.

JP4: Power selection jumper used to route the LTC3331 output to the load.

JP5: Battery selection jumper used to route the selected battery to VSTORE on the LTC3106. The LTC3106 is compatible with both primary and secondary batteries. SW2 is used to choose which battery is active. If the secondary battery is chosen to power the LTC3106, the LTC3331 cannot be powered by any battery. However, if the primary battery is chosen to power the LTC3106, the LTC3331 can be powered by the secondary battery.

JP6: Battery selection jumper used to route the primary battery to VBAT on the LTC3107.

JP7: Battery selection jumper used to route the primary battery to BAT on the LTC3330.

JP8: Battery selection jumper used to route the secondary battery to BAT_IN on the LTC3331. Note that if SW2 is set to connect the secondary battery to the LTC3106, the secondary battery cannot be connected to the LTC3331.

JP17A: Routes the LTC3107 BAT_OFF signal to the EH_ON turret and the Dust Header EH_ON output.

JP17B: Routes the LTC3330 EH_ON signal to the EH_ON turret and the Dust Header EH_ON output.

JP17C: Routes the LTC3331 EH_ON signal to the EH_ON turret and the Dust Header EH_ON output.

JP18A: Routes the LTC3106 PGOOD signal to the PGOOD turret and the dust header.

JP18B: Routes the LTC2935-2 PGOOD signal to the PGOOD turret and the dust header. The LTC3017 does not inherently generate its own PGOOD signal, so an LTC2935-2 monitors its output to create a PGOOD signal.

JP18C: Routes the LTC3330 PGOOD signal to the PGOOD turret and the dust header.

JP18D: Routes the LTC3331 PGOOD signal to the PGOOD turret and the dust header.

JP19: Selects the battery storage mode for the secondary battery connected to the LTC3331. In SHIP mode, the battery disconnect switch is forced off to ensure there is no drain on the battery. For operation with the secondary battery, RUN mode must be enabled.

JP20: Selects the charging mode for the secondary battery connected to the LTC3331. The charger can be set to OFF (battery life-extension only), CHRG for a slow charge, or FAST CHRG for a faster charge using the LTC3331's external charging circuitry.

JP21A-JP21B: Storage for unused jumpers.

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Table 3. Jumper Functions

GROUP		INDIVIDUAL		
REFERENCE	**FUNCTION**	**REFERENCE**	**FUNCTION**	**CONDITIONS/NOTES**
JP1-JP4	Route IC output to board output (EHVCC) and header	JP1	Send V_{OUT} from LTC3106 to output and header.	–
		JP2	Send V_{OUT} from LTC3107 to output and header.	
		JP3	Send V_{OUT} from LTC3330 to output and header.	
		JP4	Send V_{OUT} from LTC3331 to output and header.	
JP5-JP8	Connect ICs to their respective batteries	JP5	Power LTC3106 from currently selected battery.	SW2 selects battery
		JP6	Power LTC3107 from primary battery.	–
		JP7	Power LTC3330 from primary battery.	
		JP8	Power LTC3331 from secondary battery.	SW2 must be set to PRI
JP17	Route EH_ON signal to turret and dust header	JP17A	Connect LTC3107 BAT_OFF signal to EH_ON turret and dust header.	–
		JP17B	Connect LTC3330 EH_ON signal to EH_ON turret and dust header.	
		JP17C	Connect LTC3331 EH_ON signal to EH_ON turret and dust header.	
JP18	Route PGOOD signal to turret and dust header	JP18A	Connect LTC3106 PGOOD signal to PGOOD turret and dust header.	–
		JP18B	Connect LTC2935-2 PGOOD signal to PGOOD turret and dust header.	
		JP18C	Connect LTC3330 PGOOD signal to PGOOD turret and dust header.	
		JP18D	Connect LTC3331 PGOOD signal to PGOOD turret and dust header.	–
JP19-JP20	LTC3331 operation	JP19	Toggle ship mode to avoid draining battery when not in use.	
		JP20	Enable charging or fast charging of the secondary battery.	

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Switch Functions

SW1: Connects the ten Optional Energy Storage ceramic capacitors directly to EHVCC or VSTORE on the LTC3107. These capacitors can provide short-term power to the system in the event the load has intermittent energy requirements. These capacitors can also be disconnected entirely.

SW2: Selects between the primary and secondary batteries for the LTC3106 and connects the same battery to VBAT on the dust header (J2). Due to charging capabilities, only one IC can use the secondary battery at any time. Therefore, while the LTC3106 is connected to the secondary battery, the LTC3331 cannot receive battery power. With the switch in its default position, all of the energy-harvesting ICs have the potential to be powered by a battery.

SW4: Connects the supercapacitor storage to either the LTC3330 or the LTC3331.

SW7: Connects/disconnects both the primary and secondary batteries from the board. In the CCTR position, batteries are routed through the coulomb counters on DC2321A for monitoring. Connected batteries must be routed to ICs using JP5-JP8.

Table 4. Switch Functions

REFERENCE	NAME	FUNCTION	POSITION		RESULT	NOTES
SW1	ENERGY STORAGE	Select mode for optional energy storage	0	OFF	Optional energy storage disabled.	–
			1	EHVCC	Any V_{OUT} routed to the header uses optional energy storage.	
			2	VSTORE_LTC3107	LTC3107's VSTORE function uses optional energy storage.	
SW2	LTC3106 BATTERY	Select between batteries for LTC3106	0	PRI	LTC3106 uses primary battery, LTC3331 uses secondary.	Battery must still be routed with jumper
			1	SEC	LTC3106 uses secondary battery, LTC3331 uses no battery.	
SW4	SUPERCAP BALANCER	Connect the supercapacitor to the output of an IC	0	OFF	Supercapacitor balancer and storage disabled.	R96-R98 must be populated for active balancing
			1	LTC3330	LTC3330's supercapacitor storage enabled.	
			2	LTC3331	LTC3331's supercapacitor storage enabled.	
SW7	BATTERIES	Connect/ disconnect batteries	0	OFF	Both batteries are disconnected from the board.	JP5-JP8 route batteries to ICs
			1	ON	Both batteries are connected to the board.	
			2	CCTR	Both batteries are routed through coulomb counters on DC2321A.	

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Turret Functions

EHVCC (E1, E2): Regulated Output of all the active Energy Harvester power management circuits, referenced to BGND. When EHVCC is referenced to HGND it is a switched output that is passed through header J1 to power the load.

BGND (E3, E4, E10, E12): This is the Board Ground: the ground reference for the DC2509A. BGND is the reference for all of the parts on the board except the headers. BGND and HGND (the header ground) are connected through Q3 when the EHVCC voltage with respect to BGND reaches the rising reset threshold of the LTC2935-2 and disconnected when EHVCC falls to the falling reset threshold.

HGND (E5, E6): This is the Header Ground: the ground reference for any load that is connected to the DC2509A through one of its output headers. HGND is the switched ground that ensures the load is presented with a quickly rising voltage. BGND and HGND are connected through Q3 when the EHVCC voltage with respect to BGND reaches the rising reset threshold of the LTC2935-2 and disconnected when EHVCC falls to the falling reset threshold (thresholds configurable with R78-R86). The board is configured from the factory to connect BGND and HGND when EHVCC reaches a rising threshold of 2.85V and disconnect them when EHVCC drops below 2.25V.

EH_ON (E7): Energy Harvesting On output signal of the IC selected using JP17. A high EH_ON signal is generally an indication that the IC is relying on harvested energy rather than battery energy. The LTC3107's equivalent signal (BAT_OFF) goes high when the battery is not in use. For the LTC3330 and LTC3331, EH_ON is high when the buck switching regulator is in use (EH input) and it is low when the buck-boost switching regulator is in use (battery input). The LTC3106 does not output an EH_ON signal.

PGOOD (E8): Power Good output of the IC selected using JP18. PGOOD transitioning high indicates that regulation has been reached on V_{OUT}. Specific operation depends on which IC is generating the signal. For the universal PGOOD signal that is generated by the LTC2935-2, the rising threshold is 2.85V and the falling threshold is 2.25V. The universal PGOOD signal will switch for any of the EH ICs and can be routed to the turret by installing JP18B.

VIN_LTC3106 [330mV to 5.0V] (E9): External energy harvester input to the LTC3106.

VIN_LTC3107 [30mV to 500mV] (E11): External energy harvester input to the LTC3107.

AC1_LTC3330 [4V to 19V] (E13): External energy harvester input to AC1 on the LTC3330.

AC2_LTC3330 [4V to 19V] (E14): External energy harvester input to AC2 on the LTC3330.

AC1_LTC3331 [4V to 19V] (E15): External energy harvester input to AC1 on the LTC3331.

AC2_LTC3331 [4V to 19V] (E16): External energy harvester input to AC2 on the LTC3331.

LDO_IN (E17): Input voltage for the LDO regulator of the LTC3330. Populating R99 will connect LDO_IN to VOUT_LTC3330.

LDO_EN (E18): Active-high LDO enable input. The high logic level for this input is referenced to LDO_IN.

LDO_OUT (E19): Regulated LDO output for the LTC3330. The output voltage can be configured using R26-R31.

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LTC3106: Solar Energy Harvester with Primary or Secondary Batteries

The LTC3106 solar powered energy harvester's output (VOUT_LTC3106) can be routed to EHVCC by installing the power selection jumper JP1. The PGOOD_LTC3106 signal can be routed to the PGOOD turret by installing JP18A. The LTC3106 does not output an EH_ON indication.

SW2 toggles between the primary or secondary batteries as the backup power source for the LTC3106, and JP5 connects the selected battery to the IC's VSTORE input. Because the LTC3106 requires a logic signal to its PRI pin in order to determine which battery is attached and enable/disable charging, SW2 also routes the appropriate signal to the IC.

The operation of the LTC3106 is configurable using 0Ω resistors as jumpers. These resistors are located in tables on the back of the board. Table 16 is a guide for these resistors and describes each of their functions.

The LTC3106 has the option to enable an undervoltage threshold for LDO regulation. This threshold can be set using the voltage divider formed by R1 and R2 on the bottom of the board. In order to optimize the power drawn from a solar cell, this voltage divider should be configured so that the voltage on the RUN pin is near the maximum power point of the cell. Because the voltage feeding the resistor divider, V_{IN}, is subject to fluctuate with light levels, the voltage on the RUN pin will not be the same for all intensities of light. This feature can be enabled/disabled by installing R3 or R4 respectively.

As another option to optimize the LTC3106's operation with a specific solar cell, the board allows programming of the MPPC comparator's activation point using R18. This feature can be disabled/enabled by installing R16 or R17 respectively; when MPPC is enabled, the RUN pin's UVLO function should be disabled using R3/R4 (see Table 16). The MPP pin sources a nominal current of 1.5µA, so the resistor value can be calculated for a specific solar cell's V_{MP} using:

$$R18 = \frac{V_{MP}}{1.5\mu A}$$

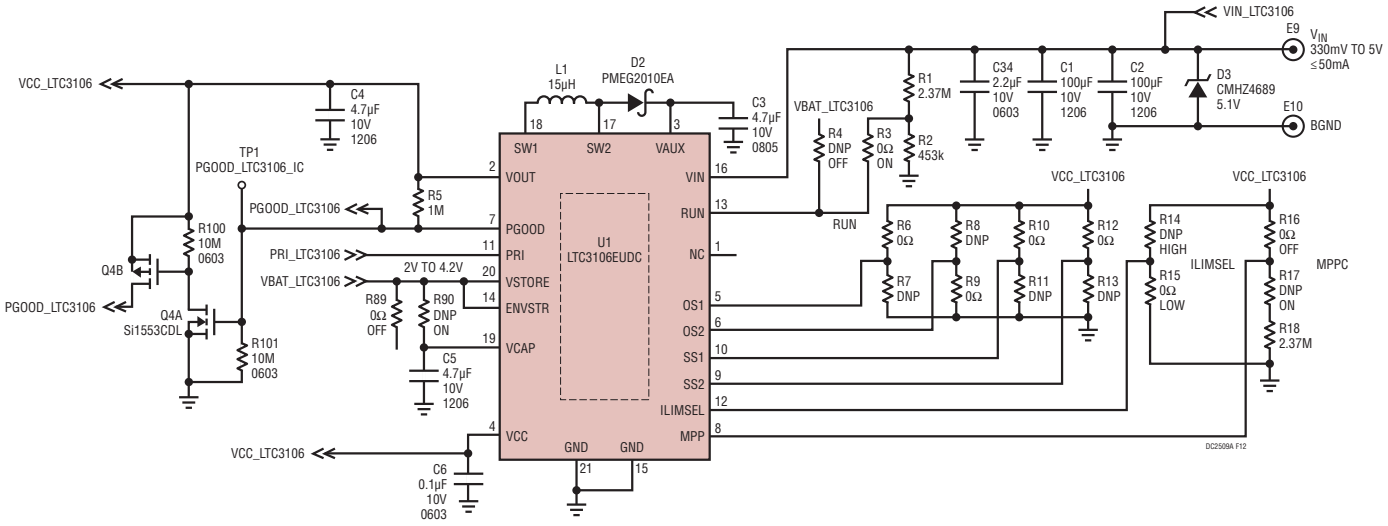


Figure 12. Schematic of LTC3106 Solar Energy Harvesting Power Supply

APPLICATION

LTC3107: TEG Energy Harvester with Primary Battery

The LTC3107 TEG powered energy harvester's output (VOUT_LTC3107) can be routed to EHVCC by installing the power selection jumper JP2. Because the LTC3107 does not output its own PGOOD signal, an additional LTC2935-2 generates a PGOOD signal based on the output voltage of the IC. This PGOOD_LTC3107 signal can be routed to the PGOOD turret by installing Jumper JP18B. The LTC3107's BAT_OFF signal can be routed to the EH_ON turret by installing JP17A.

Unlike the other ICs, the LTC3107 requires a battery to start up and adapts its output to match the voltage of its battery. With no harvested energy available, V_{OUT} will be regulated to a voltage about 230mV below the battery. While harvesting energy, the LTC3107 preserves the life of its battery and regulates its output to about 30mV below the battery voltage.

When SW1 is in the VSTORE_LTC3107 position, the optional energy storage capacitors (CO1-CO10) are connected to the LTC3107's VSTORE input to store excess harvested energy and further extend the primary battery's life.

When SW7 is ON and JP6 is installed, the primary battery is routed to the LTC3107's V_{BAT} input. As a result of the output's dependence on the battery voltage, the primary battery needs to operate at a minimum voltage in order for HGND switching to occur. For correct operation, the primary battery must have a voltage of at least:

$$V_{PRI} > V_{RISING} + 230mV$$

For the LTC2935-2's default rising threshold of 2.85V,

$$V_{PRI} > 2.85V + 230mV = 3.08V$$

If the primary battery's voltage drops below 3.08V, it should be replaced or used exclusively with other ICs. Alternatively, a backup source with a higher voltage can be used or the rising threshold of the LTC2935-2 can be lowered to accommodate the LTC3107's battery-dependent output voltage level (the resistor configuration for this lower threshold is given in Table 5). The default rising threshold is configured to allow the LTC3107's output to switch HGND but, if the LTC3107 is not being evaluated, a higher rising threshold can be used and will result in a wider hysteresis window for the other EH ICs.

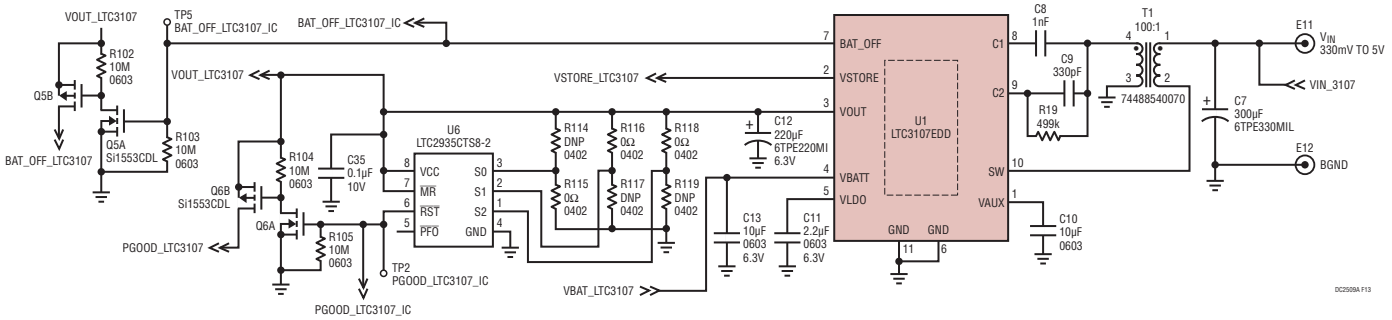


Figure 13. Schematic of LTC3107 TEG Energy Harvesting Power Supply

APPLICATION

LTC3330: Hi-Z AC, Piezoelectric, and Solar Energy Harvester with Primary Battery

The LTC3330 Hi-Z AC/piezoelectric/solar powered energy harvester's output (VOUT_LTC3330) can be routed to EHVCC by installing the power selection jumper JP3. The PGOOD_LTC3330 signal can be routed to the PGOOD turret by installing JP18C. EH_ON_LTC3330 can be routed to the EH_ON turret by installing JP17B.

An external piezoelectric or other high-impedance AC source can be routed to the LTC3330's input turrets. If one terminal of the source is connected to BGND and the other is connected to either AC1 or AC2, this creates a voltage-doubler configuration. Alternatively, if one terminal of the source is connected to AC1 and the other terminal is connected to AC2, the device is full-wave rectified. See Figure 21 for a visual of these configurations.

When SW7 is ON and JP7 is installed, the primary battery is routed to the LTC3330.

The LTC3330 has a configurable LDO regulator which can be set to different output voltages by moving R26-R31. Three turrets (LDO_IN, LDO_EN, and LDO_OUT) are available to access the inputs and outputs of the LDO. LDO_IN can be pulled to the LTC3330's output, VOUT_LTC3330, by installing R99. The regulator is enabled by pulling LDO_EN high with reference to LDO_IN.

If the application would benefit from a wider PGOOD hysteresis window than the LTC3330 provides, the PGOOD_LTC2935-2 signal can be used in place of any of the PGOOD signals generated by the harvester circuits.

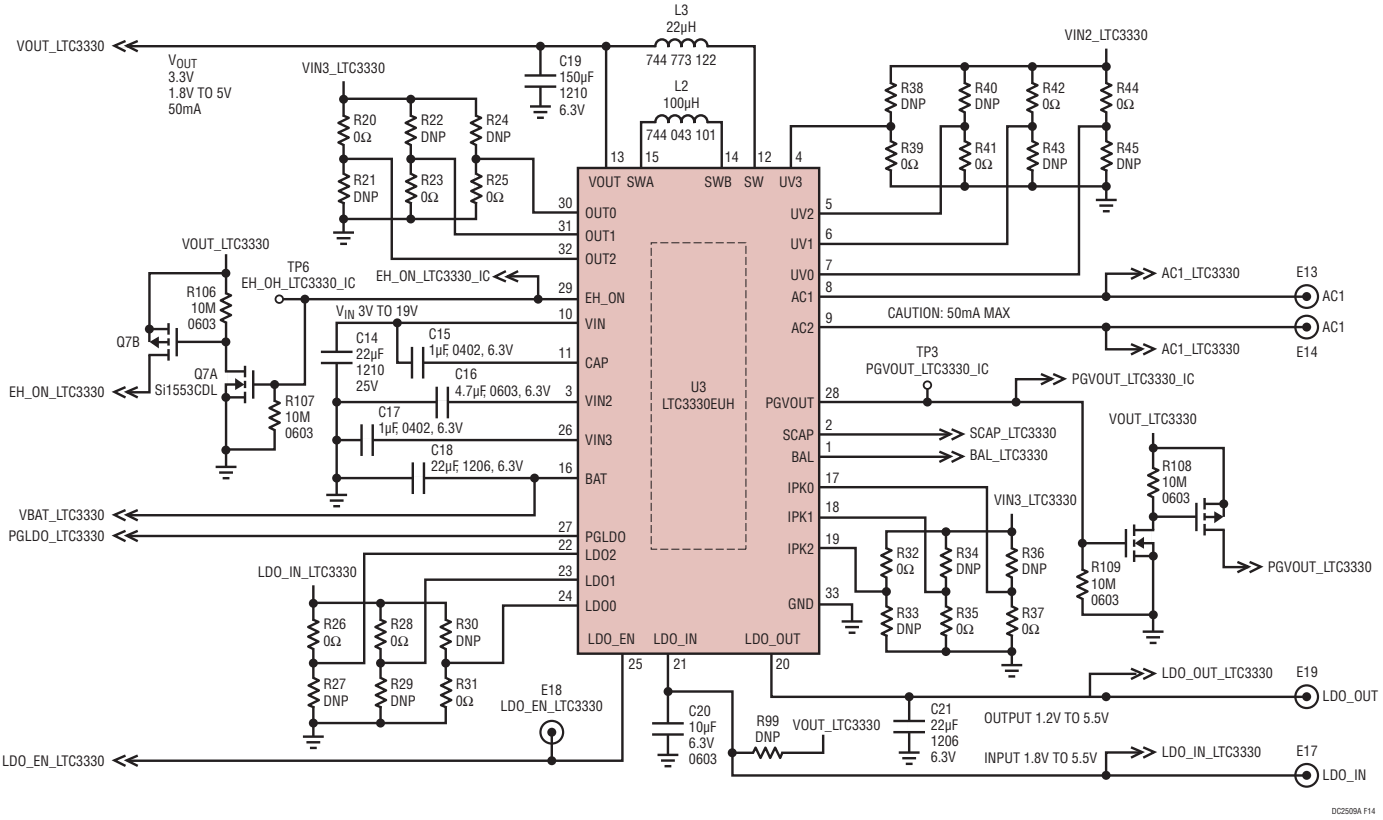


Figure 14. Schematic of LTC3330 Hi-Z AC, Piezoelectric, and Solar Energy Harvesting Power Supply

APPLICATION

LTC3331: Hi-Z AC, Piezoelectric, and Solar Energy Harvester with Secondary Battery

The LTC3331 Hi-Z AC/piezoelectric/solar powered energy harvester's output (VOUT_LTC3331) can be routed to EHVCC by installing the power selection jumper JP4. The PGOOD_LTC3331 signal can be routed to the PGOOD turret by installing Jumper JP18D. EH_ON_LTC3331 can be routed to the EH_ON turret by installing JP17C.

An external piezoelectric or other high-impedance AC source can be routed to the LTC3331's input turrets. If one terminal of the source is connected to BGND and the other is connected to either AC1 or AC2, this creates a voltage-doubler configuration. Alternatively, if one terminal of the source is connected to AC1 and the other terminal is connected to AC2, the device is full-wave rectified. See Figure 21 for a visual of these configurations.

The operation of the LTC3331 is configurable using JP19 and JP20. Charging of the secondary battery is configurable using JP20. In its OFF position, there will be no current sourced to the battery. In the CHARGE position, the battery is charged through resistor R76. For higher charging currents up to 10mA, JP20 should be placed in the FAST CHG position. In this mode, the battery is charged using external circuitry connected to the LTC3331 and the battery charge current can be set based on the value of R72.

A SHIP mode is provided which manually disconnects the battery. This may be helpful for preventing discharge of the battery when no harvestable energy is available for long periods of time such as during shipping. To disengage SHIP mode, JP19 should be installed in the RUN position.

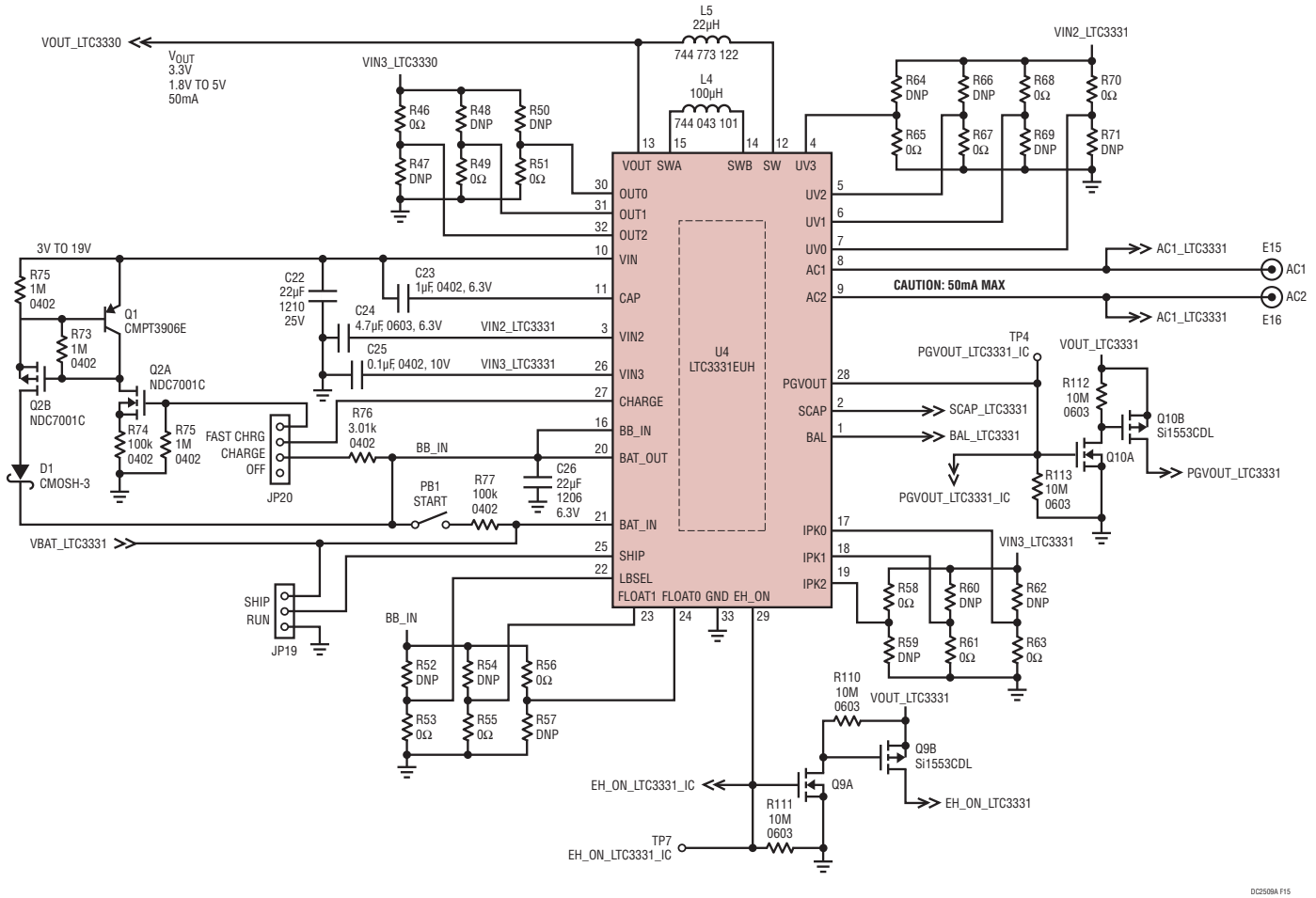


Figure 15. Schematic of LTC3331 Hi-Z AC, Piezoelectric, and Solar Energy Harvesting Power Supply

APPLICATION

When SW7 is ON and JP8 is installed, the secondary battery is routed to the LTC3331's BAT_IN pin. To connect the battery internally, JP19 must be set to RUN and the BB_IN pin needs to be brought above the BAT_OUT connect threshold.

There are two ways this can be achieved:

1. The IC has reached regulation using EH power and the battery voltage is greater than the BAT_IN connect threshold voltage (EH column in Table 12).
2. The battery voltage is greater than the BAT_OUT connect threshold voltage (PB1 column in Table 12) and tactile switch PB1 is pressed momentarily.

By default, the BAT_IN connect threshold is set to 3.03V and the BAT_OUT connect threshold is set to 3.70V. These thresholds (along with the battery disconnect and float voltages) can be adjusted using R52-R57. Note that the PB1 function does not work for settings where the BAT_OUT threshold is greater than the float voltage.

If the application would benefit from a wider PGOOD hysteresis window than the LTC3331 provides, the PGOOD_LTC2935-2 signal can be used in place of any of the PGOOD signals generated by the harvester circuits.

LTC2935-2 Power Switch Circuit

If the application requires a wide hysteresis window for the PGOOD signal, the board has the ability to use an independent PGOOD signal which is generated by the LTC2935-2 and available on JP18B. This signal acts as the PGOOD signal for the LTC3107 circuit because the LTC3107 does not have its own PGOOD output, but the PGOOD_LTC2935-2 signal can be used in place of any of the PGOOD signals generated by the harvester circuits.

Some loads do not like to see a slowly rising input voltage. Switch Q3 ensures that EHVCC on the header is off until the energy harvested output voltage is high enough to power the load. By default, the LTC2935-2 is configured to turn on Q3 at 2.85V and turn off Q3 at 2.25V. With this switching, the load will see a fast voltage rise at startup and be able to utilize all of the energy stored in the output capacitors between the 2.85V and 2.25V levels.

The DNP and 0Ω resistors (R78-R86) near the LTC2935-2 allow for customization of the PGOOD thresholds and hysteresis window. By modifying R84-R86, the digital inputs (S0, S1, S2) can be toggled when the rising or falling threshold is reached.

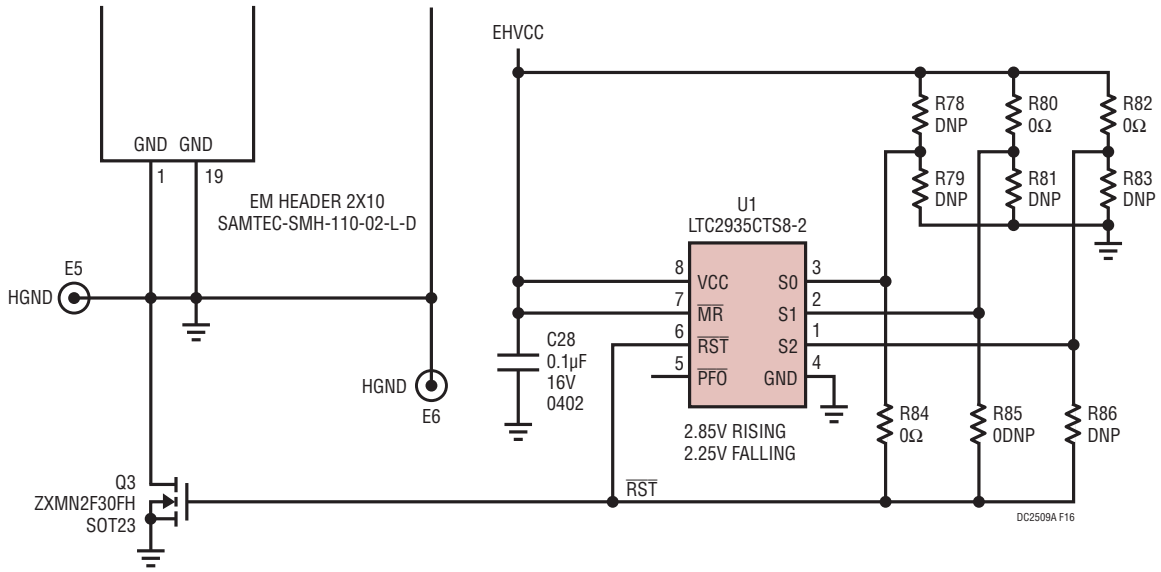


Figure 16. Schematic of LTC2935-2 Low-Power Supervisor and HGND Switching Circuit

APPLICATION

A hysteresis ('H') resistor acts as a '0' until the rising threshold is met, then becomes a '1'. Once the voltage drops below the falling threshold again, it becomes a '0'. In this way, the inputs of the LTC2935-2 can be reconfigured during operation to create a wider hysteresis window.

Table 5 shows a few recommended 0Ω resistor configurations that will result in the widest possible hysteresis windows for different rising threshold voltages. The best value for this threshold depends on which IC is being evaluated. The default setting allows the output voltage of any IC to switch the header ground, but the hysteresis window can be optimized to suit a particular IC output or application.

Table 5. Possible Settings for Widest Hysteresis Windows

ENERGY HARVESTER BEING EVALUATED	S0	S1	S2	FALLING THRESHOLD	RISING THRESHOLD
All	H	1	1	2.25V	2.85V
All Except LTC3107	1	1	H	2.25V	3.15V
Only LTC3107	H	H	1	2.25V	2.70V

The recommendations in this table are based on the default output voltage configuration where EHVCC = 3.3V.

Signal Buffering

Because DC2509A switches the ground on the output header once a target voltage threshold is reached, it is necessary to buffer any output signal that will come directly in contact with the mote. Without buffering, a signal that is outputting a logic low will give the load an unintended ground reference, causing it to draw power before the ground switching occurs. This happens as the result of a sneak path within the processor.

To prevent this, a simple FET buffer circuit is employed on all IC status signals which cross the output header, J1. With a high input signal, the N-channel FET is enhanced and pulls the P-channel gate low to connect the output to VREF. With a low input signal, the N-channel FET is off and the gate of the P-channel FET is pulled high through a resistor to keep the FET off; in this state, the output is not connected to ground, but is instead a high-impedance node.

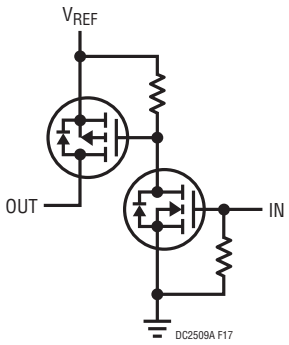


Figure 17. Simple Signal Buffer/Level Translator Circuit

On DC2321A, a pull-down resistor on the output of each buffer ensures that the signal is read as a logic low when the node is high-impedance. These resistors are pulled down to GND on DC2321A which is equivalent to HGND on DC2509A.

In addition to preventing sneak paths, the buffers also provide a voltage translation to V_{REF}. Because the LTC3330 and LTC3331 status output signals are at voltages referenced to internal rails, this voltage translation is necessary to prevent damage to the mote.

Status Signal Selection

The LTC3107, LTC3330, and LTC3331 ICs each output a logic signal indicating when they are powering the load using harvested energy rather than a backup source. Using JP17, one of these signals can be routed to the EH_ON turret.

Table 6. Presence of PGOOD / EH_ON Signals for Each IC

IC	EH_ON	PGOOD
LTC3106	–	Yes
LTC3107	Yes	Generated by LTC2935-2
LTC3330	Yes	Yes
LTC3331	Yes	Yes

Similarly, the LTC3106, LTC3330, and LTC3331 ICs each output a logic signal indicating when the output (V_{OUT}) has reached regulation. Because the LTC3107 does not inherently generate this signal, an additional LTC2935-2

APPLICATION

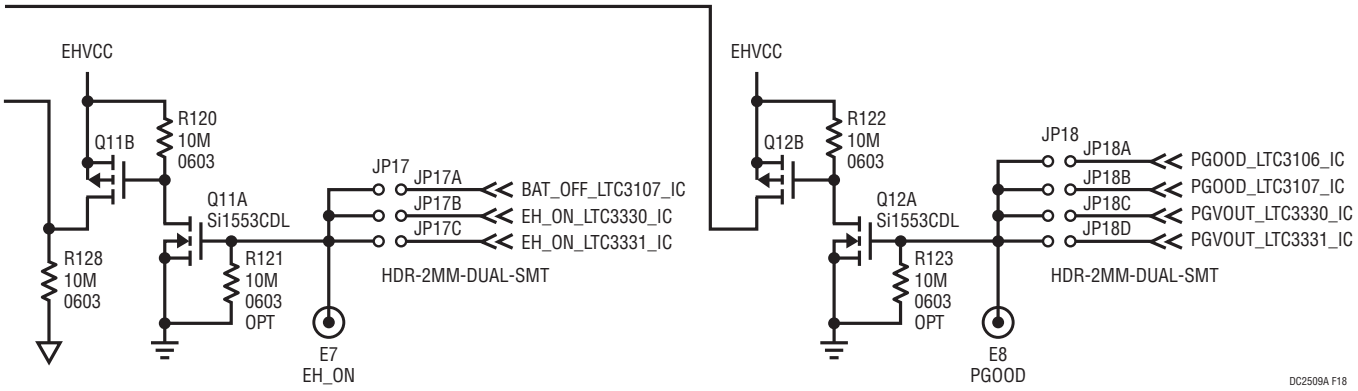


Figure 18. EH_ON and PGOOD Selection Jumpers and Turrets

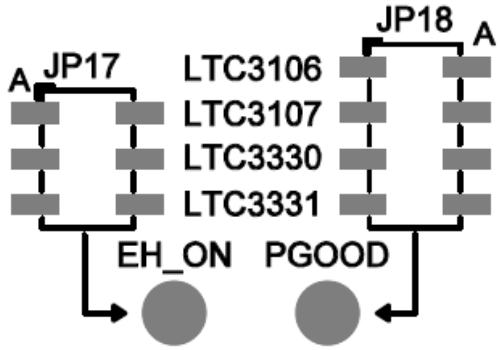


Figure 19. Signal Selection Layout

monitors its output to create its PGOOD signal. Using JP18, one of these signals can be routed to the PGOOD turret.

The name of each relevant IC is located between its appropriate EH_ON jumper and PGOOD jumper (see Figure 19). Jumper reference designators are listed on the assembly drawing.

DC9003A-B Integration

Header J2 is intended for use with the DC9003A-A/B Dust manager/mote evaluation board. The EH_ON and PGOOD signals selected by JP17 and JP18 are routed through buffers to the applicable inputs on the Dust board. When the selected PGOOD signal is low, the Dust board will use power from its own on-board battery. When PGOOD is high, power is drawn from EHVCC on DC2509A.

In order to properly interface with DC2509A, R3 on DC9003A must be changed to 750kΩ.

Ceramic Capacitor Storage

The DC2509A hosts a bank of ten optional energy storage capacitors which can be configured using SW1. In the OFF position, the capacitors are disconnected from the rest of the circuit. If SW1 is set to EHVCC, the capacitors are connected to the output voltage, EHVCC. If SW1 is set to VSTORE_LTC3107, the capacitors are connected to VSTORE on the LTC3107 and are used in the IC's own storage function.

At the default EHVCC voltage of 3.3V, the actual capacitance of each capacitor is about 80µF. This gives the storage bank a combined capacitance of about 800µF. Therefore, with the default voltage and switching threshold configurations, the ceramic capacitor bank is able to store about:

$$\text{Stored Energy}|_{V1-V2} = ½\ C\ V_1^2 - ½\ C\ V_2^2$$
$$= ½\ C\ (V_1^2 - V_2^2)$$
$$= ½\ (0.0008) \bullet (3.3^2 - 2.25^2)$$
$$= 2.331\text{mJ}$$

between 3.3V and the 2.25V LTC2935-2 falling threshold.

Supercap Storage and Active Balancer

The supercapacitor supplied with the board allows the storage of much more energy than can be stored by the bank of ceramic capacitors. At the default EHVCC voltage of 3.3V, the actual capacitance of the supercapacitor is about 13mF. Based on the above calculations, the supercapacitor is able to store 37.88mJ between 3.3V and the 2.25 default LTC2935-2 falling threshold.

APPLICATION

SW4 allows the supercapacitor to be disconnected or tied to the output of either the LTC3330 or the LTC3331. The supercapacitor that is populated by default does not have a balance pin and therefore does not need the active balancing feature of the LTC3330 or the LTC3331.

However, the board does allow the use of active balancing with alternate supercapacitors. In the case that the user wishes to use a supercapacitor with active balancing, C31 can be populated. This footprint is designed to fit CAP-XX supercapacitors in A-Type packages. See Table 7 for recommended parts that will fit the pads on the board.

Table 7. Recommended Supercapacitors

TYPE	CAPACITANCE	PART NUMBER	MANUFACTURER
WITH BALANCE PIN	85mF	GA209F	CAP-XX
	120mF	HA202F	CAP-XX
	400mF	HA230F	CAP-XX
WITHOUT BALANCE PIN	4.7mF	BZ05KB472ZSB	AVX
	15mF	BZ055B153ZSB	AVX
	33mF	BZ055B333ZSB	AVX

Before installing C31, be sure to place insulating tape over the specified contacts of C30; the note for doing so can be seen on the bottom assembly drawing as well as underneath C30 on the back of the board.

The active balancing feature is disabled/enabled through the installation of the 0Ω resistors R93-R98. By default, balancing is disabled and R93-R95 are installed. To enable balancing, these three resistors should be moved to R96-R98. Only one group of three resistors should be populated at a time.

Power Selection Diodes

Diodes D4-D7 are optional components used to "Diode-OR" multiple energy harvesting sources together. When the OR-ing diodes are installed, all of the power routing jumpers (JP1-JP4) should be off. The diode drop will be subtracted from the output voltage setpoint, so it is recommended to select a higher output voltage to compensate for the diode drop. When more than one of these diodes is installed and the associated energy harvester inputs are powered, the board will switch between energy harvester power circuits as needed to maintain the output voltage.

At some level of current dependent on the components used, an ideal diode IC becomes more efficient than regular diodes. At low load currents, regular diodes are more efficient because their power consumption is dependent upon the current being passed through. At higher currents, and ideal diode IC becomes more efficient because it requires only a quiescent current and power dissipation is not directly dependent on the current.

APPLICATION

The following tables show how to configure some settings for the LTC2935-2, LTC3106, LTC3330, and LTC3331. Moving the supplied 0Ω jumper resistor into the appropriate '1' or '0' row will pull the appropriate pin high or low and change some functionality according to the relevant table.

All of the necessary jumper resistors for these functions are supplied with the board, so no additional parts should be needed. Do not populate both the '1' and '0' resistor in the same column for any table as this will result in a short circuit.

	S0	S1	S2
1	R78	R80	R82
0	R79	R81	R83
H*	R84	R85	R86

*HYSTERESIS

DC2509A F20a

Figure 20a. Front 0Ω Resistor Jumpers for Table 8

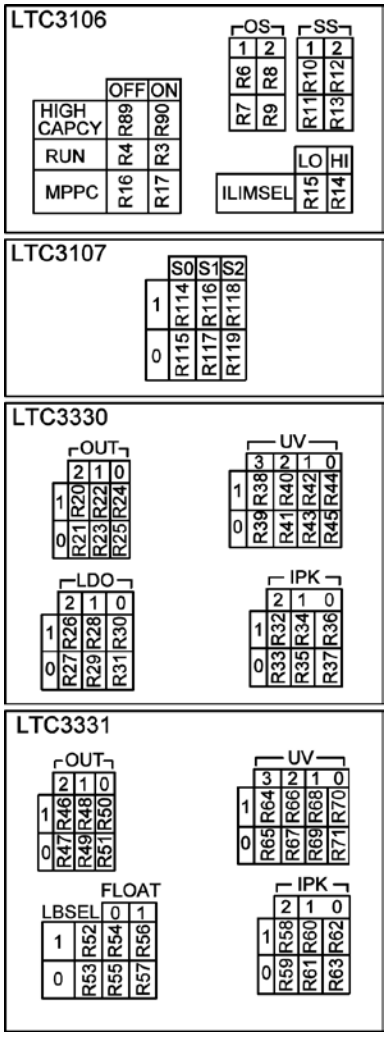


Figure 20b. Back 0Ω Resistor Jumpers for Tables 9-15

CONFIGURATION TABLES

LTC2935-2

Table 8. PGOOD Threshold Selection

S0	S1	S2	RESET THRESHOLD	POWER-FAIL THRESHOLD	
0	0	0	3.30V	3.45V	
1	0	0	3.15V	3.30V	
1	1	0	3.00V	3.15V	
0	1	0	2.85V	3.00V	
0	1	1	2.70V	2.85V	Default Rising
0	0	1	2.55V	2.70V	
1	0	1	2.40V	2.55V	
1	1	1	2.25V	2.40V	Default Falling

LTC3106

Table 9. V_{OUT} Selection

OS1	OS2	V_{OUT}
0	0	1.8V
0	1	3.0V
1	0	3.3V
1	1	5.0V

Table 10. V_{STORE} Selection

SS1	SS2	V_{STORE}
0	0	2.07V
0	1	2.9V
1	0	3.015V
1	1	4.0V

LTC3330

Table 11. LDO Voltage Selection

LDO2	LDO1	LDO0	LDO_OUT
0	0	0	1.2V
0	0	1	1.5V
0	1	0	1.8V
0	1	1	2.0V
1	0	0	2.5V
1	0	1	3.0V
1	1	0	3.3V
1	1	1	= LDO_IN

LTC3331

Table 12. Float Selection

				CONNECT		
LBSEL	FLOAT1	FLOAT0	FLOAT	EH	PB1	DISCONNECT
0	0	0	3.45V	2.35V	3.02V	2.04V
0	0	1	4.0V	3.03V	3.70V	2.70V
0	1	0	4.1V	3.03V	3.70V	2.70V
0	1	1	4.2V	3.03V	3.70V	2.70V
1	0	0	3.45V	2.85V	N/A	2.51V
1	0	1	4.0V	3.53V	N/A	3.20V
1	1	0	4.1V	3.53V	N/A	3.20V
1	1	1	4.2V	3.53V	N/A	3.20V

NOTE: Shaded Rows Represent Default Configuration Settings

CONFIGURATION TABLES

LTC3330 & LTC3331

Table 13. Output Voltage Selection

OUT2	OUT1	OUT0	V_{OUT}
0	0	0	1.8V
0	0	1	2.5V
0	1	0	2.8V
0	1	1	3.0V
1	0	0	3.3V
1	0	1	3.6V
1	1	0	4.5V
1	1	1	5.0V

Table 14. I_{PEAK_BB} Selection

IPK2	IPK1	IPK0	I_{LIN}	L_{MIN}
0	0	0	5mA	1000µH
0	0	1	10mA	470µH
0	1	0	15mA	330µH
0	1	1	25mA	220µH
1	0	0	50mA	100µH
1	0	1	100mA	47µH
1	1	0	150mA	33µH
1	1	1	250mA	22µH

Table 15. V_{IN} UVLO Threshold Selection

UV3	UV2	UV1	UV0	UVLO RISING	UVLO FALLING
0	0	0	0	4V	3V
0	0	0	1	5V	4V
0	0	1	0	6V	5V
0	0	1	1	7V	6V
0	1	0	0	8V	7V
0	1	0	1	8V	5V
0	1	1	0	10V	9V
0	1	1	1	10V	5V
1	0	0	0	12V	11V
1	0	0	1	12V	5V
1	0	1	0	14V	13V
1	0	1	1	14V	5V
1	1	0	0	16V	15V
1	1	0	1	16V	5V
1	1	1	0	18V	17V
1	1	1	1	18V	5V

NOTE: Shaded Rows Represent Default Configuration Settings

APPLICATION

0Ω Resistor Jumper Functions

Table 16. 0Ω Resistor Jumper Functions

RELEVANT PART	RESISTORS	FUNCTION	DEFAULT POSITION	DEFAULT MODE	DESCRIPTION
LTC3106	R3, R4	RUN Threshold ON/OFF	R3	RUN Threshold	Enable/Disable Undervoltage Threshold Mode for V_{IN} on the LTC3106. The Undervoltage Threshold Is Configurable by Changing the Values of the Resistors in the External Voltage Divider (R1 and R2)
	R6-R9	Set V_{OUT}	R6, R9	V_{OUT} = 3.3V	Sets Output Regulation Voltage Output. See Table 9
	R10-R13	Set V_{STORE}	R10, R12	V_{STORE} = 4.0V	Sets V_{STORE} Operating Voltage. See Table 10
	R14, R15	Set Peak Current Limit	R15	Low Current Limit	Selects the Peak Current Limit for the LTC3106 by Enabling/Disabling the Automatic Power Adjust Feature. In LOW Mode, the LTC3106 Will Operate at the Lowest Peak Current and in HIGH Mode it Will Operate at Higher Peak Currents
	R16, R17	MPPC OFF/ON	R16	MPPC Disabled	Disables/Enables Maximum Power Point Control for Efficient Energy-Harvesting. The Activation Point for the MPP Comparator is Programmable Using R18. The Nominal MPPC Current is 1.2µA, so the Nominal Set Point is V_{MPPC} = 1.2µA • R18
	R89, R90	Set Battery Capacity	R89	Low Capacity Battery	Selects High/Low Battery Capacity Mode for the LTC3106. The Batteries Supplied with the Board are Considered Low-Capacity
LTC3330	R20-R25	Set V_{OUT}	R20, R23, R25	V_{OUT} = 3.3V	Sets Output Regulation Voltage Output. See Table 13
	R26-R31	Set LDO Voltage	R26, R28, R31	LDO_OUT = 3.3V	Sets Low-Dropout Regulated Voltage Output. See Table 11
	R32-R37	Set I_{PEAK_BB}	R32, R35, R37	I_{LIN} = 50mA	Sets Current Limit for the LTC3330's Buck-Boost Switching Regulator. See Table 14
	R38-R45	Set UVLO	R39, R41, R42, R44	RISING = 7V FALLING = 6V	Sets Undervoltage Lockout Thresholds for the LTC3330's Buck Switching Regulator. See Table 15
	R99	Set LDO_IN	DNP	LDO_IN Floating (LDO Disabled)	Ties LDO_IN to VOUT_LTC3330
LTC3331	R46-R51	Set V_{OUT}	R46, R49, R51	V_{OUT} = 3.3V	Sets Output Regulation Voltage Output. See Table 13
	R52-R57	Set Float, Connect, and Disconnect	R53, R55, R56	FLOAT = 4.0V CONNECT = 3.03V DISCONNECT = 2.70V	Selects Battery Float Voltage and Connect/Disconnect Voltage Levels. See Table 12
	R58-R63	Set I_{PEAK_BB}	R58, R61, R63	I_{LIN} = 50mA	Sets Current Limit for the LTC3331's Buck-Boost Switching Regulator. See Table 14
	R64-R71	Set UVLO	R65, R67, R68, R70	RISING = 7V FALLING = 6V	Sets Undervoltage Lockout Thresholds for the LTC3331's Buck Switching Regulator. See Table 15
LTC2935-2	R78-R86	Set PGOOD Thresholds	R80, R82, R84	RISING = 2.85V FALLING = 2.25V	Sets Rising/Falling Thresholds for the LTC2935-2's Generated PGOOD Signal Which Switches HGND = BGND. NOTE: Only One Hysteresis Jumper (R84, R85, R86) Should be Installed at a Time. See Table 8
Supercap	R93-R98	Balance OFF/ON	R93-R95	Active Balancing Disabled	Disables/Enables Active Balancing Using the BAL Pin of a Supercapacitor. Install R93-R95 to Disable Balancing or Install R96-R98 to Enable Balancing. Only One Group Can be Populated at Once. The Default Capacitor Does Not Allow Balancing

TRANSDUCERS

Solar Cells

The DC2509A allows solar cells to be connected using the energy harvesting transducer input turrets. Some options for solar cells are listed in Table 17.

The LTC3106 operates near the maximum power point of the cells in parallel using the undervoltage threshold function on its RUN pin. This function is enabled/disabled using R3/R4 and configured using R1/R2. See Table 16 for details.

LTC3330 and LTC3331 are able to regulate their input near the max power point of a solar panel using a UVLO function. The UVLO rising and falling thresholds can be configured to straddle the VMPP of solar cells in order to extract max power. See Table 15 for details.

TEG

Power from a TEG is generated based on a temperature differential across its surfaces. However, without proper thermal management, a temperature applied to one side will eventually permeate through the device and even out the thermal gradient across the junction, reducing power output.

As a result, proper heat sinking is necessary in applications where the thermal gradient is created by the differential between the ambient temperature and one other temperature source. In these applications, the heat sink helps to keep one side of the device near room temperature.

In applications where two temperature sources are present (excluding ambient temperature), heat sinking may not be necessary. For example, if one hot and one cold source are near each other and a TEG is placed between them, the sources will hold each side of the TEG near their temperature, and a heat sink is not needed.

Table 17. Recommended Solar Cells

MPP OUTPUT (600 LUX)			MANUFACTURER/PART NUMBER	SUGGESTED IC
V_{MPP} (V)	I_{MPP} (µA)	P_{MPP} (µW)		
3.28	27	89	China Solar LTD, KS-3726-8	LTC3106 (Single/Parallel) LTC3330/LTC3331 (Series)
0.49	457	224	Fujikura, FDSC-FTC6	LTC3106 (MPP function)
1.64	122	200	Panasonic, AM-5412CAR	LTC3106 (RUN function)

TRANSDUCERS

Piezoelectric or High-Z AC Input

The energy harvesting input turrets allow users to connect a piezoelectric, or any other high-impedance AC or DC energy harvesting device, to the rectified AC1 and AC2 inputs of the LTC3330 and LTC3331. Sources routed to these inputs have the option to be configured in voltage doubler or full-wave rectifier mode.

For voltage doubler configuration, one side of the device is grounded while the other is routed to an IC's AC1 or AC2 input. This general configuration is shown in Figure 21a. In voltage doubler mode, the UVLO window should be set to the open circuit voltage of the piezo device.

For full-wave rectifier configuration, the device is routed across an IC's AC1 and AC2 inputs. This general configuration is shown in Figure 21c. In full-wave rectifier mode, the UVLO window should be set to approximately half the open circuit voltage of the piezo device.

Figure 21b shows the internal rectifier circuit that is common to both the LTC3330 and the LTC3331. This input is capable of accepting power from a wide range of AC or DC sources.

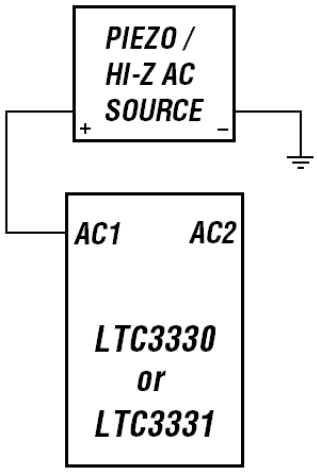


Figure 21a. Voltage Doubler Mode

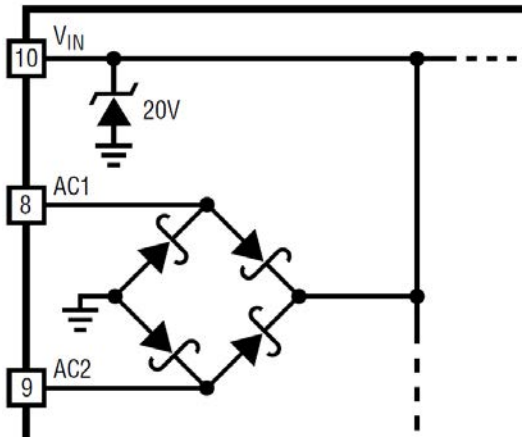


Figure 21b. LTC3330 and LTC3331 Internal Rectifier

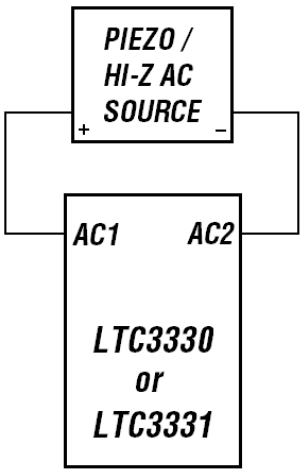


Figure 21c. Full-Wave Rectifier Mode

Figure 21.

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
LTC3106 Circuit Components				
1	2	C1, C2	CAP, CHIP, 100µF, 10V, 20%, X5R, 1206	TDK, C3216X5R1A107M160AC
2	1	C3	CAP, CHIP, 4.7µF, 10V, 10%, X7R, 0805	WURTH, 885 012 207 025
3	2	C4, C5	CAP, CHIP, 47µF, 10V, 20%, X5R, 1206	WURTH, 885 012 108 012
4	1	C6	CAP, CHIP, 0.1µF, 10V, 10%, X7R, 0603	WURTH, 885 012 206 020
5	1	C34	CAP, CHIP, X7R, 2.2µF, 10%, 10V, 0603	WURTH, 885012206027
6	1	D2	DIODE SCHOTTKY 20V, 1A, SOD-323	NXP, PMEG2010EA
7	1	D3	DIODE ZENER (5.1V, 55mA, REVERSE)	CENTRAL, CMHZ4689
8	1	L1	INDUCTOR, SHIELDED 15µH, 1.03A, 0.22Ω, 4.8mm × 4.8mm	WURTH, 744042150
9	2	R1, R18	RES, CHIP, 2.37MΩ, 1%, 1/10W, 0603	VISHAY, CRCW06032M37FKEA
10	1	R2	RES, CHIP, 453kΩ, 1%, 1/10W, 0603	VISHAY, CRCW0603453KFKEA
11	1	R5	RES, CHIP, 1MΩ, 1/10W, 1%, 0603	PANASONIC, ERJ-3EKF1004V
12	1	U1	LOW QUIESCENT CURRENT, BUCK-BOOST POWER MANAGER WITH MPPC	LINEAR TECH, LTC3106EUDC
LTC3107 Circuit Components				
13	1	C7	CAP, TANTALUM-POLYMER, 330µF, 6.3V, 20%	PANASONIC, 6TPE330MIL
14	1	C8	CAP, CHIP, 1000pF, 50V, 10%, X7R, 0603	WURTH, 885 012 206 083
15	1	C9	CAP, CHIP, 330pF, 50V, 10%, X7R, 0603	WURTH, 885 012 206 080
16	2	C10, C13	CAP, CHIP, 10µF, 6.3V, 20%, X5R, 0603	WURTH, 885 012 106 006
17	1	C11	CAP, CHIP, X5R, 2.2µF, 6.3V, 20%, 0603	WURTH, 885 012 106 004
18	1	C12	CAP, TANTALUM-POLYMER, 220µF, 6.3V, 20%	PANASONIC, 6TPE220MI
19	1	C35	CAP, CHIP, X5R, 0.1µF, 20%, 10V, 0402	WURTH, 885 012 105 010
20	1	R19	RES, CHIP, 499kΩ, 1/10W, 0603	PANASONIC, ERJ-3EKF4993V
21	1	T1	TRANSFORMER, 100:1 TURNS RATIO, 6.0mm × 6.0mm	WURTH, 74488540070
22	1	U2	ULTRALOW VOLTAGE ENERGY HARVESTER/PRIMARY BATTERY LIFE EXTENDER	LINEAR TECH, LTC3107EDD
23	1	U6	IC, ULTRALOW POWER SUPERVISOR WITH POWER-FAIL OUTPUT, TSOT-23	LINEAR TECH, LTC2935CTS8-2
LTC3330 Circuit Components				
24	1	C14	CAP, CHIP, X5R, 22µF, 20%, 25V, 1210	WURTH, 885 012 109 014
25	2	C15, C17	CAP, CHIP, X5R, 1µF, 20%, 6.3V, 0402	WURTH, 885 012 105 006
26	1	C16	CAP, CHIP, X5R, 4.7µF, 20%, 6.3V, 0603	WURTH, 885 012 106 005
27	2	C18, C21	CAP, CHIP, X5R, 22µF, 20%, 6.3V, 1206	WURTH, 885 012 108 003
28	1	C19	CAP, CHIP, X5R, 150µF, 20%, 6.3V, 1210	SAMSUNG, CL32A157MQVNNNE
29	1	C20	CAP, CHIP, 10µF, 6.3V, 20%, X5R, 0603	WURTH, 885 012 106 006
30	1	L2	INDUCTOR, 100µH , 0.51A, 0.60Ω, 4.8mm × 4.8mm	WURTH, 744043101
31	1	L3	INDUCTOR, 22µH, 1.00A, 0.37Ω, 4mm × 4.5mm	WURTH, 744773122
32	1	U3	ENERGY HARVESTING DC/DC WITH BATTERY BACKUP	LINEAR TECH, LTC3330EUH
LTC3331 Circuit Components				
33	1	C22	CAP, CHIP, X5R, 22µF, 20%, 25V, 1210	WURTH, 885 012 109 014
34	1	C23	CAP, CHIP, X5R, 1µF, 20%, 6.3V, 0402	WURTH, 885 012 105 006
35	1	C24	CAP, CHIP, X5R, 4.7µF, 20%, 6.3V, 0603	WURTH, 885 012 106 005

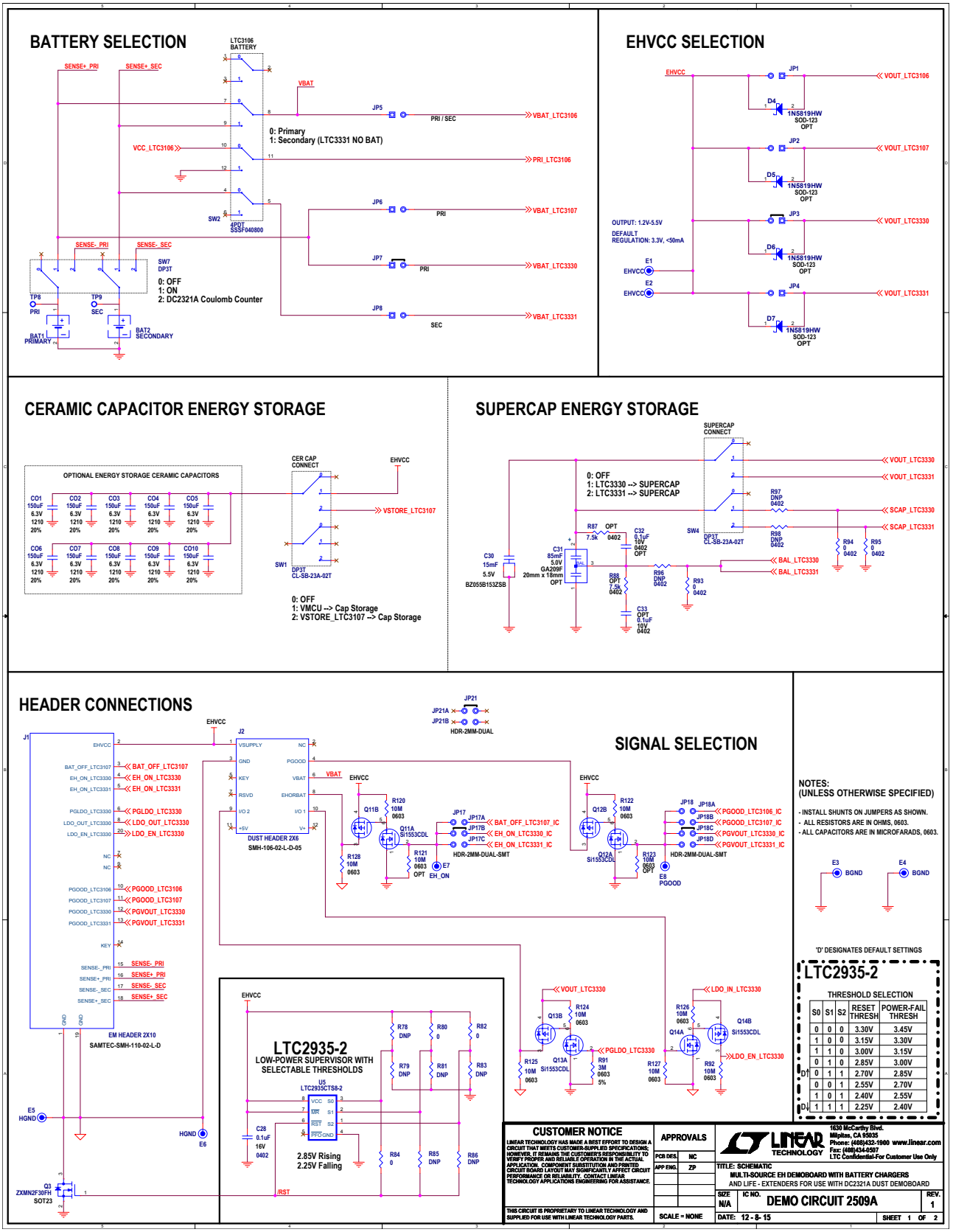
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
36	1	C26	CAP, CHIP, X5R, 22µF, 20%, 6.3V, 1206	WURTH, 885 012 108 003
37	1	C27	CAP, CHIP, X5R, 150µF, 20%, 6.3V, 1210	SAMSUNG, CL32A157MQVNNNE
38	1	C25	CAP, CHIP, X5R, 0.1µF, 20%, 10V, 0402	WURTH, 885 012 105 010
39	1	D1	DIODE, SCHOTTKY, 30V, 0.1A, SOD-523	CENTRAL, CMOSH-3
40	1	L4	INDUCTOR, 100µH , 0.51A, 0.60Ω, 4.8mm × 4.8mm	WURTH, 744043101
41	1	L5	INDUCTOR, 22µH, 1.00A, 0.37Ω, 4mm × 4.5mm	WURTH, 744773122
42	1	Q1	SMT, BIPOLAR, PNP, 40V, SOT-23	CENTRAL, CMPT3906E
43	1	Q2	SMT, DUAL MOSFET, N-CHANNEL/P-CHANNEL, 60V, SuperSOT-6	FAIRCHILD, NDC7001C
44	1	R72	RES, CHIP, 113Ω, 1/16W,1%, 0402	VISHAY, CRCW0402113RFKED
45	2	R73, R75	RES, CHIP, 1MΩ, 1/16W,1%, 0402	VISHAY, CRCW04021M00FKED
46	1	R74	RES, CHIP, 100kΩ, 1/16W,1%, 0402	VISHAY, CRCW0402100KFKED
47	1	R76	RES, CHIP, 3.01kΩ, 1/16W,1%, 0402	VISHAY, CRCW04023K01FKED
48	1	R77	RES, CHIP, 100Ω, 1/16W,1%, 0402	VISHAY, CRCW0402100RFKED
49	1	U4	NANOPOWER BUCK-BOOST DC/DC WITH EH BATTERY CHARGER	LINEAR TECH, LTC3331EUH
Switched Output and Signal Buffering Components				
50	1	C28	CAP, CHIP, X5R, 0.1µF, 20%, 10V, 0402	WURTH, 885 012 105 010
51	1	Q3	N-CHANNEL MOSFET, 30V, SOT23	ZETEX, ZXMN2F30FH
52	11	Q4-Q14	DUAL MOSFET 20V N-TYPE/P-TYPE	VISHAY, SI1553CDL-T1-GE3
53	1	R91	RES, CHIP, 3MΩ, 1%, 1/10W, 0603	VISHAY, CRCW06033M00FKEA
54	24	R92, R100-R113, R120-R128	RES, CHIP, 10MΩ, 1%, 1/10W, 0603	VISHAY, CRCW060310M0FKEA
55	1	U5	IC, ULTRALOW POWER SUPERVISOR WITH POWER-FAIL OUTPUT, TSOT-23	LINEAR TECH, LTC2935CTS8-2
Power Sources and Energy Storage Components				
56	1	BAT1	CR2032 COIN LI-ION BATTERY	ENERGIZER , CR2032VP
57	1	BAT2	COIN LI-ION BATTERY Lir2032	POWERSTREAM, Lir2032
58	2	BTH1, BTH2	BATTERY HOLDER COIN CELL 2032 SMD	WURTH, 79527141
59	1	C30	SUPERCAP, 15mF, –20%, +80%, 5.5V, SMD	AVX, BZ055B153ZSB
60	10	CO1-CO10	CAP, CHIP, X5R, 150µF, 20%, 6.3V, 1210	SAMSUNG, CL32A157MQVNNNE
Additional Demo Board Circuit Components				
61	0	C31 (OPT)	SUPERCAP, 85mF, 5.0V, 20mm × 18mm	CAP-XX, GA209F
62	0	C32, C33 (OPT)	CAP, CHIP, X5R, 0.1µF, 20%, 10V, 0402	WURTH, 885 012 105 010
63	0	D4-D7 (OPT)	DIODE, SCHOTTKY, 40V, 1A, SOD-123	DIODES INC, 1N5819HW-7-F
64	0	R87, R88 (OPT)	RES, CHIP, 7.5kΩ, 1/16W, 1%, 0402	VISHAY, CRCW04027K50FKED
Hardware: For Demo Board Only				
65	19	E1-E19	TURRET, 0.061 DIA	MILL-MAX, 2308-2
66	1	J1	2×10, 20-PIN, SMT RIGHT ANGLE SOCKET WITH KEY (PIN 14), 0.100"	SAMTEC, SMH-110-02-L-D-14
67	1	J2	2×6, 12-PIN, SMT RIGHT ANGLE SOCKET WITH KEY (PIN 5), 0.100"	SAMTEC, SMH-106-02-L-D-05
68	8	JP1-JP4, JP5-JP8	SMT HEADER, 2 PINS, 2mm	SAMTEC, TMM-102-01-F-S-SM
69	2	JP17	SMT HEADER, 6 TOTAL PINS, 2 ROWS, 2mm	WURTH, 621 006 219 21

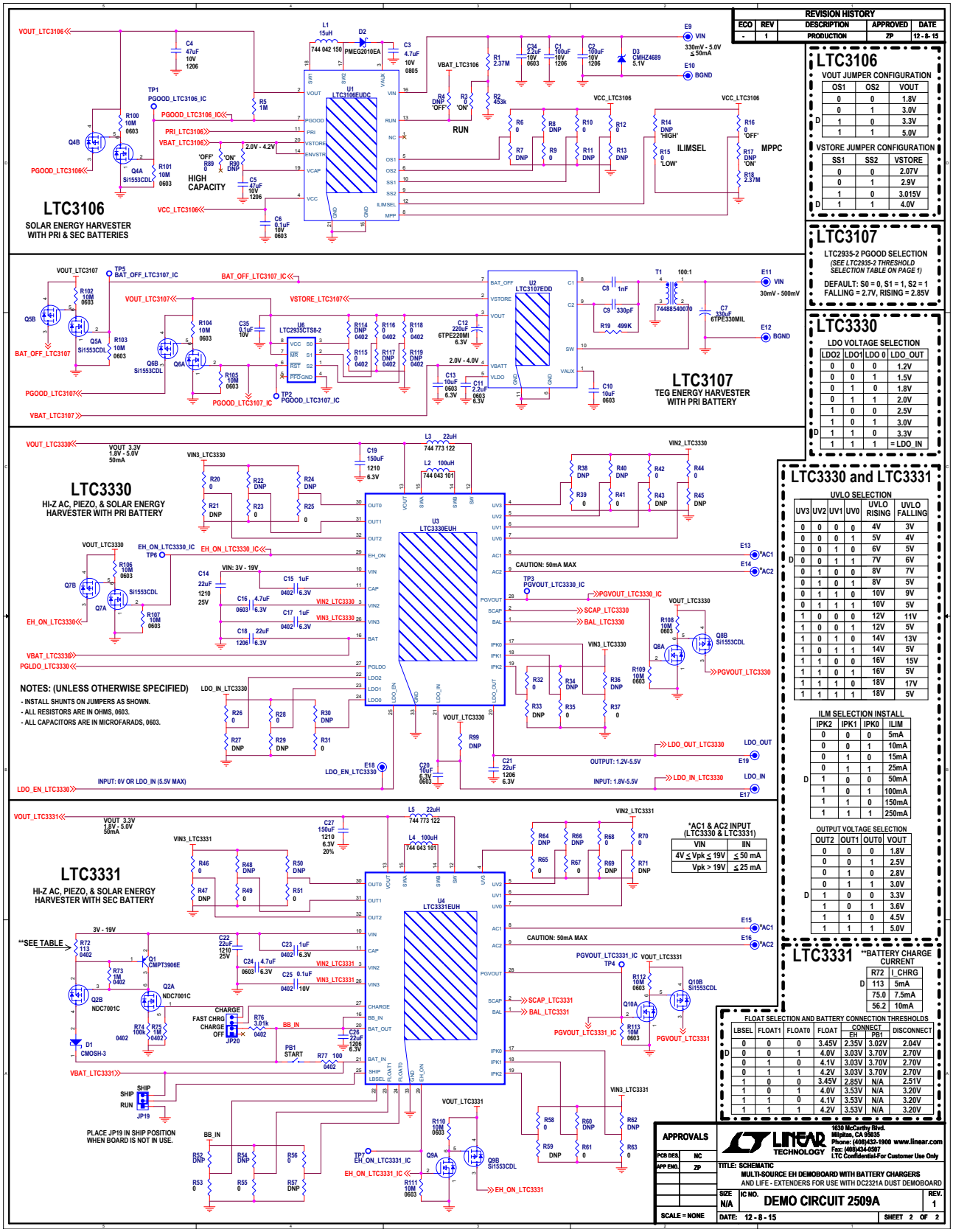
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
70	1	JP18	SMT HEADER, 8 TOTAL PINS, 2 ROWS, 2mm	WURTH, 621 008 219 21
71	1	JP19	HEADER, 3 PINS, 2mm	WURTH, 620 003 111 21
72	1	JP20	HEADER, 4 PINS, 2mm	WURTH, 620 004 111 21
73	1	JP21	HEADER, 4 TOTAL PINS, 2 ROWS, 2mm	WURTH, 620 004 211 21
74	7	JP3, JP7, JP17B, JP18C, JP19, JP20, JP21A	SHUNT 2MM	WURTH, 608 002 134 21
75	1	PB1	SWITCH TACTILE, SPST-NO, 0.05A 12V	WURTH, 434111025826
76	34	R3, R6, R9, R10, R12, R15, R16, R20, R23, R25, R26, R28, R31, R32, R35, R37, R39, R41, R42, R44, R46, R49, R51, R53, R55, R56, R58, R61, R63, R65, R67, R68, R70, R89	RES, CHIP, 0Ω, 0603	VISHAY, CRCW06030000Z0EA
77	0	R4, R7, R8, R11, R13, R14, R17, R21, R22, R24, R27, R29, R30, R33, R34, R36, R38, R40, R43, R45, R47, R48, R50, R52, R54, R57, R59, R60, R62, R64, R66, R69, R71, R90, R99 (OPT)	RES, CHIP, 0Ω, 0603	VISHAY, CRCW06030000Z0EA
78	0	R78, R79, R81, R83, R85, R86, R96, R97, R98, R114, R117, R119 (OPT)	RES, CHIP, 0Ω, 0402	VISHAY, CRCW04020000Z0ED
79	9	R80, R82, R84, R93, R94, R95, R115, R116, R118	RES, CHIP, 0Ω, 0402	VISHAY, CRCW04020000Z0ED
80	3	SW1, SW4, SW7	DP3T SLIDE SWITCH, 12mm × 3.5mm, 0.2A 12VDC	COPAL, CL-SB-23A-02T
81	1	SW2	4PDT SLIDE SWITCH, 16.5mm × 7mm, 0.1A 30VDC	ALPS, SSSF040800
82	1		DPDT SLIDE SWITCH, 8.5mm × 3.5mm, 0.2A 12VDC	COPAL, CL-SB-22A-01T
83	0.001	–	ELECTRICAL TAPE, 3/4" × 1/2"	3M, 33+ SUPER (3/4" × 66')
84	4	STANDOFF ×6 (OPT)	STANDOFF, HEX .625"L, 4-40, THR NYLON	KEYSTONE, 1902F
85	4	SCREW ×6 (OPT)	SCREW, MACH, PHIL, 4-40, .250 IN, NYLON	B&F FASTENER SUPPLY, NY PMS 440 0025 PH
86	1	–	FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 2509A
87	1	–	STENCIL - TOP	STENCIL #2590A-TOP
88	1	–	STENCIL - BOTTOM	STENCIL #2509A-BOTTOM
Skipped Reference Designators (to Match DC2344A)				
89	0	C29 (DOES NOT EXIST)	–	–
90	0	JP9-JP16 (DOES NOT EXIST)	–	–
91	0	SW3, SW5, SW6 (DOES NOT EXIST)	–	–

SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM



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