SL2 ICS53

Wafer addendum

Rev. 3.0 — 21 March 2007 | Product data sheet
135830 | PUBLIC

1. General description

This specification describes the electrical, physical and dimensional properties of Au-bumped sawn wafers on FFC of I•CODE SLI-S Label ICs on an NXP C075EE process and is the base for delivery of tested I•CODE SLI-S Label ICs.

2. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Ordering Code
SL2 ICS5301EW/V7		bumped sawn wafer on UV-tape	9352 837 46005

3. Mechanical specification

3.1 Wafer

- Diameter: 8”
- Thickness: 150 µm ± 15 µm

3.2 Wafer backside

- Material: Si
- Treatment: ground + stress releave
- Roughness: R_a max. 0.5 µm

  R_t max. 5 µm

3.3 Chip dimensions

- Chip size: 940 x 900µm^2
- Scribe lines: 50 / 50 µm

3.4 Passivation

- Type: sandwich structure
- Material: PSG / Nitride (on top)
- Thickness: 500 nm / 600 nm

founded by Philips

3.5 Au bump

- Bump material: > 99.9 % pure Au
- Bump hardness: 35 – 80 HV 0.005
- Bump shear strength: > 70 MPa
- Bump height: 18 μm
- Bump height uniformity:
  - within a die: ± 2 μm
  - within a wafer: ± 3 μm
  - wafer to wafer: ± 4 μm
- Bump flatness: ± 1.5 μm
- Bump size:
  - LA, LB: 60 x 60 $μm^2$
  - VSS[1], TEST[1]: 60 x 60 $μm^2$
- Bump size variation: ± 5 μm
- Under bump metallization: sputtered TiW

1.Pads VSS and TEST are disconnected when wafer is sawn.

© NXP B.V. 2007. All rights reserved.

3.6 Reference die definition (SECS II Wafer map format)

- Physical appearance: no chip structure, full die size
- Local coordinates: x=-67, y= -20

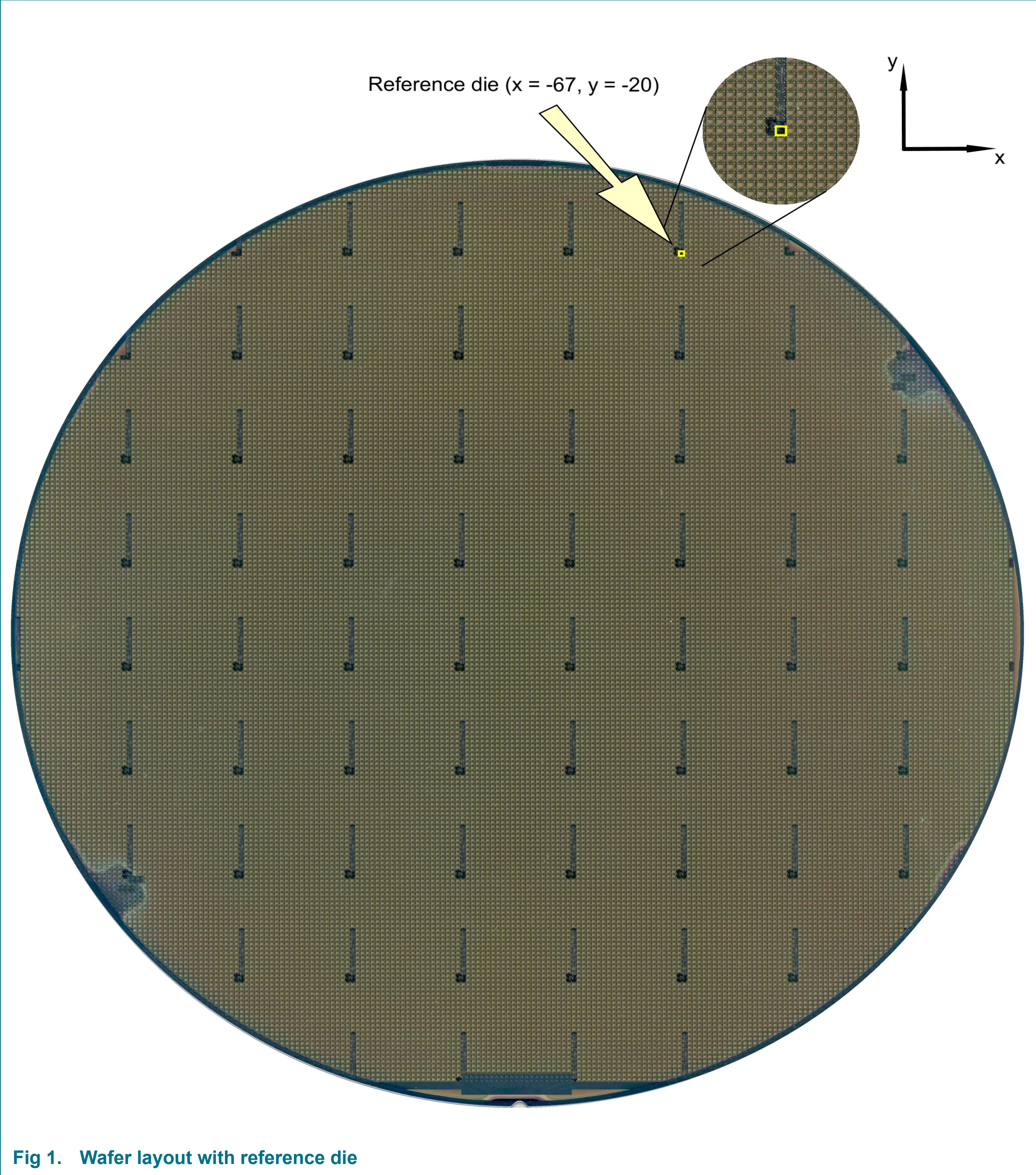

Fig 1. Wafer layout with reference die

© NXP B.V. 2007. All rights reserved.

4. Fail die identification

4.1 Fail die identification

No inkdots are applied to the wafer.

Electronic wafer mapping (SECS II format) covers the electrical test results and additionally the results of mechanical/visual inspection.

4.2 Wafer mapping

Wafer mapping for failed die information is available on floppy-disk.

Format: SECS II format

© NXP B.V. 2007. All rights reserved.

5. Limiting values

Table 2. Limiting values[1][2]

Absolute Maximum Ratings

Symbol	Parameter		Min	Type	Max	Unit
T_{STOR}	Storage temperature range		-55		+140	°C
Tj	Junction temperature		-55		+140	°C
V_{ESD}	Electrostatic discharge voltage	[3]			±2	kV_{peak}
$I_{max\ LA\text{-}LB}$	Maximum input peak current				±60	mA_{peak}
T_{jop}	Operating junction temperature		-25		+85	°C
$I_{LA\text{-}LB}$	Input current	[4]			30	mA_{rms}

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the Operating Conditions and Electrical Characteristics section of this specification is not implied.

[2] This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.

[3] MIL-STD-883D, Method 3015.7, Human Body Model

[4] The voltage between LA and LB is limited by the on-chip voltage limitation circuitry (corresponding to parameter $I_{LA\text{-}LB}$)

© NXP B.V. 2007. All rights reserved.

6. Characteristics

6.1 Electrical characteristics

T_{op}= -25 to 85° C

Table 3. Characteristics [1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{LA-LB}	Minimum Supply Voltage for READ/WRITE				2.5	2.7	V_{rms}
f_{op}	Operating Frequency		[2]	13.553	13.560	13.567	MHz
C_{res}	Input Capacitance between LA – LB	$V_{LA-LB} = 2\ V_{rms}$	[3]	22.3	23.5	24.7	pF
P_{min}	Minimum Operating Supply Power		[4]		280		µW
m	Modulation of RF Voltage for Demodulator Response	$m = \frac{V_{max} - V_{min}}{V_{max} + V_{min}}$	[5]				%
tP_{sm}	Modulation Pulse Length of RF Voltage		[5]				µs
tD	Demodulator Response Time	m ≥ 10 %, 100 %	[5]				µs
Rmod	Load Modulation		[5]				Ω
t_{ret}	EEPROM Data Retention	$T_{amb} \leq 55$ °C		10			Years
n_{write}	EEPROM Write Endurance			100000			Cycles

[1] Typical ratings are not guaranteed. These values listed are at room temperature.

[2] Bandwidth limitation (±7 kHz) according to ISM band regulations.

[3] Measured with an HP4285A LCR meter at 13.56 MHz

[4] Including losses in resonant capacitor and rectifier

[5] refer to ISO/IEC 15693-2 and 15693-3 including pulse shapes and tolerances; proper coil design assumed

© NXP B.V. 2007. All rights reserved.

7. Chip orientation and bond pad locations

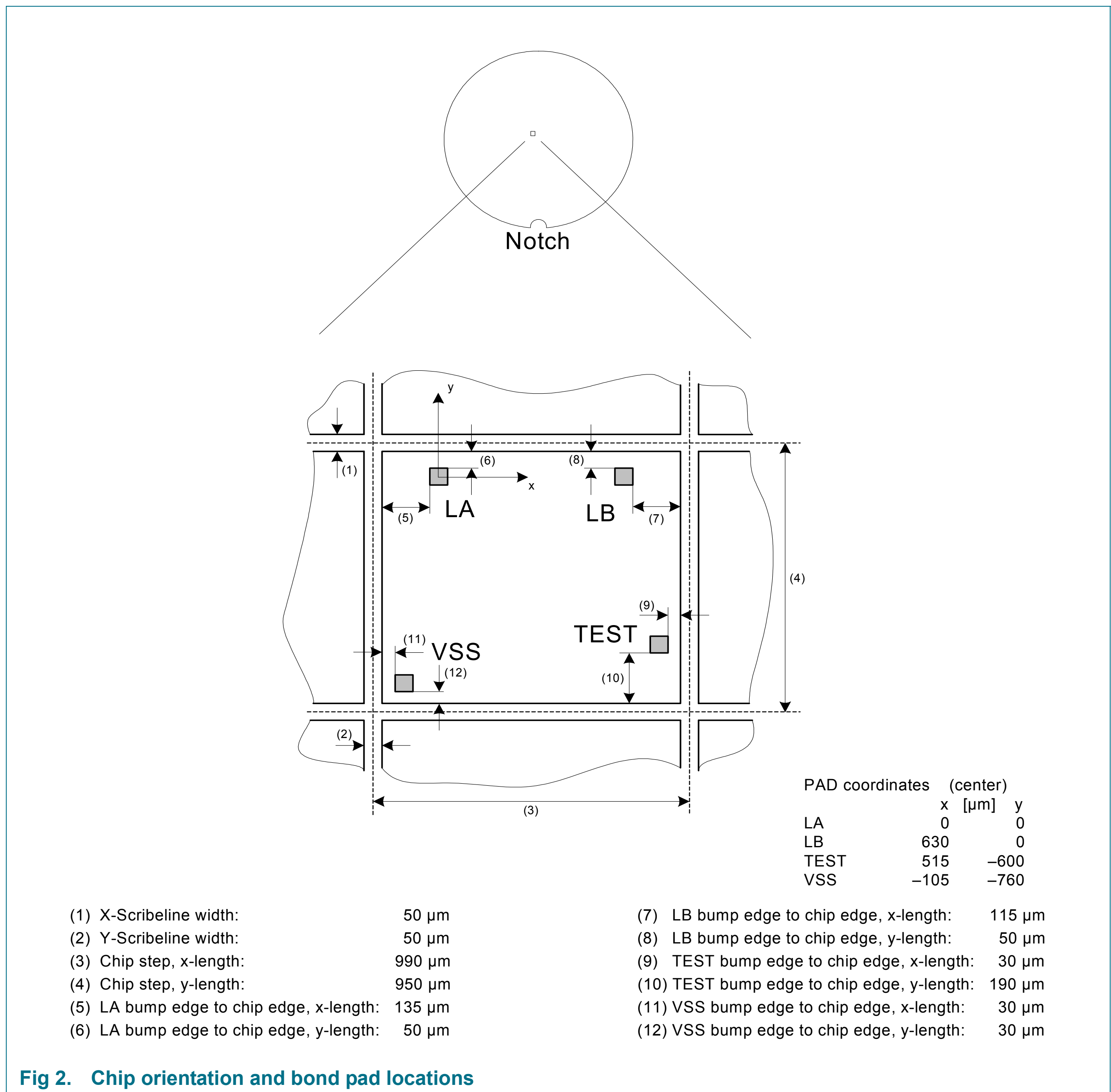

Fig 2. Chip orientation and bond pad locations

8. Final wafertest specification

- Minimum yield per wafer: 30 % of 29941 potential good dies.
- Minimum yield per lot: 30 %

© NXP B.V. 2007. All rights reserved.

9. References

- Data sheet ’General specification for 8” wafers on UV-tape’
- Data sheet ’General quality specification’
- Application note ’SECS II wafer map format’
- Data sheet ’I•CODE SLI-S/I•CODE SLI-S HC, Functional Specification’
- Application note ’I•CODE coil design guide’

© NXP B.V. 2007. All rights reserved.

10. Revision history

Table 4. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
135830	21 March 2007	Product data sheet		Revision 3.0
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name.			

© NXP B.V. 2007. All rights reserved.

11. Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

11.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

11.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of a NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer’s own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

11.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

12. Contact information

For additional information, please visit: **http://www.nxp.com**

For sales office addresses, send an email to: **salesaddresses@nxp.com**

© NXP B.V. 2007. All rights reserved.

13. Tables

Table 1. Ordering information 1
Table 2. Limiting values[1][2] 5
Table 3. Characteristics [1] 6
Table 4.Revision history 9

14. Figures

Fig 1. Wafer layout with reference die 3
Fig 2.Chip orientation and bond pad locations7

15. Contents

1 General description 1
2 Ordering information 1
3 Mechanical specification 1
3.1 Wafer 1
3.2 Wafer backside 1
3.3 Chip dimensions 1
3.4 Passivation 1
3.5 Au bump 2
3.6 Reference die definition (SECS II Wafer map format) 3
4 Fail die identification 4
4.1 Fail die identification 4
4.2 Wafer mapping 4
5 Limiting values 5
6 Characteristics 6
6.1 Electrical characteristics 6
7 Chip orientation and bond pad locations 7
8 Final wafertest specification 7
9 References 8
10 Revision history 9
11 Legal information 10
11.1 Data sheet status 10
11.2 Definitions 10
11.3 Disclaimers 10
11.4 Trademarks 10
12 Contact information 10
13 Tables 11
14 Figures 11
15 Contents 11

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2007. All rights reserved.

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 21 March 2007
Document identifier: 135830