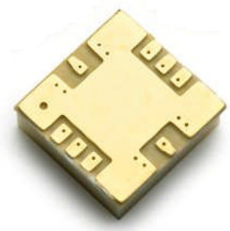
AMMP-5024

30kHz – 40 GHz Traveling Wave Amplifier

Data Sheet



Description

Avago Technologies' AMMP-5024 is a broadband PHEMT GaAs MMIC TWA designed for medium output power and high gain over the full 30 KHz to 40 GHz frequency range. The design employs a 9-stage, cascade-connected FET structure to ensure flat gain and power as well as uniform group delay. E-beam lithography is used to produce uniform gate lengths of 0.15um and MBE technology assures precise semiconductor layer control.

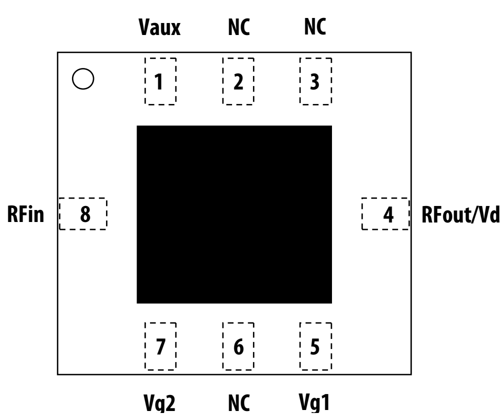
Features

- Surface Mount Package 5.0 x 5.0 x 2.0 mm
- Wide Frequency Range 30kHz – 40GHz
- High Gain: 14.8 dB Typical @ 22GHz
- Output P1dB: 22 dBm Typical @ 22GHz
- 50 Ohm Input and Output Match

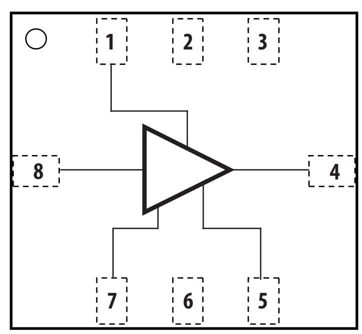
Applications [1]

- Broadband Test and Measurement Applications

Package Diagram



Functional Block Diagram



Pin	Function
1	V_{aux}
2	Not Used
3	Not Used
4	RF_{out} / Vd
5	V_{g1}
6	Not Used
7	V_{g2}
8	RF_{in}

Attention: Observe precautions for handling electrostatic sensitive devices.
ESD Machine Model (Class A): 40V
ESD Human Body Model (Class 0): 150V
Refer to Avago Application Note A004R: Electrostatic Discharge Damage and Control.

Note: MSL Rating = Level 2A

Electrical Specifications

1. All tested parameters guaranteed with measurement accuracy ± 0.5 dB for gain.

Table 1. RF Electrical Characteristics (Freq=22GHz, Vd= 7.0V, Idq=200mA, TA= 25°C, Zin=Zo=50Ω)

Parameter	Min	Typ.	Max	Unit
Small-signal Gain, Gain	12.5	14.8	16.5	dB
Noise Figure, NF		4.6		dB
Output Power at 1dB Gain Compression, P1dB		22		dBm
Third Order Intercept Point; Δf=100MHz; Pin=-5dBm, OIP3		25		dBm
Input Return Loss, RLin		13		dB
Output Return Loss, RLout		14		dB
Reverse Isolation, Isolation		30		dB

Table 2. RF Electrical Characteristics (Freq=22GHz, Vd= 4.0V, Idq=160mA, TA= 25°C, Zin=Zo=50Ω)

Parameter	Min	Typ.	Max	Unit
Small-signal Gain, Gain		15		dB
Noise Figure, NF		4.6		dB
Output Power at 1dB Gain Compression, P1dB		19		dBm
Third Order Intercept Point; Δf=100MHz; Pin=-5dBm, OIP3		18.5		dBm
Input Return Loss, RLin		13		dB
Output Return Loss, RLout		14		dB
Reverse Isolation, Isolation		27		dB

Table 3. Recommended Operating Range

(Vd=7V, Vg2=open, Ta= 25°C, otherwise specified)

	Specifications				
Description	Min.	Typical	Max.	Unit	Comments
Drain Supply Voltage, Vd		7		V	
Total Drain Supply Current, Id		200		mA	Vg1 set for typical Id
First Gate Voltage, Vg1	-3.5	-3.0	-2.5	V	Vd=7V, Id=200mA
Saturated Drain Current, Idss		350		mA	Vg1=0V
First Gate Minimum Drain Current, Idsmin (Vg1)		80		mA	Vg1=-7V

Table 4. Thermal Properties

Parameter	Test Conditions	Value
Thermal Resistance, θjc		θjc = 16.2 °C/W

Note:
1. Channel-to-board Thermal Resistance is measured using QFI method.

Absolute Minimum and Maximum Ratings

Table 5. Minimum and Maximum Ratings

	Specifications			
Description	**Min.**	**Max.**	**Unit**	**Comments**
Drain Supply Voltage, Vd		10	V	
Drain Current, Id		380	mA	
First Gate Voltage, Vg1	-9.5	0	V	
First Gate Current, Ig1	-38	1	mA	
Second Gate Voltage, Vg2	-3.5	4	V	
Second Gate Current, Ig2	-20		mA	
RF Input Power, Pin		17	dBm	CW
Channel Temperature, Tch		+150	°C	
Storage Temperature, Tstg	-65	+150	°C	
Maximum Assembly Temperature, Tmax		+260	°C	20 second Maximum

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to this device. The absolute maximum ratings for DC and Power parameters were determined at an ambient temperature of 25°C unless noted otherwise.

Selected performance plots

These measurements are in 50Ω test environment at Vd = 7V, Id = 200mA, Vg2 = Open, TA = 25°C.

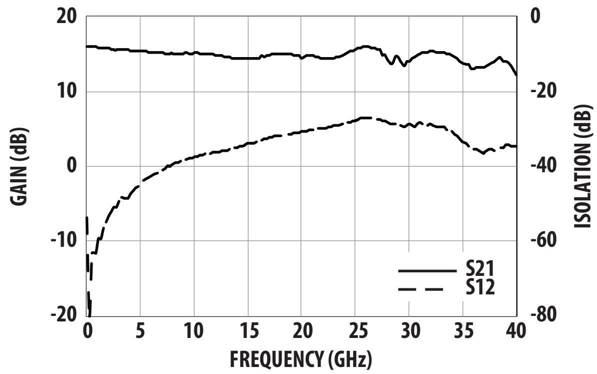


Figure 1. Gain and Reverse Isolation

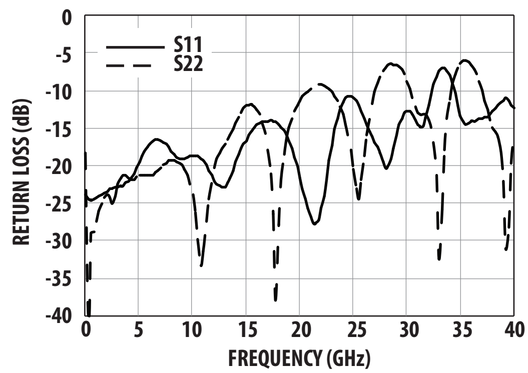


Figure 2. Return Loss (Input and Output).

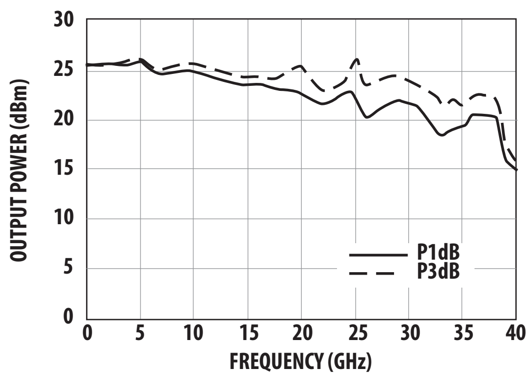


Figure 3. Output Power (P1dB and P3dB)

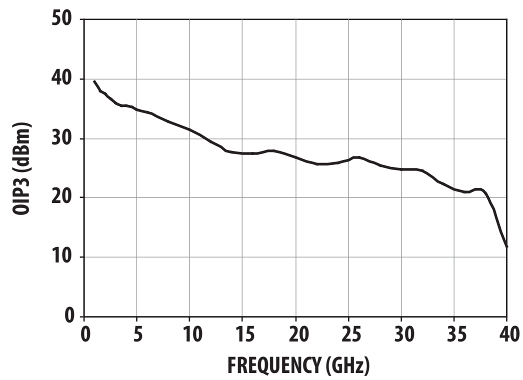


Figure 4. Output IP3

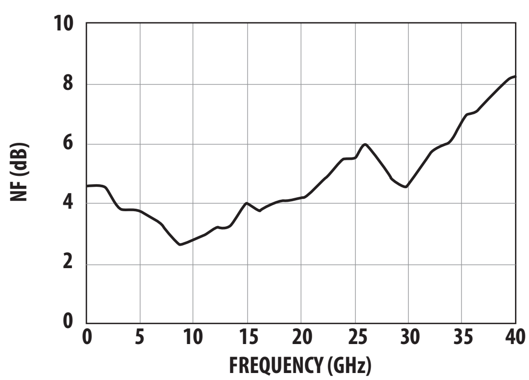


Figure 5. Npise Figure

These measurements are in 50Ω test environment at Vd = 4V, Id = 160mA, Vg2 = Open, TA = 25°C

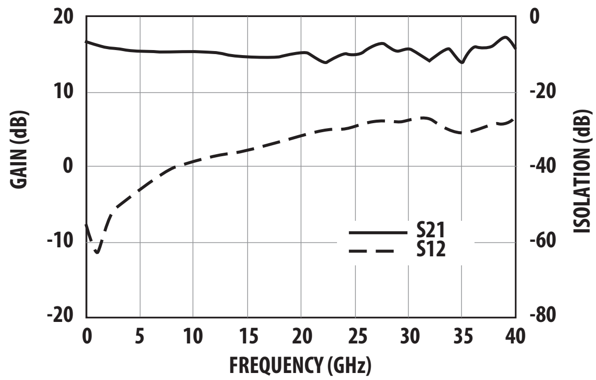


Figure 6. Gain and Reverse Isolation

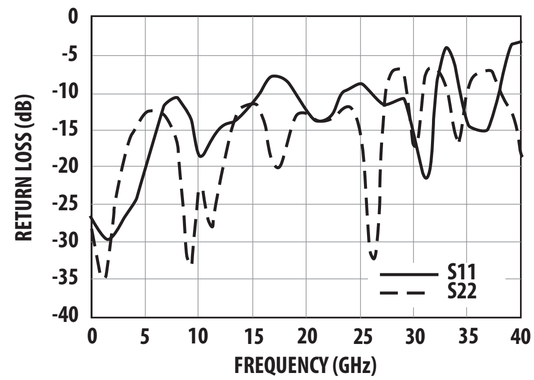


Figure 7. Return Loss (Input and Output).

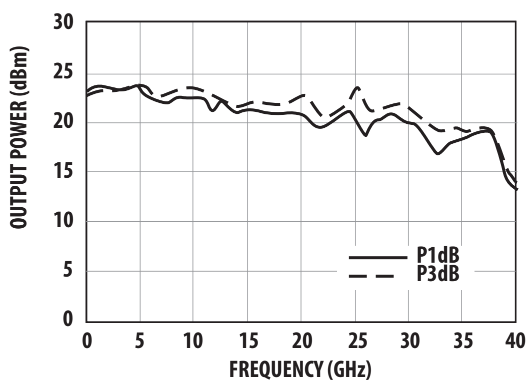


Figure 8. Output Power (P1dB and P3dB)

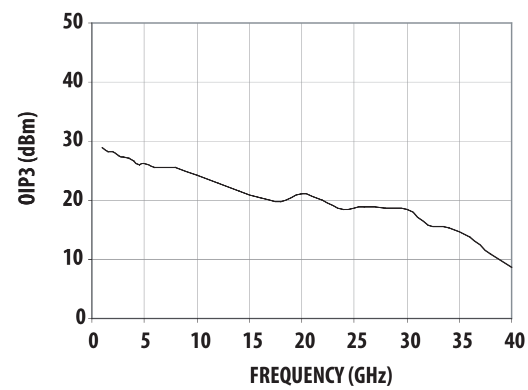


Figure 9. Output IP3

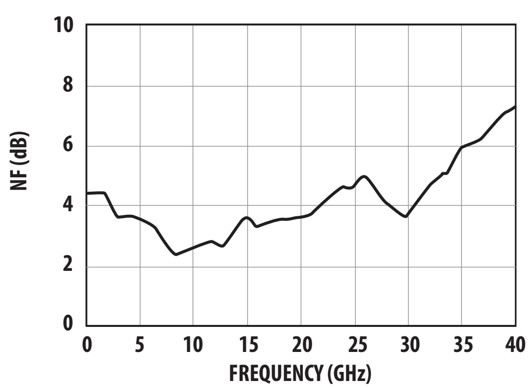


Figure 10. Noise Figure

Over Temperature Performance Plots

These measurements are in 50Ω test environment at Vd = 7V, Id = 200mA

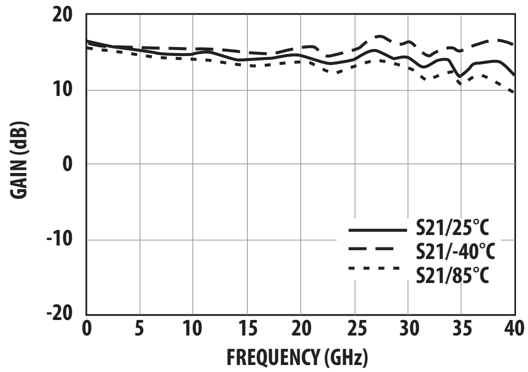


Figure 11. Gain and Temperature.

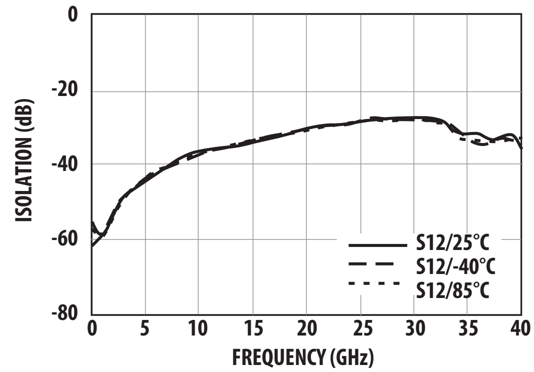


Figure 12. Isolation and Temperature.

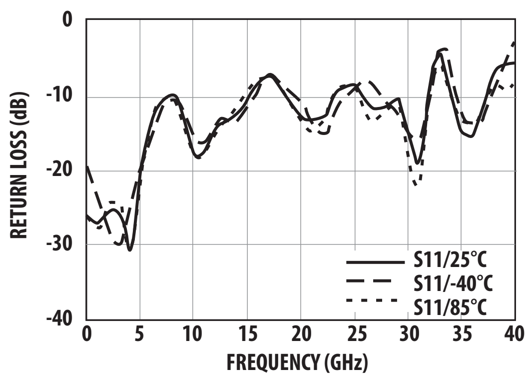


Figure 13. Input Return Loss and Temperature.

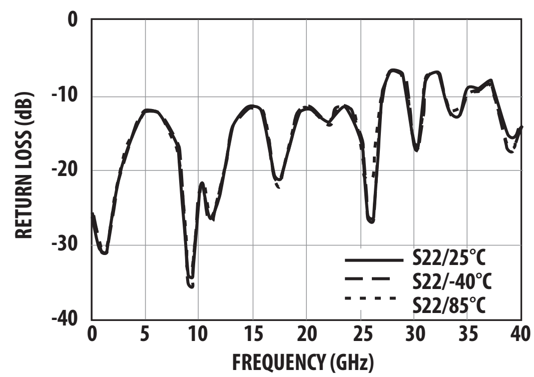


Figure 14. Output Return Loss and Temperature.

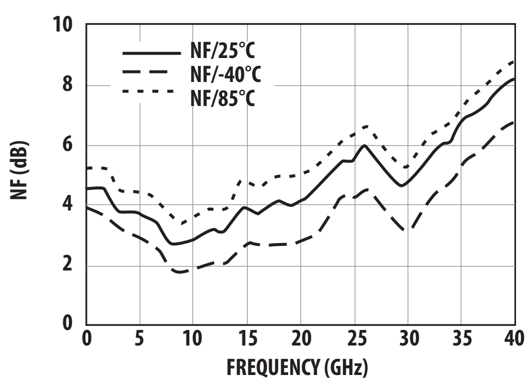


Figure 15. Noise Figure and Temperature.

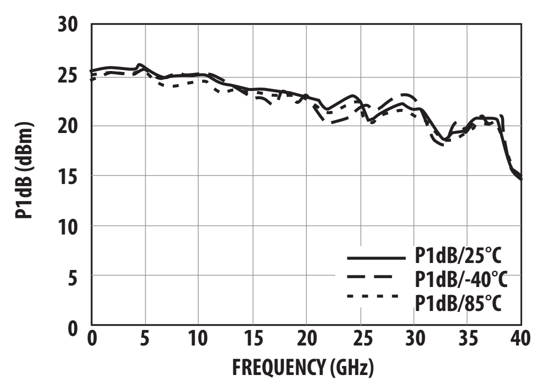


Figure 16. P1dB and Temperature.

Typical Scattering Parameters

Please refer to <http://www.avagotech.com> for typical scattering parameters data.

Biasing and Operation

AMMP-5024 is biased with a single positive drain supply (Vd) a negative gate supply (Vg1) and has a positive control gate supply (Vg2). For best overall performance the recommended bias condition for the AMMP-5024 is Vd =7V and Id = 200 mA. To achieve this drain current level, Vg1 is typically between –2.5 to –3.5V. Typically, DC current flow for Vg1 is –10 mA. Open circuit is the default setting for Vg2 when not utilizing gain control.

Using the simplest form of assembly, the device is capable of delivering flat gain over a 2–40 GHz range. However, this device is designed with DC coupled RF I/O ports, and operation may be extended to lower frequencies (<2 GHz) through the use of off-chip low-frequency extension circuitry and proper external biasing components. With low frequency bias extension it may be used in a variety of time domain applications (through 40 Gb/s).

When bypass capacitors are connected to the AUX pads, the low frequency limit is extended down to the corner frequency determined by the bypass capacitor and the combination of the on-chip 50 ohm load and small de-queing resistor. At this frequency the small signal gain will increase in magnitude and stay at this elevated level down to the point where the Caux bypass capacitor acts as an open circuit, effectively rolling off the gain completely. The low frequency limit can be approximated from the following equation:

$$f_{Caux} = \frac{1}{2\pi Caux\,(Ro + R_{DEQ})}$$

where:

Ro is the 50Ω gate or drain line termination resistor.

RDEQ is the small series dequeing resistor and 10Ω.

Caux is the capacitance of the bypass capacitor connected to the AUX Drain and AUX Gate pad in farads.

With the external bypass capacitors connected to the AUX gate and AUX drain pads, gain will show a slight increase between 1.0 and 1.5 GHz. This is due to a series combination of Caux and the on-chip resistance but is exaggerated by the parasitic inductance (Lc) of the bypass capacitor and the inductance of the bond wire (Ld).

Input and output RF ports are DC coupled; therefore, DC decoupling capacitors are required if there are DC paths. (Do not attempt to apply bias to these pads.)

Package Dimension, PCB Layout and Tape and Reel information

Please refer to Avago Technologies Application Note 5520, AMxP-xxxx production Assembly Process (Land Pattern A)

Ordering Information

Part Number	Devices per Container	Container
AMMP-5024-BLKG	10	Antistatic Bag
AMMP-5024-TR1G	100	7” Reel
AMMP-5024-TR2G	500	7” Reel

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