IXYS

Advance Technical Information

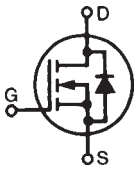
X-Class HiPERFET Power MOSFET

IXFP4N85XM

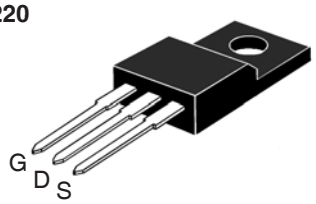
V_{DSS} = 850V
I_{D25} = 3.5A
$R_{DS(on)}$ ≤ 2.5Ω

(Electrically Isolated Tab)

N-Channel Enhancement Mode



OVERMOLDED TO-220



G = Gate D = Drain
S = Source

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	850	V
V_{DGR}	T_J = 25°C to 150°C, R_{GS} = 1MΩ	850	V
V_{GSS}	Continuous	±30	V
V_{GSM}	Transient	±40	V
I_{D25}	T_C = 25°C, Limited by T_{JM}	3.5	A
I_{DM}	T_C = 25°C, Pulse Width Limited by T_{JM}	10.0	A
I_A	T_C = 25°C	2	A
E_{AS}	T_C = 25°C	125	mJ
dv/dt	$I_S \le I_{DM}$, $V_{DD} \le V_{DSS}$, $T_J \le 150°C$	50	V/ns
P_D	T_C = 25°C	35	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	°C
M_d	Mounting Torque	1.13 / 10	Nm/lb.in
Weight		2.5	g

Features

- International Standard Package
- Plastic Overmolded Tab
- Low $R_{DS(ON)}$ and Q_G
- Avalanche Rated
- Low Package Inductance

Advantages

- High Power Density
- Easy to Mount
- Space Savings

Applications

- Switch-Mode and Resonant-Mode Power Supplies
- DC-DC Converters
- PFC Circuits
- AC and DC Motor Drives
- Robotics and Servo Controls

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{DSS}	V_{GS} = 0V, I_D = 250μA	850			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250μA	3.0		5.5	V
I_{GSS}	V_{GS} = ±30V, V_{DS} = 0V			±100	nA
I_{DSS}	$V_{DS} = V_{DSS}$, V_{GS} = 0V			5	μA
	T_J = 125°C			500	μA
$R_{DS(on)}$	V_{GS} = 10V, I_D = 2A, Note 1			2.5	Ω

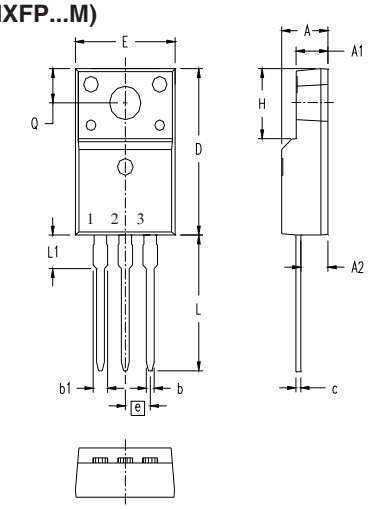
Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max	
g_{fs}	V_{DS} = 10V, I_D = 2A, Note 1	1.2	2.0		S
R_{Gi}	Gate Input Resistance		3		Ω
C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		247		pF
C_{oss}			305		pF
C_{rss}			5		pF
	Effective Output Capacitance				
$C_{o(er)}$	Energy related; V_{GS} = 0V, V_{DS} = 0.8 • V_{DSS}		27		pF
$C_{o(tr)}$	Time related; V_{GS} = 0V, V_{DS} = 0.8 • V_{DSS}		60		pF
$t_{d(on)}$	**Resistive Switching Times**		13		ns
t_r	V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 2A		27		ns
$t_{d(off)}$	R_G = 30Ω (External)		28		ns
t_f			20		ns
$Q_{g(on)}$	V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 2A		7.0		nC
Q_{gs}			2.3		nC
Q_{gd}			3.3		nC
R_{thJC}				3.57	°C/W
R_{thCS}			0.50		°C/W

Source-Drain Diode

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max	
I_S	V_{GS} = 0V			4	A
I_{SM}	Repetitive, pulse Width Limited by T_{JM}			16	A
V_{SD}	I_F = I_S, V_{GS} = 0V, Note 1			1.4	V
t_{rr}	I_F = 2A, -di/dt = 100A/μs		170		ns
Q_{RM}	V_R = 100V		770		nC
I_{RM}			9		A

Note 1. Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.

OVERMOLDED TO-220 (IXFP...M)



Terminals: 1 - Gate
2 - Drain
3 - Source

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.177	.193	4.50	4.90
A1	.092	.108	2.34	2.74
A2	.101	.117	2.56	2.96
b	.028	.035	0.70	0.90
b1	.050	.058	1.27	1.47
c	.018	.024	0.45	0.60
D	.617	.633	15.67	16.07
E	.392	.408	9.96	10.36
e	.100 BSC		2.54 BSC	
H	.255	.271	6.48	6.88
L	.499	.523	12.68	13.28
L1	.119	.135	3.03	3.43
ØP	.121	.129	3.08	3.28
Q	.126	.134	3.20	3.40

ADVANCE TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

Fig. 1. Output Characteristics @ T_J = 25ºC

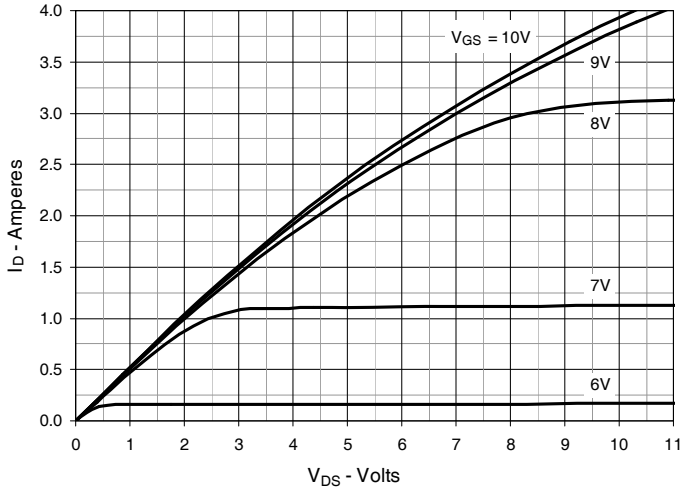


Fig. 2. Extended Output Characteristics @ T_J = 25ºC

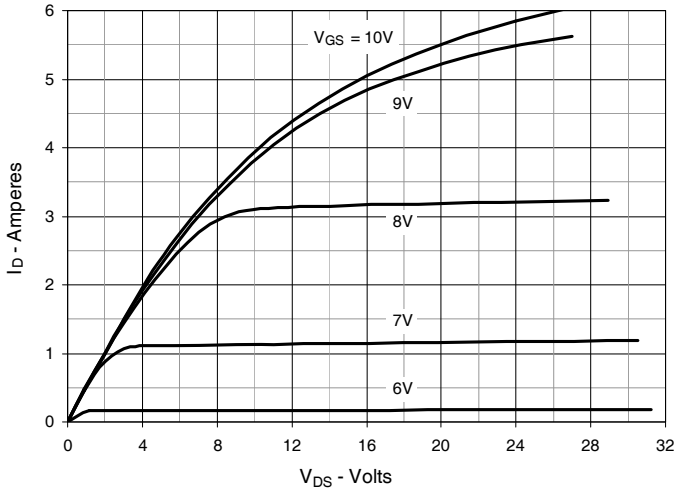


Fig. 3. Output Characteristics @ T_J = 125ºC

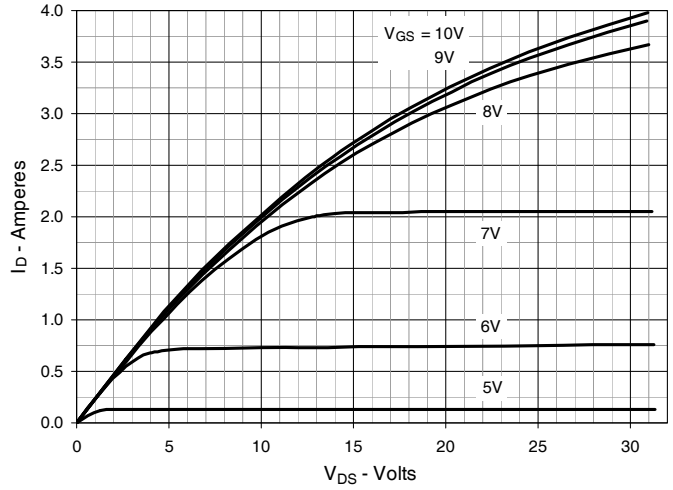


Fig. 4. $R_{DS(on)}$ Normalized to I_D = 2A Value vs. Junction Temperature

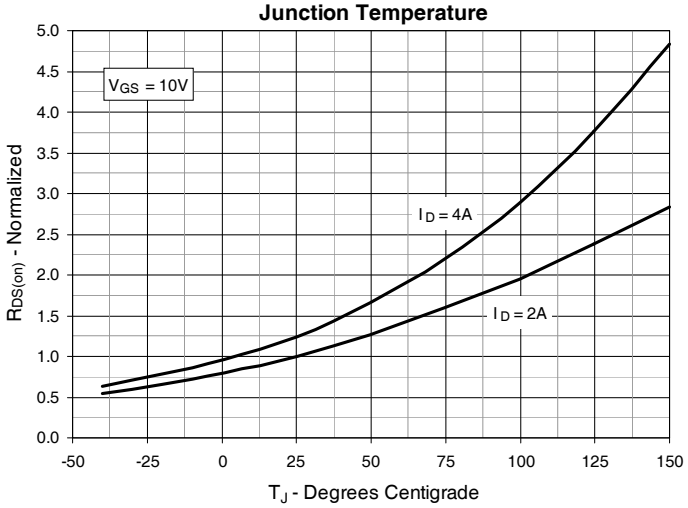


Fig. 5. $R_{DS(on)}$ Normalized to I_D = 2A Value vs. Drain Current

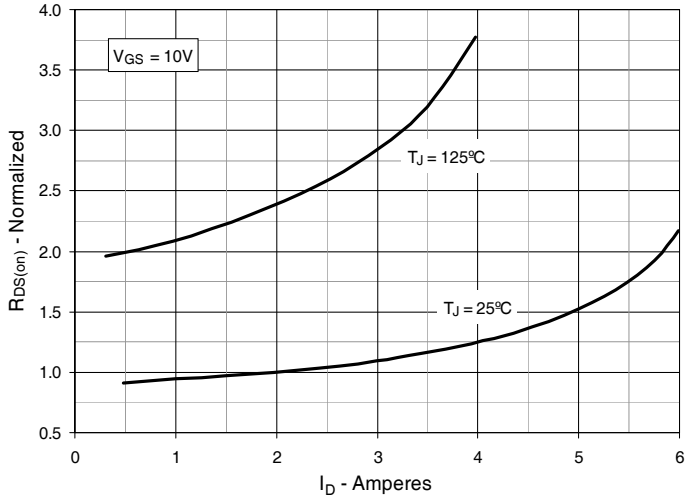


Fig. 6. Input Admittance

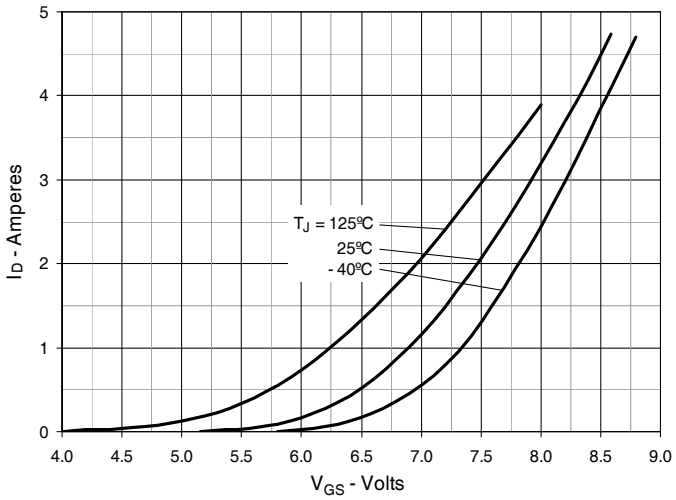


Fig. 7. Transconductance

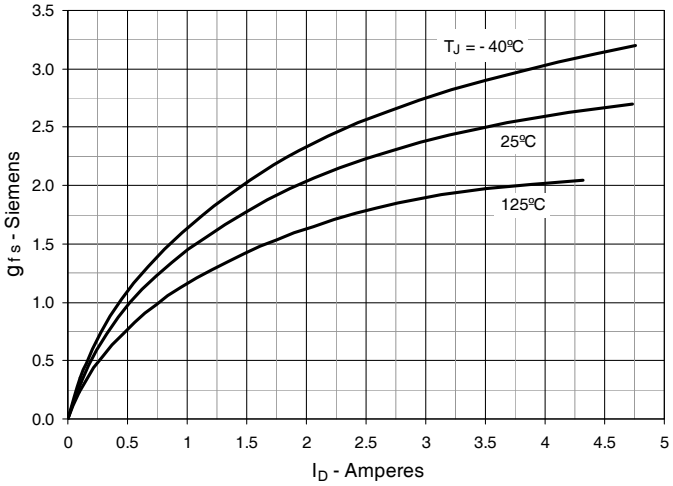


Fig. 8. Forward Voltage Drop of Intrinsic Diode

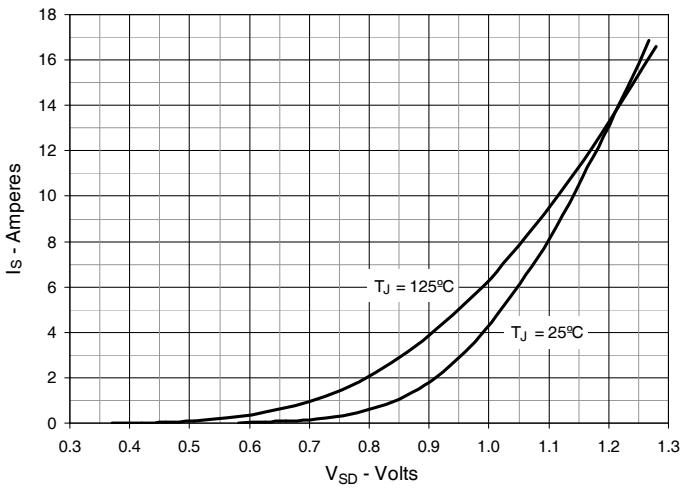


Fig. 8. Gate Charge

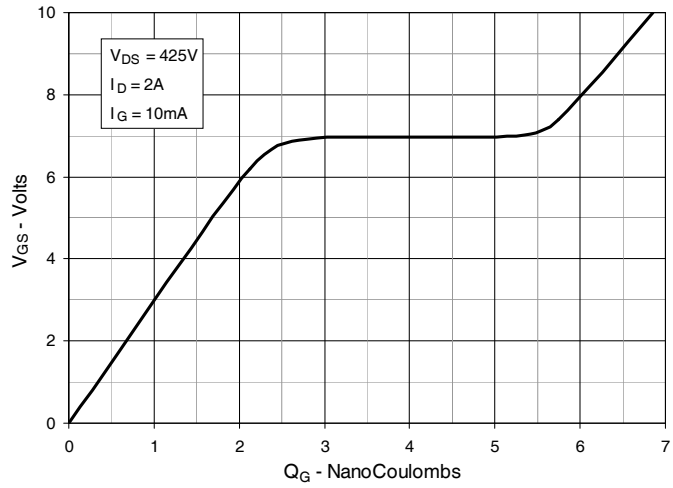


Fig. 9. Capacitance

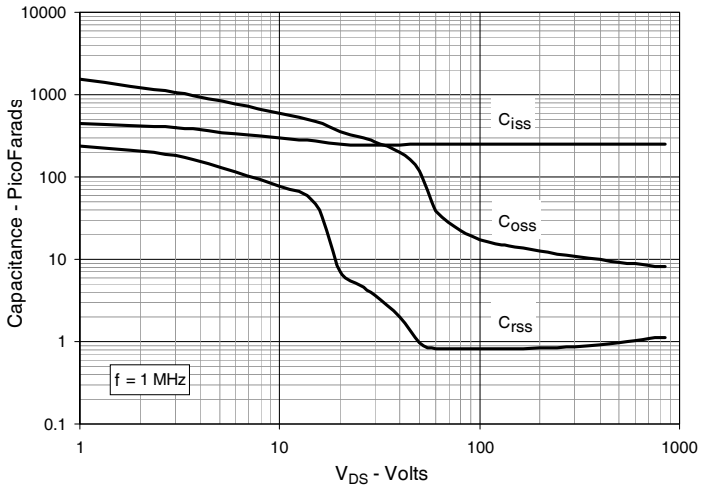


Fig. 11. Output Capacitance Stored Energy

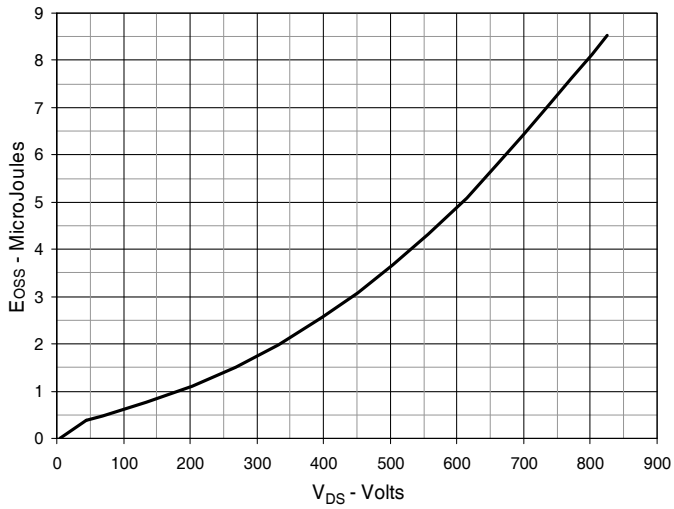


Fig. 12. Forward-Bias Safe Operating Area

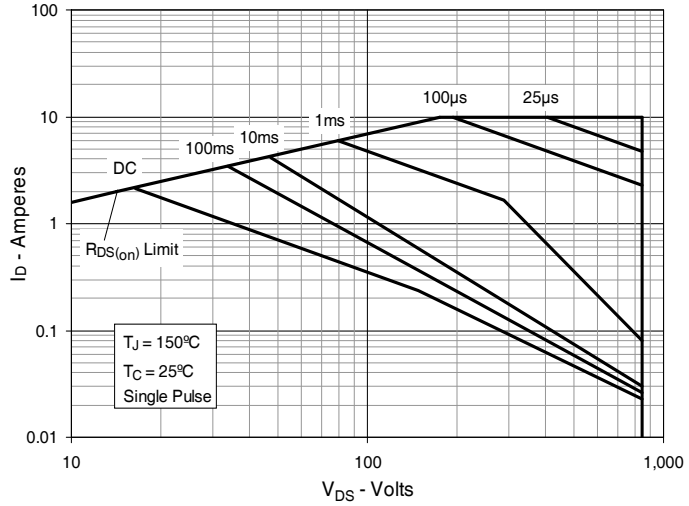


Fig. 13. Maximum Transient Thermal Impedance