MSSP MODULE

MSSP Module Silicon/Data Sheet Errata

The PICmicro® microcontrollers you have received all exhibit anomalous behavior in their Master SSP (MSSP) modules, as described in this document. They otherwise conform functionally to the descriptions provided in their respective Device Data Sheets and Reference Manuals, as amended by silicon release errata for particular devices.

Users are encouraged to review the latest Device Data Sheets and errata available for additional information concerning an individual device. These documents may be obtained directly from the Microchip corporate web site, at **www.microchip.com**.

These issues are expected to be resolved in future silicon revisions of the designated parts.

Silicon issues 1 and 2 affect all silicon revisions of the following devices:

- PIC16C717
- PIC16C770
- PIC16C771
- PIC16C773
- PIC16C774
- PIC16F737
- PIC16F747
- PIC16F767
- PIC16F777
- PIC16F872
- PIC16F873
- PIC16F873A
- PIC16F874
- PIC16F874A
- PIC16F876
- PIC16F876A
- PIC16F877
- PIC16F877A
- PIC17C752
- PIC17C756
- PIC17C756A
- PIC17C762
- PIC17C766
- PIC18C242
- PIC18C252
- PIC18C442
- PIC18C452
- PIC18C601
- PIC18C801
- PIC18C658
- PIC18C858
- PIC18F2220
- PIC18F2320
- PIC18F242
- PIC18F2439
- PIC18F248
- PIC18F252
- PIC18F2539
- PIC18F258
- PIC18F4220
- PIC18F4320
- PIC18F442
- PIC18F4439
- PIC18F448
- PIC18F452
- PIC18F4539
- PIC18F458
- PIC18F6520
- PIC18F6525
- PIC17F6585
- PIC18F6620
- PIC18F6621
- PIC18F6680
- PIC18F6720
- PIC18F8520
- PIC18F8525
- PIC18F8585
- PIC18F8620
- PIC18F8621
- PIC18F8680
- PIC18F8720

1. Module: I^2C™ (Slave Mode)

In its current implementation, the module may fail to correctly recognize certain Repeated Start conditions. For this discussion, a Repeated Start is defined as a Start condition presented to the bus after an initial valid Start condition has been recognized and the Start status bit (SSPSTAT<3>) has been set and before a valid Stop condition is received.

If a Repeated Start is not recognized, a loss of synchronization between the Master and Slave may occur; the condition may continue until the module is reset. A NACK condition, generated by the Slave for any reason, will not reset the module.

This failure has been observed only under two circumstances:

- A Repeated Start occurs within the frame of a data or address byte. The unexpected Start condition may be erroneously interpreted as a data bit, provided that the required conditions for setup and hold times are met.
- A Repeated Start condition occurs between two back-to-back slave address matches in the same Slave, with the $R/\overline{W}$ bit set to Read (= `1`) in both cases. (This circumstance is regarded as being unlikely in normal operation.)

Work around

A time-out routine should be used to monitor the module's operation. The timer is enabled upon the receipt of a valid Start condition; if a time-out occurs, the module is reset. The length of the time-out period will vary from application to application and will need to be determined by the user.

Two methods are suggested to reset the module:

1. Change the mode of the module to something other than the desired mode by changing the settings of bits, SSPM3:SSPM0 (SSPCON1<3:0>); then, change the bits back to the desired configuration.
2. Disable the module by clearing the SSPEN bit (SSPCON1<5>); then, re-enable the module by setting the bit.

Other methods may be available.

Clarifications/Corrections to the Data Sheets

Note: Items 1-3 apply to the Data Sheets for the following devices:

- PIC16C717/770/771 (DS41120B)
- PIC16C773/774 (DS30275A)
- PIC16F872 (DS30221B)
- PIC16F873/874/876/877 (DS30292C)
- PIC16F873A/874A/876A/877A (DS39582B)
- PIC17C752/756A/762/766 (DS30289B)
- PIC18C242/252/442/452 (DS39026C)
- PIC18C601/801 (DS39541A)
- PIC18C658/858 (DS30475A)
- PIC18F242/252/442/452 (DS39564B)
- PIC18F2220/2320/4220/4320 (DS39599C)
- PIC18F2439/2539/4439/4539 (DS30485A)
- PIC18F6520/6620/6720/8520/8620/8720 (DS39609B)
- PIC18F6585/6680/8585/8680 (DS30491C)

1. Module: MSSP (SPI Mode)

The description of the operation of the CKE bit (SSPSTAT<6>) is clarified. Please substitute the description in Register 1, below, for all occurrences of the existing text for the SSPSTAT register, bit 6 (new text in **bold**).

Note: This text refers only to the operation of the CKE bit in SPI mode; its operation in I^2C mode is unchanged. For those data sheets that describe the SSPSTAT register in separate locations for SPI and I^2C modes, this description applies only to the register titled “SSPSTAT Register (SPI Mode)”.

2. Module: MSSP (SPI Slave Mode)

The description of the operation of SPI Slave mode is clarified as follows: the state of the clock line (SCK) must match the polarity for the Idle state before enabling the module.

The subsection of the “MSSP Module” chapter, entitled “Slave Mode” (Subsection 3.6 in the majority of data sheets, Subsection 3.5 in others), is amended by adding the following paragraph to the end of the existing text:

“Before enabling the module in SPI Slave mode, the clock line must match the proper Idle state. The clock line can be observed by reading the SCK pin. The Idle state is determined by the CKP bit (SSPCON1<4>) .”

REGISTER 1: SSPSTAT: MSSP STATUS REGISTER (EXCERPT)

bit 6 **CKE:** SPI Clock Edge Select bit

`1` = **Transmit occurs on transition from active to Idle clock state**
`0` = **Transmit occurs on transition from Idle to active clock state**

Note: Polarity of clock state is set by the CKP bit (SSPCON1<4>).

3. Module: MSSP (I^2C Mode)

The table for the I^2C Baud Rate Generator clock rates is revised. Replace the I^2C Clock Rate Table with the following:

TABLE 1: I^2C™ CLOCK RATE w/BRG

F_{OSC}	F_{CY}	F_{CY} * 2	BRG Value	F_{SCL} (2 Rollovers of BRG)
40 MHz	10 MHz	20 MHz	18h	400 kHz(1)
40 MHz	10 MHz	20 MHz	1Fh	312.5 kHz
40 MHz	10 MHz	20 MHz	63h	100 kHz
16 MHz	4 MHz	8 MHz	09h	400 kHz(1)
16 MHz	4 MHz	8 MHz	0Ch	308 kHz
16 MHz	4 MHz	8 MHz	27h	100 kHz
4 MHz	1 MHz	2 MHz	02h	333 kHz(1)
4 MHz	1 MHz	2 MHz	09h	100 kHz
4 MHz	1 MHz	2 MHz	00h	1 MHz(1)

Note 1: The I^2C™ interface does not conform to the 400 kHz I^2C specification (which applies to rates greater than 100 kHz) in all details, but may be used with care where higher rates are required by the application.

4. Module: MSSP (I^{2}C Mode)

> **Note:** Item 4 applies to the Data Sheets for the following devices:
> - PIC16C717/770/771 (DS41120B)
> - PIC16C773/774 (DS30275A)
> - PIC16F872 (DS30221B)
> - PIC16F873/874/876/877 (DS30292C)
> - PIC16F873A/874A/876A/877A (DS39582B)

The description of the I^{2}C pins related to the TRIS bits is clarified. To ensure proper communication of the I^{2}C Slave mode, the TRIS bits (TRISx [SDA, SCL]) corresponding to the I^{2}C pins must be set to '1'. If any TRIS bits (TRISx<7:0>) of the port containing the I^{2}C pins (PORTx [SDA, SCL]) are changed in software during I^{2}C communication using a Read-Modify-Write instruction (BSF, BCF), then the I^{2}C mode may stop functioning properly and I^{2}C communication may suspend. Do not change any of the TRISx bits (TRIS bits of the port containing the I^{2}C pins) using the instruction BSF or BCF during I^{2}C communication. If it is absolutely necessary to change the TRISx bits during communication, the following method can be used:

```
MOVF    TRISC, W        ; Example for a 40-pin part such as the PIC16F877A
IORLW   0x18            ; Ensures <4:3> bits are '11'
ANDLW   B'11111001'     ; Sets <2:1> as output, but will not alter other bits
                        ; User can use their own logic here, such as IORLW, XORLW and ANDLW
MOVWF   TRISC
```

REVISION HISTORY

Revision A Document (7/2002):

Original version (I^2C Slave Issue)

Revision B Document (1/2003):

Clarification of original issue to include Restart conditions. Addition of data sheet clarification 1 (SPI Mode, CKE bit).

Revision C Document (3/2003):

Addition of data sheet clarification 2 (SPI Slave Mode, operation).

Revision D Document (9/2004):

Updated list of affected devices for silicon issue 1 (I^2C – Slave Mode) and 2 (MSSP – SPI, Slave Mode), removed silicon issue 3 (I^2C – Slave Mode) and added data sheet clarifications 3 and 4 (MSSP – I^2C Mode).

Revision E Document (7/2006):

Removed silicon issue 2 (MSSP – SPI, Slave Mode).

NOTES:

Note the following details of the code protection feature on Microchip devices:

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