Data Sheet | November 3, 2009 | FN6583.2

Negative Signal Swing, Sub-ohm, Dual SPDT with Click and Pop Elimination Single Supply Switch with Enable Pin

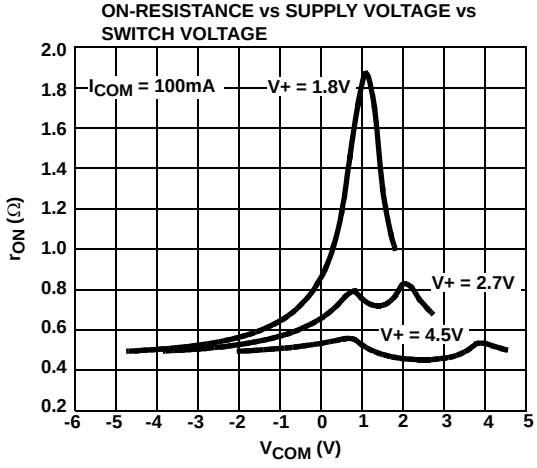
The Intersil ISL54065 device is a low ON-resistance, low voltage, bi-directional, dual single-pole/double-throw (SPDT) analog switch. It is designed to operate from a single +1.8V to +6.5V supply and pass signals that swing down to 6.5V below the positive supply rail. Targeted applications include battery powered equipment that benefit from low r_{ON} (0.56Ω), low power consumption (8nA) and fast switching speeds (t_{ON} = 55ns, t_{OFF} = 18ns). The digital inputs are 1.8V logic-compatible up to a +3V supply. The ISL54065 also features integrated circuitry to eliminate click and pop noise to an audio speaker.

The ISL54065 is offered in a small form factor package, alleviating board space limitations. It is available in a tiny 12 Ld 2.2x1.4mm µTQFN.

The ISL54065 is a committed dual single-pole/double-throw (SPDT) that consist of two normally open (NO) and two normally closed (NC) switches with independent logic control. This configuration can be used as a dual 2-to-1 multiplexer.

TABLE 1. FEATURES AT A GLANCE

	ISL54065
Number of Switches	2
SW	SPDT or 2-1 MUX
4.3V r_{ON}	0.65Ω
4.3V t_{ON}/t_{OFF}	43ns/23ns
2.7V r_{ON}	0.9Ω
2.7V t_{ON}/t_{OFF}	55ns/18ns
1.8V r_{ON}	1.8Ω
1.8V t_{ON}/t_{OFF}	145ns/28ns
Packages	12 Ld µTQFN



Features

- Pb-Free (RoHS Compliant)
- Single Supply Operation . . . . . .+1.8V to +6.5V
- Negative Signal Swing (Max 6.5V Below V+)
- Enable Pin to Disable All Switches
- Integrated Click and Pop Elimination Circuitry
- Click and Pop Circuitry Disable Pin
- ON-Resistance (r_{ON})
  - V+ = +4.5V 0.52Ω
  - V+ = +4.3V 0.65Ω
  - V+ = +2.7V 0.9Ω
  - V+ = +1.8V 1.8Ω
- r_{ON} Matching Between Channels 10mΩ
- r_{ON} Flatness Across Signal Range 0.33Ω
- Low THD+N @ 32Ω Load 0.02%
- Low Power Consumption @ 3V (P_D). 24nW
- Fast Switching Action (V+ = +4.3V)
  - t_{ON} 43ns
  - t_{OFF} 23ns
- ESD HBM Rating . . . . . .>6kV
- Guaranteed Break-Before-Make
- 1.8V Logic Compatible (+3V supply)
- Low I+ Current when V_{INH} is not at the V+ Rail
- Available in 12 Ld 2.2mm x 1.4mm µTQFN Package

Applications

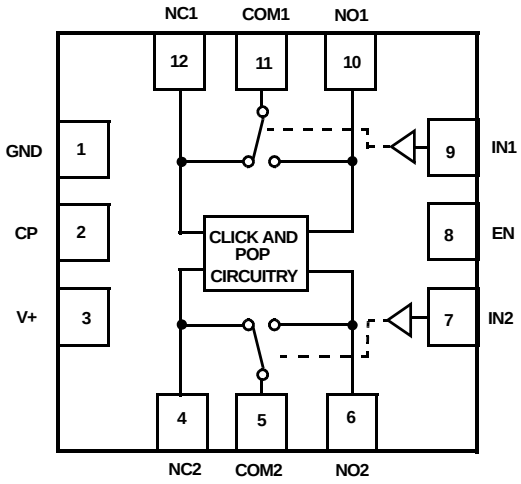
- Audio and Video Switching
- Battery powered, Handheld, and Portable Equipment
  - MP3 and Multimedia Players
  - Cellular/mobile Phones
  - Pagers
  - Laptops, Notebooks, Palmtops
- Portable Test and Measurement
- Medical Equipment

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Application Note AN557 “Recommended Test Procedures for Analog Switches”

Pinout (Note 1)

ISL54065
(12 LD µTQFN)
TOP VIEW



Pin Descriptions

PIN	FUNCTION
V+	Supply Voltage(+1.8V to +6.5V). Decouple V+ to ground by placing a 0.1µF capacitor at the V+ and GND supply lines as near as the IC as possible.
GND	Ground Connection
INx	Input Select Pin
EN	Switch Enable Pin
COMx	Analog Switch Common Pin
NOx	Analog Switch Normally Open Pin
NCx	Analog Switch Normally Closed Pin
CP	Click and Pop Circuitry Enable Pin

NOTE:

1. Switches Shown for EN = Logic “1” and INx = Logic “0”.

Truth Table

EN	IN1	IN2	NC1	NC2	NO1	NO2
0	X	X	OFF	OFF	OFF	OFF
1	0	0	ON	ON	OFF	OFF
1	0	1	ON	OFF	OFF	ON
1	1	0	OFF	ON	ON	OFF
1	1	1	OFF	OFF	ON	ON

NOTE: Logic “0” ≤0.5V. Logic “1” ≥1.4V with a 3V supply.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL54065IRUZ-T*	GG	-40 to +85	12 Ld Thin µTQFN (Tape and Reel)	L12.2.2x1.4A

*Please refer to TB347 for details on reel specifications.
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings

V+ to GND . . . . . -0.5 to 7.0V
Input Voltages
NOx, NCx (Note 2) . . . . . (V+ - 7V) to ((V+) + 0.5V)
INx, EN (Note 2) . . . . . -0.5 to ((V+) + 0.5V)
Output Voltages
COMx (Note 2) . . . . . (V+ - 7V) to ((V+) + 0.5V)
Continuous Current NOx, NCx, or COMx . . . . . ±300mA
Peak Current NOx, NCx, or COMx
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±500mA
ESD Rating:
Human Body Model . . . . . >6kV
Machine Model . . . . . >400V
Charged Device Model . . . . . >1.5kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)
12 Ld µTQFN Package (Note 3)	155

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . . -40°C to +85°C
Power Supply Range . . . . . +1.8V to +6.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

2. Signals on NCx, NOx, INx, EN, CP, or COMx exceeding V+ or GND by the specified amount are clamped by internal diodes. Limit forward diode current to maximum current ratings.
3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications - 5V Supply

Test Conditions: V+ = +4.5V to +5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, V_{EN} = V_{INH}, V_{CP} = V_{INL} (Note 4), unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 5, 6)	TYP	MAX (Notes 5, 6)	UNITS
ANALOG SWITCH CHARACTERISTICS						
ON-Resistance, r_{ON}	V+ = 4.5V, I_{COM} = 100mA, V_{NO} or V_{NC} = (V+ -6.5) to V+ (see Figure 5)	25	-	0.52	-	Ω
		Full	-	0.68	-	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V+ = 4.5V, I_{COM} = 100mA, V_{NO} or V_{NC} = Voltage at max r_{ON} (Note 8)	25	-	10	-	mΩ
		Full	-	13.1	-	mΩ
r_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 4.5V, I_{COM} = 100mA, V_{NO} or V_{NC} = (V+ -6.5) to V+ (Note 7)	25	-	0.11	-	Ω
		Full	-	0.14	-	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 5V, V_{COM} = -1.5V, 5V, V_{NO} or V_{NC} = 5V, -1.5V	25	-	-8.13	-	nA
		Full	-	-0.4	-	µA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 5V, V_{COM} = -1.5V, 5V, V_{NO} or V_{NC} = Float	25	-	-4.42	-	nA
		Full	-	-0.33	-	µA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 4.5V, V_{NO} or V_{NC} = 3.0V, R_L = 50Ω, C_L = 35pF (see Figure 1)	25	-	35	-	ns
		Full	-	50	-	ns
Turn-OFF Time, t_{OFF}	V+ = 4.5V, V_{NO} or V_{NC} = 3.0V, R_L = 50Ω, C_L = 35pF (see Figure 1)	25	-	16	-	ns
		Full	-	22	-	ns
Break-Before-Make Time Delay, t_D	V+ = 5.5V, V_{NO} or V_{NC} = 3.0V, R_L = 50Ω, C_L = 35pF (see Figure 3)	Full	-	18	-	ns
Charge Injection, Q	V_G = 0V, R_G = 0Ω, C_L = 1.0nF (see Figure 2)	25	-	170	-	pC
OFF-Isolation	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{NO} or V_{NC} = $1V_{RMS}$ (see Figure 4)	25	-	60	-	dB
Crosstalk (Channel-to-Channel)	R_L = 50Ω, C_L = 5pF, f = 1MHz, V_{NO} or V_{NC} = $1V_{RMS}$ (See Figure 6)	25	-	-75	-	dB
Total Harmonic Distortion	f = 20Hz to 20kHz, V_{COM} = $0.5V_{P-P}$, R_L = 32Ω	25	-	0.02	-	%
-3dB Bandwidth	V_{COM} = $1V_{RMS}$, R_L = 50Ω, C_L = 5pF	25	-	60	-	MHz
NOx or NCx OFF Capacitance, C_{OFF}	f = 1MHz (see Figure 7)	25	-	36	-	pF
COMx ON Capacitance, $C_{COM(ON)}$	f = 1MHz (see Figure 7)	25	-	88	-	pF

Electrical Specifications - 5V Supply

Test Conditions: V+ = +4.5V to +5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, V_{EN} = V_{INH}, V_{CP} = V_{INL} (Note 4), unless otherwise specified. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 5, 6)	TYP	MAX (Notes 5, 6)	UNITS
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 5.5V, V_{INx} = 0V or V+	25	-	0.008	0.1	µA
		Full	-	1.41	-	µA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		Full	-	-	0.8	V
Input Voltage High, V_{INH}		Full	2.4	-	-	V
Input Current, I_{INH}, I_{INL}	V+ = 5.5V, V_{INx} = 0V or V+	25	-0.1	-	0.1	µA
		Full	-	0.3	-	µA

Electrical Specifications - 4.3V Supply

Test Conditions: V+ = +3.9V to +4.5V, GND = 0V, V_{EN} = V+, V_{INH} = 1.6V, V_{INL} = 0.5V (Note 4), Unless Otherwise Specified**.**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 5, 6)	TYP	MAX (Notes 5, 6)	UNITS
ANALOG SWITCH CHARACTERISTICS						
ON-Resistance, r_{ON}	V+ = 4.3V, I_{COM} = 100mA, V_{NO} or V_{NC} = (V+ -6.5V) to V+ (see Figure 5)	25	-	0.65	-	Ω
		Full	-	0.72	-	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V+ = 4.3V, I_{COM} = 100mA, V_{NO} or V_{NC} = Voltage at max r_{ON} (Note 8)	25	-	10	-	mΩ
		Full	-	15	-	mΩ
r_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 4.3V, I_{COM} = 100mA, V_{NO} or V_{NC} = (V+ -6.5V) to V+ (Note 7)	25	-	0.1	-	Ω
		Full	-	0.14	-	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 4.3V, V_{COM} = -1.2V, 4.3V, V_{NO} or V_{NC} = 4.3V, -1.2V	25	-0.1	-	0.1	µA
		Full	-1	-0.33	1	µA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 4.3V, V_{COM} = -1.2V, 4.3V, V_{NO} or V_{NC} = Float	25	-0.1	-	0.1	µA
		Full	-1	-0.33	1	µA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 3.9V, V_{NO} or V_{NC} = 3.0V, R_L = 50Ω, C_L = 35pF (see Figure 1)	25	-	43	-	ns
		Full	-	50	-	ns
Turn-OFF Time, t_{OFF}	V+ = 3.9V, V_{NO} or V_{NC} = 3.0V, R_L = 50Ω, C_L = 35pF (see Figure 1)	25	-	23.1	-	ns
		Full	-	23.2	-	ns
Break-Before-Make Time Delay, t_D	V+ = 4.5V, V_{NO} or V_{NC} = 3.0V, R_L = 50Ω, C_L = 35pF (see Figure 3)	Full	-	22	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (see Figure 2)	25	-	200	-	pC
OFF-Isolation	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{NO} or V_{NC} = $1V_{RMS}$ (see Figure 4)	25	-	60	-	dB
Crosstalk (Channel-to-Channel)	R_L = 50Ω, C_L = 5pF, f = 1MHz, V_{NO} or V_{NC} = $1V_{RMS}$ (see Figure 6)	25	-	-75	-	dB
Total Harmonic Distortion	f = 20Hz to 20kHz, V_{COM} = $0.5V_{P-P}$, R_L = 32Ω	25	-	0.025	-	%
NOx or NCx OFF Capacitance, C_{OFF}	f = 1MHz (see Figure 7)	25	-	36	-	pF
COMx ON Capacitance, $C_{COM(ON)}$	f = 1MHz (see Figure 7)	25	-	88	-	pF
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 4.5V, V_{IN} = 0V or V+	25	-	0.003	0.1	µA
		Full	-	0.9	-	µA

Electrical Specifications - 4.3V Supply

Test Conditions: V+ = +3.9V to +4.5V, GND = 0V, V_{EN} = V+, V_{INH} = 1.6V, V_{INL} = 0.5V (Note 4), Unless Otherwise Specified**. (Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 5, 6)	TYP	MAX (Notes 5, 6)	UNITS
Positive Supply Current, I+	V+ = 4.2V, V_{IN} = 2.85V	25	-	0.78	12	µA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		Full	-	-	0.5	V
Input Voltage High, V_{INH}		Full	1.6	-	-	V
Input Current, I_{INH}, I_{INL}	V+ = 4.5V, V_{IN} = 0V or V+	25	-0.5	-	0.5	µA
		Full	-	0.2	-	µA

Electrical Specifications - 3V Supply

Test Conditions: V+ = +2.7V to +3.3V, GND = 0V, V_{EN} = V+, V_{INH} = 1.4V, V_{INL} = 0.5V (Note 4), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 5, 6)	TYP	MAX (Notes 5, 6)	UNITS
ANALOG SWITCH CHARACTERISTICS						
ON-Resistance, r_{ON}	V+ = 2.7V, I_{COM} = 100mA, V_{NO} or V_{NC} = (V+ -6.5V) to V+, (See Figure 5)	25	-	0.9	-	Ω
		Full	-	0.96	-	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V+ = 2.7V, I_{COM} = 100mA, V_{NO} or V_{NC} = Voltage at max r_{ON}, (Note 8)	25	-	10	-	mΩ
		Full	-	17	-	mΩ
r_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 2.7V, I_{COM} = 100mA, V_{NO} or V_{NC} = (V+ -6.5V) to V+, (Notes 7, 9)	25	-	0.33	0.5	Ω
		Full	-	0.35	0.55	Ω
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 2.7V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (see Figure 1)	25	-	55	-	ns
		Full	-	82	-	ns
Turn-OFF Time, t_{OFF}	V+ = 2.7V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF, (See Figure 1)	25	-	18	-	ns
		Full	-	24	-	ns
Break-Before-Make Time Delay, t_D	V+ = 3.3V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (see Figure 3)	Full	-	30	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (see Figure 2)	25	-	150	-	pC
OFF-Isolation	R_L = 50Ω, C_L = 35pF, f = 100kHz, V_{NO} or V_{NC} = $1V_{RMS}$ (see Figure 4)	25	-	60	-	dB
Crosstalk (Channel-to-Channel)	R_L = 50Ω, C_L = 35pF, f = 1MHz, V_{NO} or V_{NC} = $1V_{RMS}$ (see Figure 6)	25	-	-75	-	dB
Total Harmonic Distortion	f = 20Hz to 20kHz, V_{COM} = $0.5V_{P-P}$, R_L = 32Ω	25	-	0.04	-	%
NOx or NCx OFF Capacitance, C_{OFF}	f = 1MHz (see Figure 7)	25	-	36	-	pF
COMx ON Capacitance, $C_{COM(ON)}$	f = 1MHz (see Figure 7)	25	-	88	-	pF
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		25	-	-	0.5	V
Input Voltage High, V_{INH}		25	1.4	-	-	V
Input Current, I_{INH}, I_{INL}	V+ = 3.3V, V_{IN} = 0V or V+	25	-0.5	-	0.5	µA
		Full	-	0.2	-	µA

Electrical Specifications - 1.8V Supply

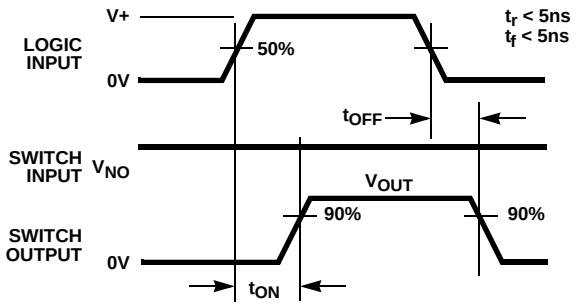
Test Conditions: V+ = +1.8V, GND = 0V, V_{EN} = V+, V_{INH} = 1.0V, V_{INL} = 0.4V (Note 4), Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 5, 6)	TYP	MAX (Notes 5, 6)	UNITS
ANALOG SWITCH CHARACTERISTICS						
ON-Resistance, r_{ON}	V+ = 1.8V, I_{COM} = 100mA, V_{NO} or V_{NC} = (V+ -6.5V) to V+ (see Figure 5)	25	-	1.87	-	Ω
		Full	-	1.97	-	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V+ = 1.8V, I_{COM} = 100mA, V_{NO} or V_{NC} = Voltage at max r_{ON} (Note 8)	25	-	16	-	mΩ
		Full	-	30	-	mΩ
r_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 1.8V, I_{COM} = 100mA, V_{NO} or V_{NC} = (V+ -6.5V) to V+, (Note 7)	25	-	1.34	-	Ω
		Full	-	1.43	-	Ω
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 1.8V, V_{NO} or V_{NC} = 1.8V, R_L = 50Ω, C_L = 35pF (see Figure 1)	25	-	145	-	ns
		Full	-	150	-	ns
Turn-OFF Time, t_{OFF}	V+ = 1.8V, V_{NO} or V_{NC} = 1.8V, R_L = 50Ω, C_L = 35pF (see Figure 1)	25	-	20	-	ns
		Full	-	22	-	ns
Break-Before-Make Time Delay, t_D	V+ = 1.8V, V_{NO} or V_{NC} = 1.8V, R_L = 50Ω, C_L = 35pF (see Figure 3)	Full	-	130	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (see Figure 2)	25	-	40	-	pC
NOx or NCx OFF Capacitance, C_{OFF}	f = 1MHz (see Figure 7)	25	-	36	-	pF
COMx ON Capacitance, $C_{COM(ON)}$	f = 1MHz (see Figure 7)	25	-	88	-	pF
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		25	-	-	0.4	V
Input Voltage High, V_{INH}		25	1.0	-	-	V
Input Current, I_{INH}, I_{INL}	V+ = 2.0V, V_{IN} = 0V or V+	25	-0.5	-	0.5	µA
		Full	-	0.19	-	µA

NOTES:

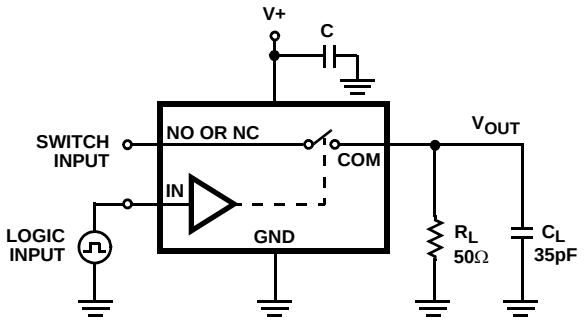
4. V_{IN} = input voltage to perform proper function.
5. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. Flatness is defined as the difference between maximum and minimum value of on-resistance over the specified analog signal range.
8. r_{ON} matching between channels is calculated by subtracting the channel with the highest max r_{ON} value from the channel with lowest max r_{ON} value, between NC1 and NC2 or between NO1 and NO2.
9. Limits established by characterization and are not production tested.

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + r_{ON}}$$

FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

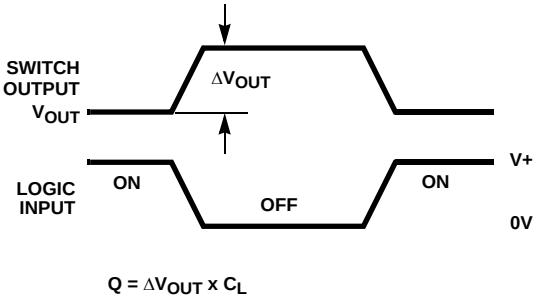
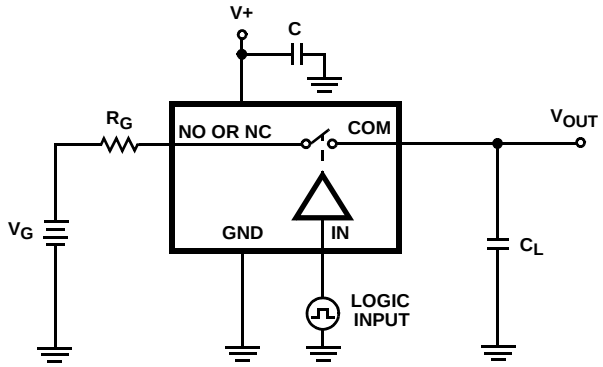


FIGURE 2A. MEASUREMENT POINTS



Repeat test for all switches.

FIGURE 2B. TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

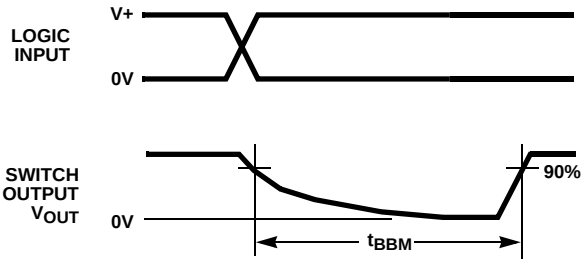
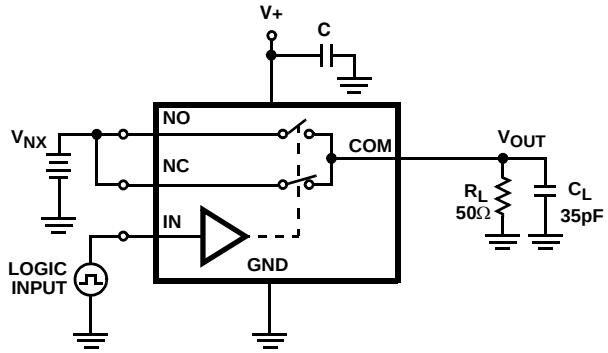


FIGURE 3A. MEASUREMENT POINTS

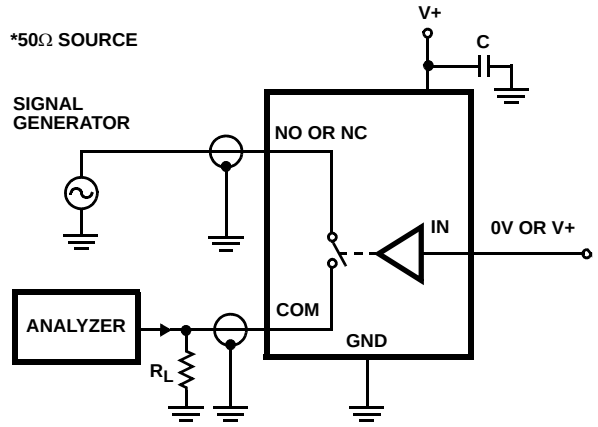


Repeat test for all switches. C_L includes fixture and stray capacitance.

FIGURE 3B. TEST CIRCUIT

FIGURE 3. BREAK-BEFORE-MAKE TIME

Test Circuits and Waveforms (Continued)



Signal direction through switch is reversed, worst case values are recorded.

FIGURE 4. OFF-ISOLATION TEST CIRCUIT

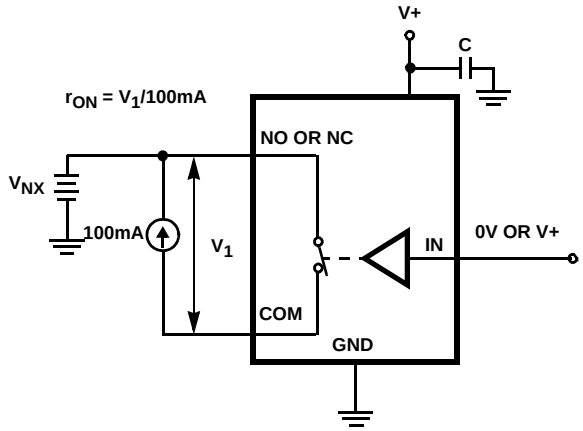
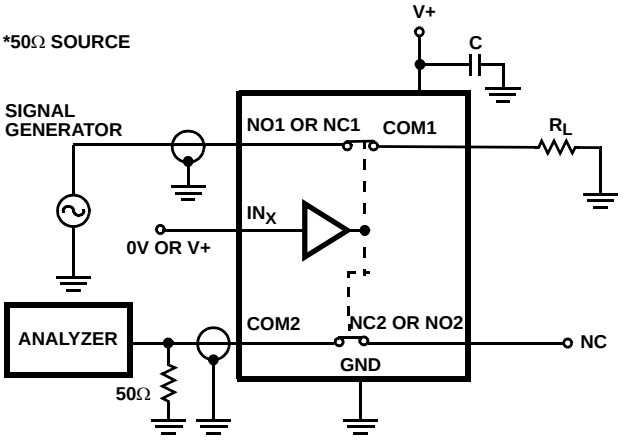
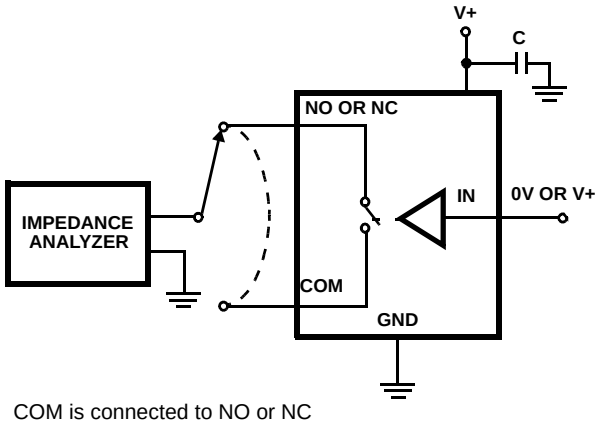


FIGURE 5. r_{ON} TEST CIRCUIT



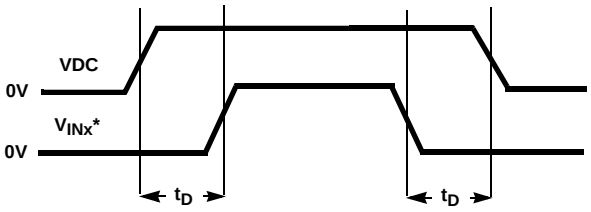
Signal direction through switch is reversed, worst case values are recorded.

FIGURE 6. CROSSTALK TEST CIRCUIT



COM is connected to NO or NC during ON capacitance measurement.

FIGURE 7. CAPACITANCE TEST CIRCUIT



***V_{INx} waveform for Click and Pop Elimination on NOx terminal. For Click and Pop Elimination on NCx terminal invert INx.**

t_D = 200ms measured at 50% points.

FIGURE 8A. CLICK AND POP WAVEFORM

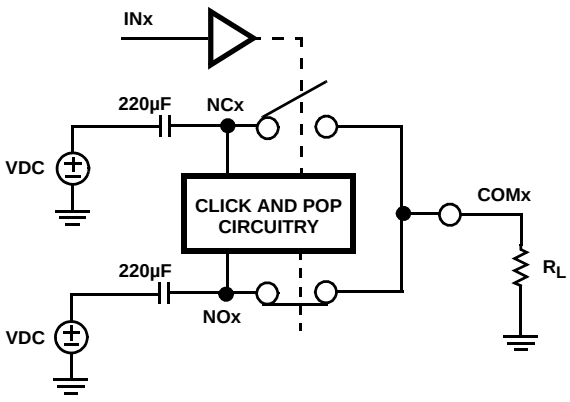


FIGURE 8B. CLICK AND POP TEST CIRCUIT

FIGURE 8. CLICK AND POP ELIMINATION

Detailed Description

The ISL54065 is a bidirectional, dual single pole-double throw (SPDT) analog switch that offers precise switching from a single 1.8V to 6.5V supply with low ON-resistance (0.83Ω) and high speed operation (t_{ON} = 55ns, t_{OFF} = 18ns). The device is especially well suited for portable battery powered equipment due to its low operating supply voltage (1.8V), low power consumption (8nA), and a tiny 2.2x1.4mm µTQFN package. The low ON-resistance and RON flatness provide very low insertion loss and signal distortion for applications that require signal switching with minimal interference by the switch.

Supply Sequencing and Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. The ISL54065 contains ESD protection diodes on each pin of the IC (see Figure 9). These diodes connect to either a +Ring or -Ring for ESD protection. To prevent forward biasing the ESD diodes to the +Ring, V+ must be applied before any input signals, and the input signal voltages must remain between recommended operating range.

If these conditions cannot be guaranteed, then precautions must be implemented to prohibit the current and voltage at the logic pin and signal pins from exceeding the maximum ratings of the switch. The following two methods can be used to provided additional protection to limit the current in the event that the voltage at a logic pin or switch terminal goes above the V+ rail.

Logic inputs can be protected by adding a 1kΩ resistor in series with the logic input (see Figure 9). The resistor limits the input current below the threshold that produces permanent damage.

This method is not acceptable for the signal path inputs. Adding a series resistor to the switch input defeats the purpose of using a low r_{ON} switch. Connecting external Schottky diodes to the signal pins will shunt the fault current to the V+ supply instead of through the internal ESD diodes thereby protecting the switch. These Schottky diodes must be sized to handle the expected fault current.

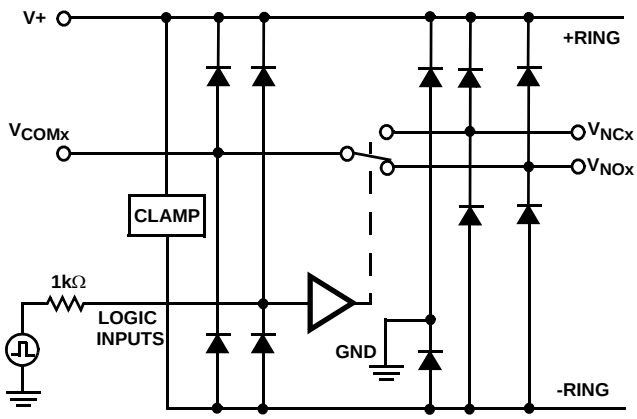


FIGURE 9. OVERVOLTAGE PROTECTION

Power-Supply and By-Pass Considerations

The ISL54065 construction is typical of most single supply CMOS analog switches, in that they have two supply pins: V+ and GND. V+ and GND drive the internal CMOS switches and set their analog voltage limits. Unlike switches with a 5.5V maximum supply voltage, the ISL54065's 6.5V maximum supply voltage provides plenty of head room for the 10% tolerance of 5V supplies due to overshoot and noise spikes.

The minimum recommended supply voltage is 1.8V. It is important to note that the input signal range, switching times, and ON-resistance degrade at lower supply voltages. Refer to "Electrical Specifications" tables, beginning on page 3, and "Typical Performance Curves", beginning on page 11, for details.

V+ and GND also power the internal logic and level shifters. The level shifters convert the input logic levels to V+ and GND signals levels to drive the analog switch gate terminals. A high frequency decoupling capacitor placed as close to the V+ and GND pin as possible is recommended for proper operation of the switch. A value of 0.1µF is highly recommended.

Negative Signal Swing Capability

The ISL54065 contains circuitry that allows the analog switch signal to swing below ground. The device has an analog signal range of 6.5V below V+ up to the V+ rail (see Figure 16) while maintaining low r_{ON} performance. For example, if V+ = 5V, then the analog input signal range is from -1.5V to +5V. If V+ = 2.7V then the range is from -3.8V to +2.7V.

Click and Pop Operation

The ISL54065 contains circuitry that prevents audible click and pop noises that may occur when audio sources are powered on or off. Single supply audio sources are biased at a DC offset that can generate transients during power on/off. A DC blocking capacitor is needed to remove the DC bias at the speaker load. For 32Ω headphones, a 220µF capacitor is typically used to preserve the audio bandwidth. The power

on/off transients are AC coupled by the 220µF capacitor to the speaker load causing a click and pop noise.

The ISL54065 has shunt switches on the NO and NC pins to eliminate click and pop transients (see Figure 10). These switches are driven complimentary to the main switch. When NC is connected to COM, the shunt switch is active on the NO pin (and vice versa). The shunt switches connect an impedance (140Ω typical, see Figure 25) from the NO/NC pin to ground to discharge any transients that may appear on the NO or NC pins.

When the DC bias becomes active at the source, the NO and NC terminals will also have a DC offset due to capacitor dv/dt principle. The DC offset will be discharged through the shunt impedance on the NO and NC terminals instead of the speaker, eliminating click and pop noise. On the ISL54065, the Click and Pop Circuitry is enabled when the CP pin is logic high (>1.4V). The Click and Pop Circuitry may be disabled by tying the CP pin low (<0.4V).

*Under high impedance loads (20kΩ) such as the input impedance of pre-amplifiers, the COM terminal voltage may rise due to small leakage currents charging the COM capacitance. This is not seen when low impedance (32Ω) loads such as headphones are used because the small leakage currents does not result in significant potential drop across the load. If the user desires to reduce the voltage build up on the COM pin, a 1kΩ to ground may be placed on the COM pin. This impedance is small enough to reduce the voltage build up significantly while not increasing the power dissipation dramatically. Current consumption considerations will need to be taken for driving a smaller load impedance under this scenario.

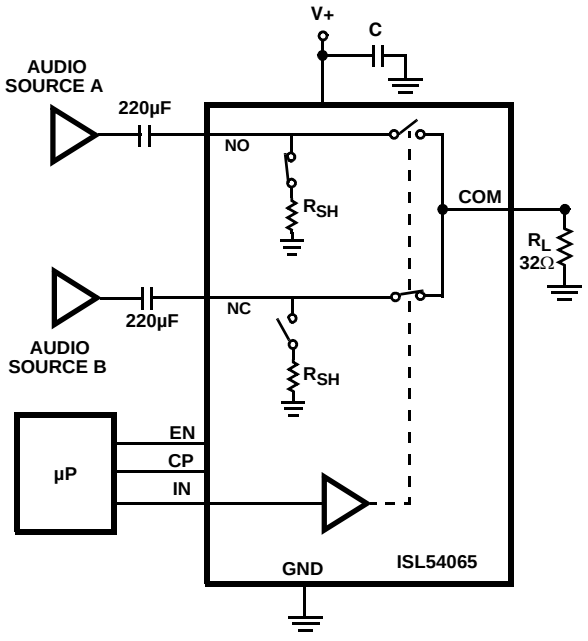


FIGURE 10. CLICK AND POP OPERATION

Click and Pop with Enable Pin

Click and pop elimination can be driven with the Enable pin by setting it low. Having the Enable pin low turns OFF the main switches (NO and NC) while the Click and Pop Circuitry will be active. Transient voltages due to power on/off from both sources will be shunted to ground. For proper Click and Pop Elimination the Enable pin should be driven high at least 200ms after any source transients occurs to avoid audible transients at the speaker load.

Click and Pop with Input Select Pin

Click and pop elimination can also be driven with the Input Select pin. When INx = 0, the NOx terminals are connected to the shunt impedance. When INx = 1, the NCx terminals are connected to the shunt impedance. In this situation, only one of the source transient voltages will be shunted to ground, depending on the Input Select state. The Input Select pin should be driven 200ms after any source transients occurs to prevent audible transients at the speaker load.

Logic-Level Thresholds

This switch family is 1.8V CMOS compatible (0.45V V_{OLMAX} and 1.35V V_{OHMIN}) over a supply range of 1.8V to 3.3V (see Figure 16). At 3.3V the V_{IL} level is 0.5V maximum. This is still below the 1.8V CMOS guaranteed low output maximum level of 0.45V, but noise margin is reduced. At 3.3V the V_{IH} level is 1.4V minimum. While this is above the 1.8V CMOS guaranteed high output minimum of 1.35V under most operating conditions the switch will recognize this as a valid logic high.

The digital input stages draws a larger supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation. The ISL54065 has been designed to minimize the supply current whenever the digital input voltage is not driven to the supply rails (0V to V+). For example driving the device with 2.85V logic high while operating with a 4.2V supply the device draws only 1µA of current.

High-Frequency Performance

In 50Ω systems, the ISL54065 has an ON switch -3dB bandwidth of 60MHz (see Figure 21). The frequency response is very consistent over a wide V+ range, and for varying analog signal levels.

An OFF switch acts like a capacitor across the open terminals and AC couples higher frequencies, resulting in signal feed-through from a switch's input to its output. Off-Isolation is the resistance to this feed-through. Crosstalk indicates the amount of feed-through from one switch channel to another switch channel. Figure 22 details the high Off-Isolation and Crosstalk rejection provided by this part. At 100kHz, Off-Isolation is about 60dB in 50Ω systems, decreasing approximately 20dB per decade as frequency

increases. At 1MHz, Crosstalk is about -75dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases.

Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin, V+ and GND. One of these diodes conducts if any analog signal exceeds the recommended analog signal range.

Virtually all the analog switch leakage current comes from the ESD diodes and reversed biased junctions in the switch cell. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased to either the +Ring or -Ring and the analog input signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the +Ring or -Ring and the reverse biased junctions at the internal switch cell constitutes the analog-signal-path leakage current.

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified

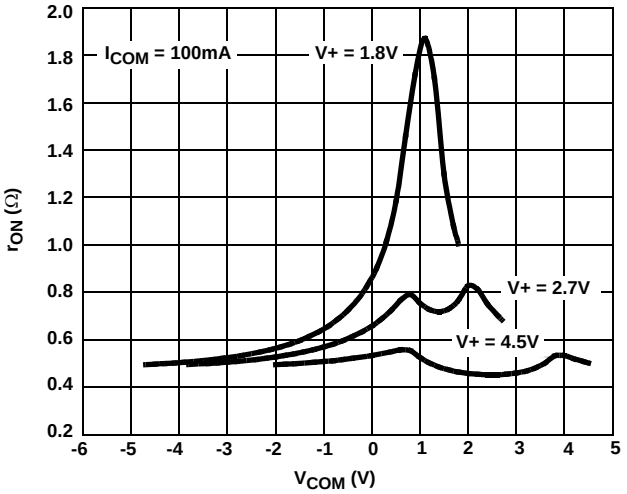


FIGURE 11. ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

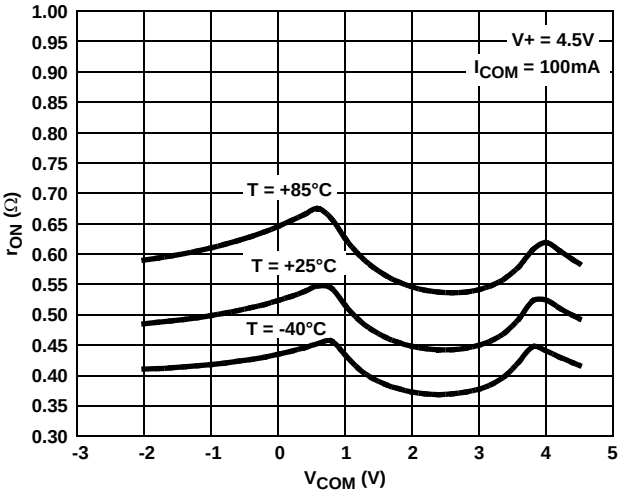


FIGURE 12. ON-RESISTANCE vs SWITCH VOLTAGE

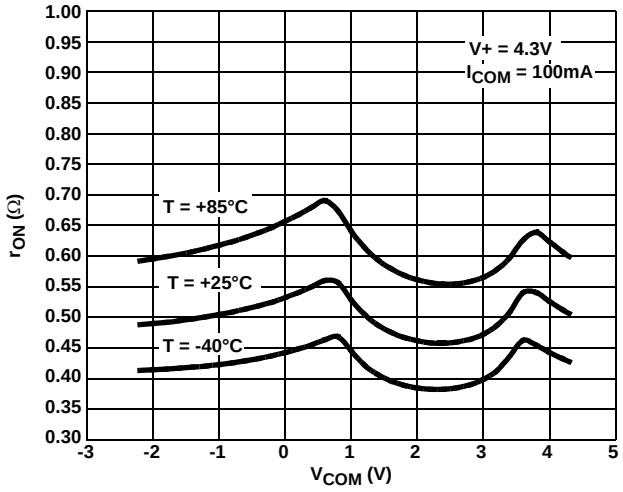


FIGURE 13. ON-RESISTANCE vs SWITCH VOLTAGE

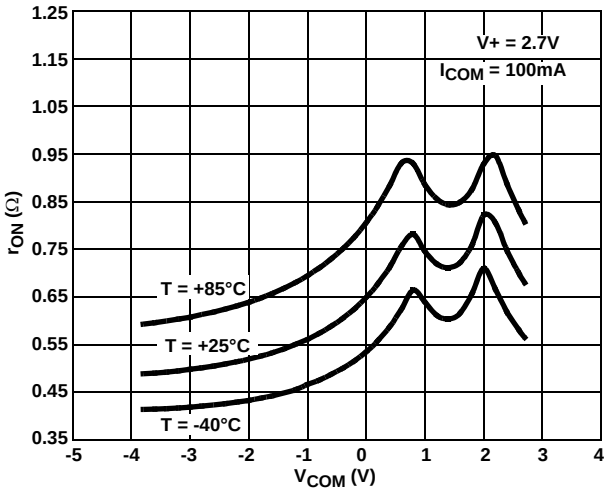


FIGURE 14. ON-RESISTANCE vs SWITCH VOLTAGE

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

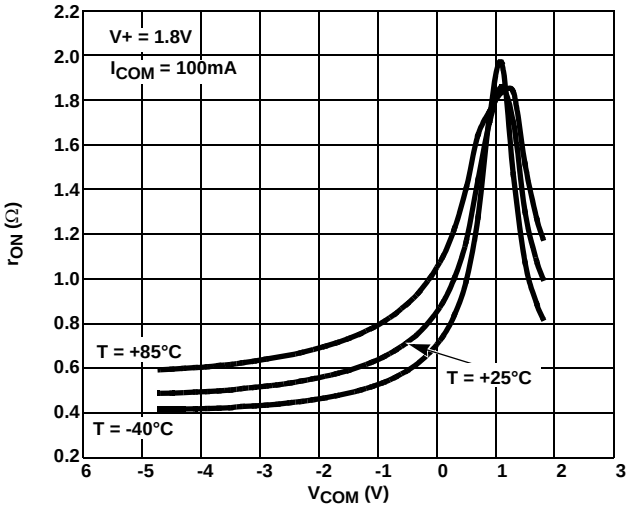


FIGURE 15. ON-RESISTANCE vs SWITCH VOLTAGE

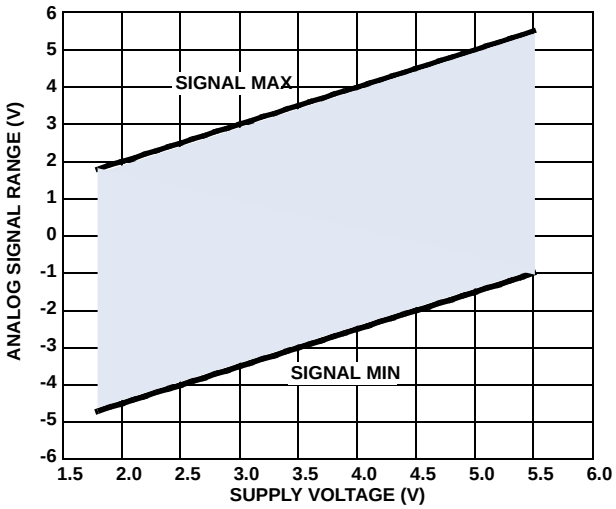


FIGURE 16. ANALOG SIGNAL RANGE vs SUPPLY VOLTAGE

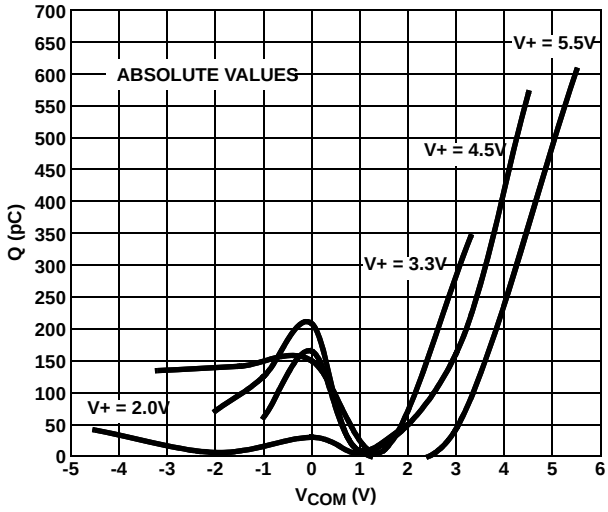


FIGURE 17. CHARGE INJECTION vs SWITCH VOLTAGE

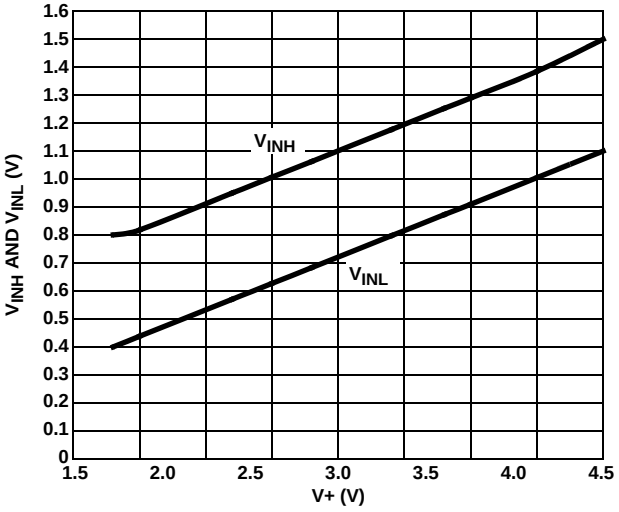


FIGURE 18. DIGITAL SWITCHING POINT vs SUPPLY VOLTAGE

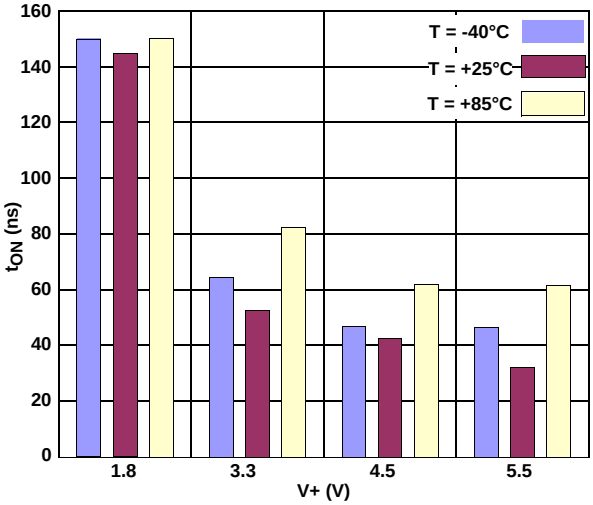


FIGURE 19. TURN - ON TIME vs SUPPLY VOLTAGE

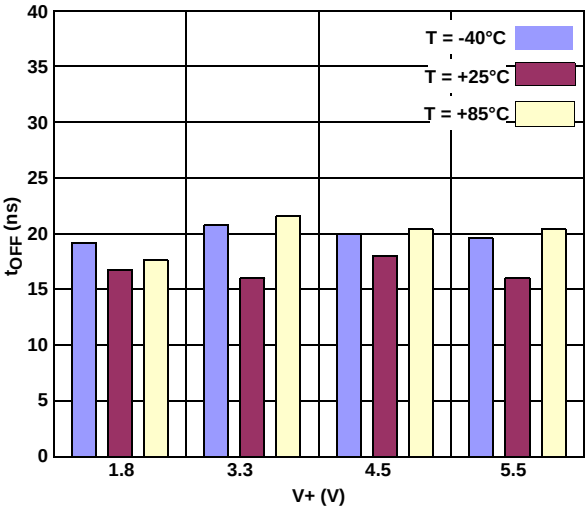


FIGURE 20. TURN - OFF TIME vs SUPPLY VOLTAGE

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

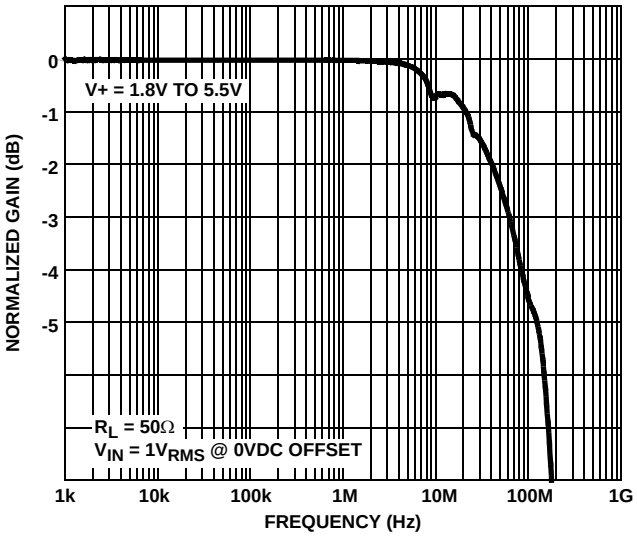


FIGURE 21. FREQUENCY RESPONSE

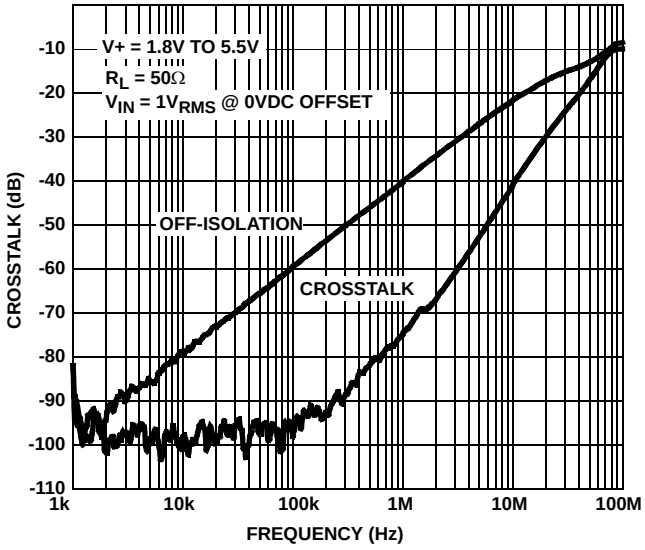


FIGURE 22. CROSSTALK AND OFF ISOLATION

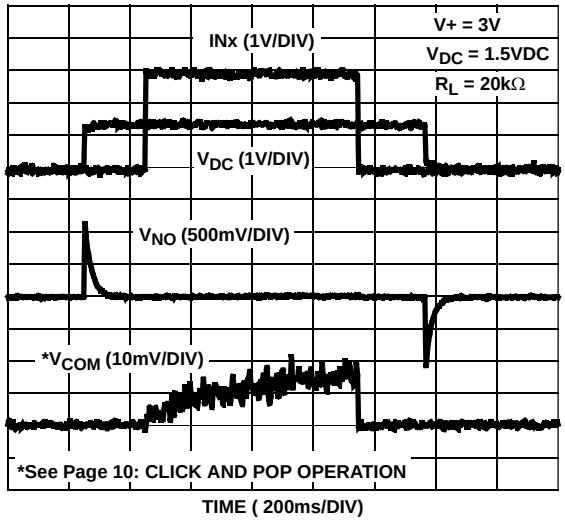


FIGURE 23. CLICK AND POP ELIMINATION 20kΩ LOAD 200ms DELAY

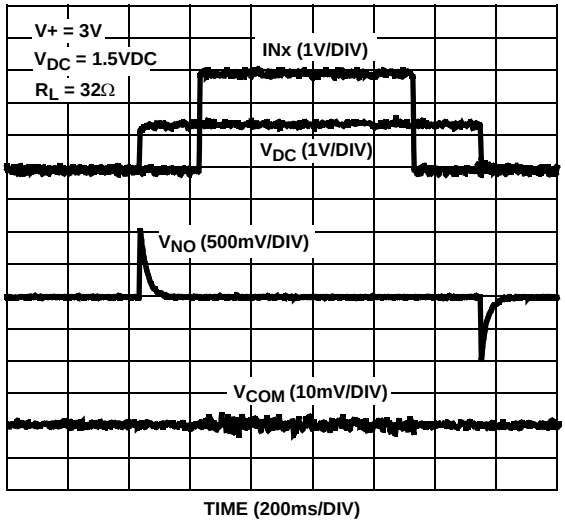


FIGURE 24. CLICK AND POP ELIMINATION 32Ω LOAD 200ms DELAY

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

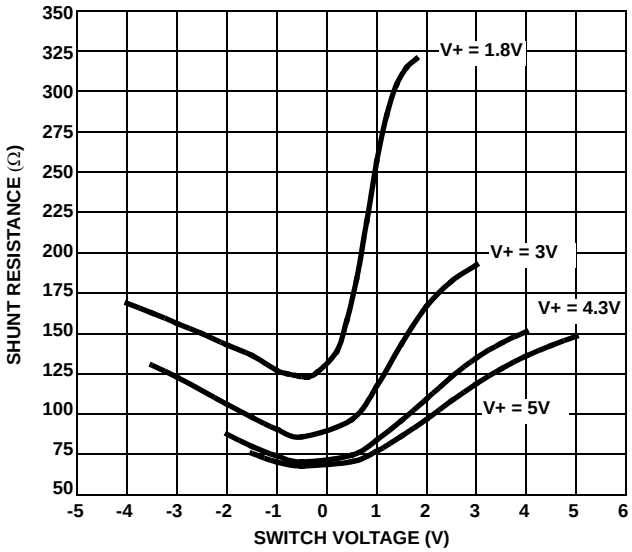


FIGURE 25. SHUNT RESISTANCE vs SWITCH VOLTAGE

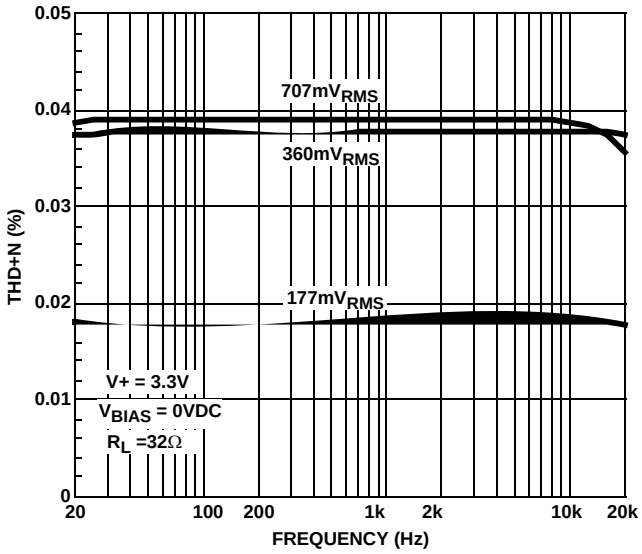


FIGURE 26. TOTAL HARMONIC DISTORTION vs FREQUENCY

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND (DFN Paddle Connection: Tie to GND or Float)

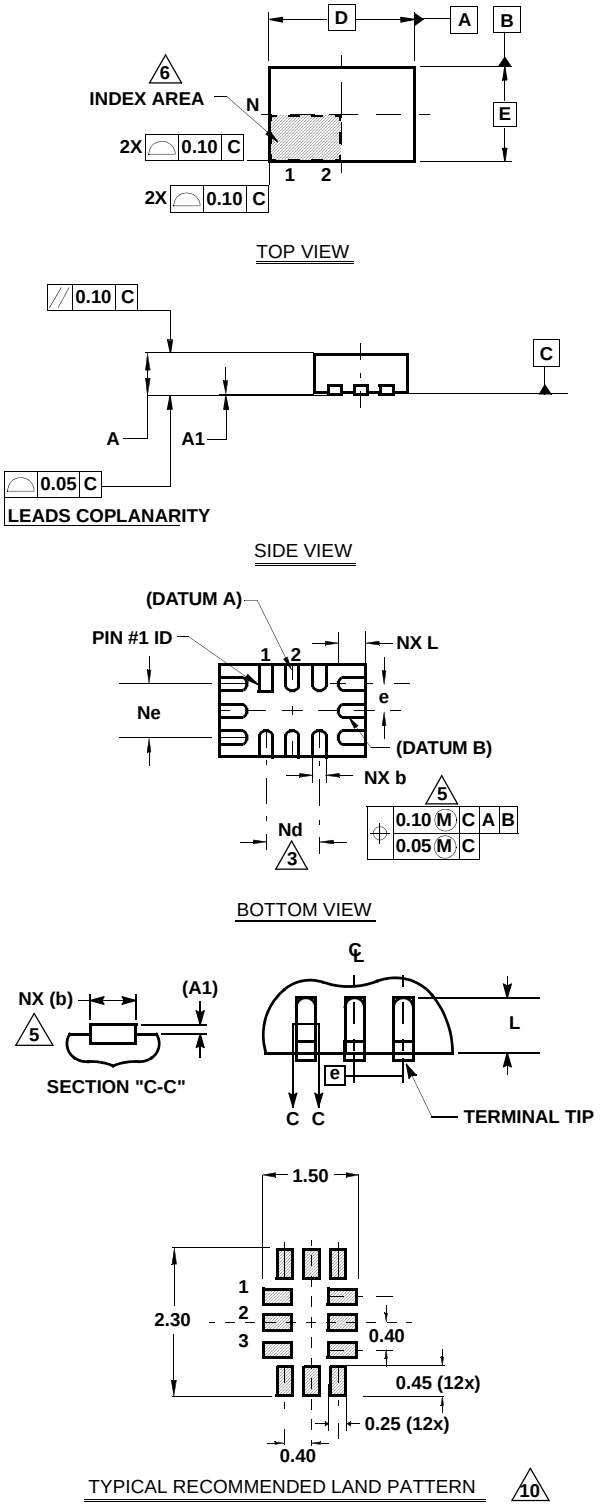
TRANSISTOR COUNT:

432

PROCESS:

Submicron CMOS

Ultra Thin Quad Flat No-Lead Plastic Package (UTQFN)



L12.2.2x1.4A

12 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3		0.127 REF		-
b	0.15	0.20	0.25	5
D	2.15	2.20	2.25	-
E	1.35	1.40	1.45	-
e		0.40 BSC		-
k	0.20	-	-	-
L	0.35	0.40	0.45	-
N		12		2
Nd		3		3
Ne		3		3
θ	0	-	12	4

Rev. 0 12/06

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on D and E side, respectively.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Maximum package warpage is 0.05mm.
8. Maximum allowable burrs is 0.076mm in all directions.
9. Same as JEDEC MO-255UABD except:
   No lead-pull-back, "A" MIN dimension = 0.45 not 0.50mm
   "L" MAX dimension = 0.45 not 0.42mm.
10. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.