TLE493D-W2B6

Low Power 3D Hall Sensor with I²C Interface and Wake Up Function

User Manual

About this document

Scope and purpose

This document provides product information and descriptions regarding:

- I²C Registers
- I²C Interface
- Wake Up mode
- Diagnostic and Tests

Intended audience

This document is aimed at engineers and developers of hard and software using the sensor TLE493D-W2B6.

Table of contents

1 I^2C Registers

The TLE493D-W2B6 includes several registers that can be accessed via Inter-Integrated Circuit interface (I^2C) to read data as well as to write and configure settings.

1.1 Registers overview

A bitmap overview is presented in Figure 1. Basically the following sections are available:

- measurement data (green bits in registers 00_H till 05_H)
- sensor status and diagnostics (grey bits in registers 05_H, 06_H, $0E_H$, $0F_H$, 10_H and 11_H)
- configuration parameters such as the power mode (orange bits in registers 10_H, 11_H and 13_H)
- Wake Up values in registers (blue bits in registers 07_H till $0F_H$).

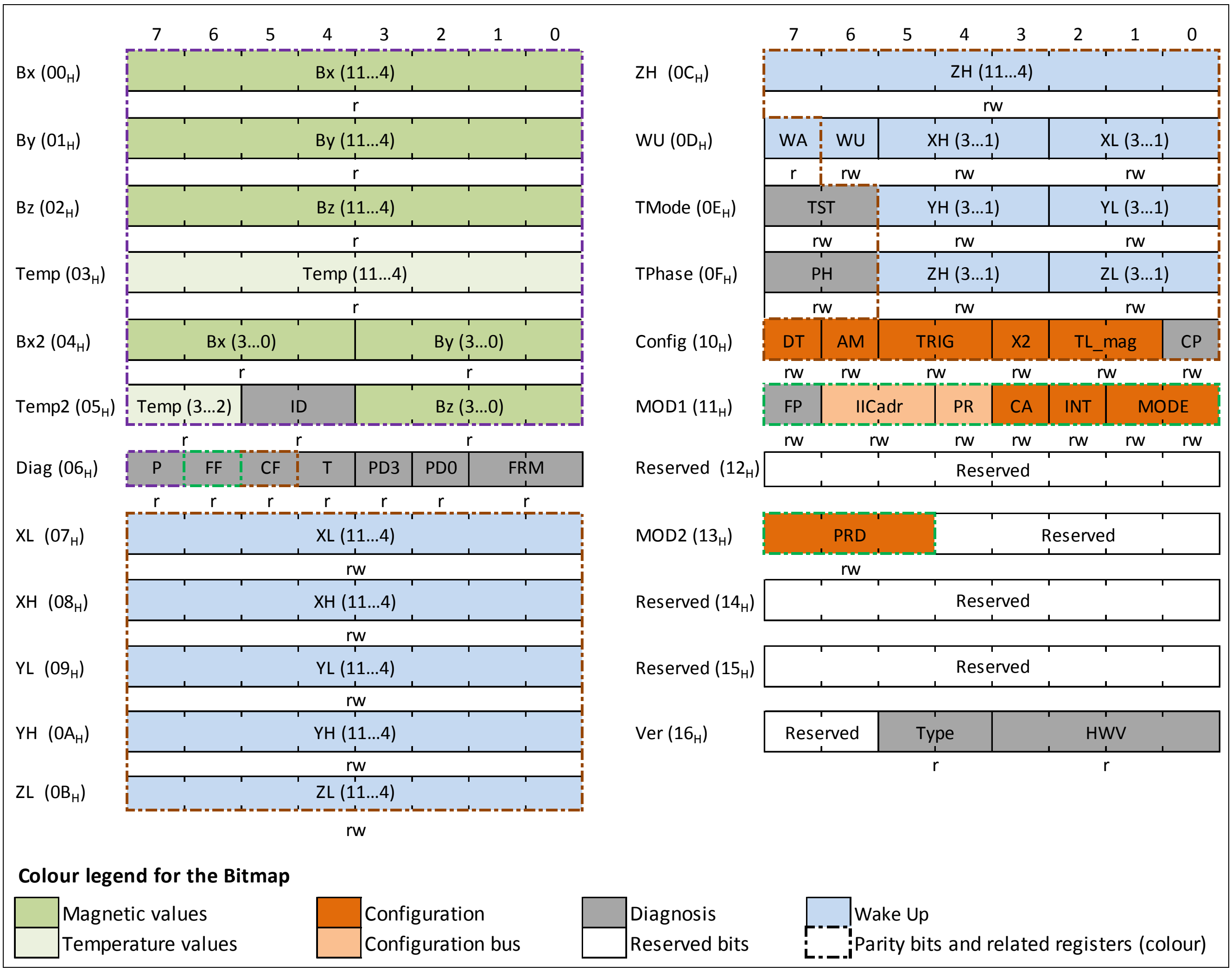

Figure 1 TLE493D-W2B6 Bitmap

The diagnostic register 06_H contains parity information as a diagnostic mechanism. The bitmap illustrates this and marks the relationship of the sections to this flags with different colored lines/frames around the bit contents.

Table 1 Registers overview

Register name	Register long name	Address
Bx, By and Bz	Magnetic values MSBs	00_H, 01_H, 02_H
Temp	Temperature value MSBs	03_H
Bx2	Magnetic values LSBs	04_H
Temp2	Temperature and magnetic LSBs and device address	05_H
Diag	Sensor diagnostic and status register	06_H
XL, YL and ZL	Wake Up lower threshold MSBs	07_H, 09_H, $0B_H$
XH, YH and ZH	Wake Up upper threshold MSBs	08_H, $0A_H$, $0C_H$
WU	Wake Up X thresholds LSBs	$0D_H$
TMode	Test Mode and Wake Up Y thresholds LSBs	$0E_H$
TPhase	Test Phase and Wake Up Z thresholds LSBs	$0F_H$
Config	Configuration register	10_H
MOD1	Power mode, interrupt, address, parity	11_H
MOD2	Low Power Mode update rate	13_H
Ver	Version register	16_H

1.2 Register descriptions

The I^2C registers can be read or written at any time. It is recommended to read measurement data in a synchronized fashion, i.e. after an interrupt pulse (/INT). This avoids reading inconsistent sensor or diagnostic data, especially in fast mode. Additionally, several flags can be checked to ensure the register values are consistent and the ADC was not running at the time of readout.

1.2.1 Bit types

The TLE493D-W2B6 contains read bits, write bits and reserved bits.

Table 2 Bit Types

Abbreviation	Function	Description
r	Read	Read-only bits
rw	Read Write	Readable and writable bit
	Reserved	Bits that must keep the default values (read prior to write required)

1.2.2 Measurement data and registers combined in the I^2C parity bit “P”

The I^2C communication of the registers in this chapter is protected with the parity bit “P”, described in the Diag register with the address 06_H. See also Figure 1 - parity bits and related registers.

To make sure all data is consistent, the registers from 00_H to 06_H should be read with the same I^2C command. Otherwise, the sampled data (X, Y, Z, Temperature) may correspond to different conversion cycles.

Magnetic values MSBs

Register names	Address	Reset Value
Bx, By and Bz	00_H 01_H 02_H	80_H

7 … 0
Bx, By and Bz (11…4)

Field	Bits	Type	Description
Bx, By and Bz	7:0	r	Bx, By and Bz values Signed value as two's complement from the HALL probes in the x, y and z-direction of the magnetic field. Contains the eight Most Significant Bits. If Bz is deactivated the Bz value is the reset value.

Back to TLE493D-W2B6 Bitmap.

Temperature value MSBs

Register name	Address	Reset Value
Temp	03_H	80_H

7 … 0
Temp (11…4)

Field	Bits	Type	Description
Temp	7:0	r	Temperature value Signed value as two's complement. If the temperature measurement is deactivated, the Temp value is the reset value.

Back to TLE493D-W2B6 Bitmap.

Magnetic values LSBs

Register name	Address	Reset Value
Bx2	04_H	00_H

7 … 4	3 … 0
Bx (3…0)	**By** (3…0)

Field	Bits	Type	Description
Bx	7:4	r	Bx value Signed value as two's complement from the HALL probes in the x-direction of the magnetic field. Contains the four Least Significant Bits.
By	3:0	r	By value Signed value as two's complement from the HALL probes in the y-direction of the magnetic field. Contains the four Least Significant Bits.

Back to TLE493D-W2B6 Bitmap.

Temperature and magnetic LSBs and device address

Register name	Address	Reset Value
Temp2	05_H	(Product Type A0) **00_H** (Product Type A1) **10_H** (Product Type A2) **20_H** (Product Type A3) **30_H**

7	6	5	4	3			0
Temp (3…2)		**ID**		**Bz** (3…0)			

Field	Bits	Type	Description
Temp	7:6	r	Temperature value Signed value as two's complement. If the temperature measurement is deactivated, the Temp value is the reset value.
ID	5:4	r	ID Readback of the sensor ID, from IICadr. µC shall verify the address sent by the sensor. See Table 4.
Bz	3:0	r	Bz value Signed value as two's complement from the HALL probes in the z-direction of the magnetic field. Contains the four Least Significant Bits. If Bz is deactivated the Bz value is 0_H.

Back to TLE493D-W2B6 Bitmap.

1.2.3 Wake Up and registers combined in the I^2C parity flag “CF”

The I^2C communication of the registers in this chapter is protected by the parity bit CF, which is described in the Diag register with the address 06_H. See also Figure 1 - parity bits and related registers.

Wake Up lower threshold MSBs

Register names	Address	Reset Value
XL, YL and ZL	07_H 09_H $0B_H$	80_H

7							0
XL, YL and ZL (11...4)							

Field	Bits	Type	Description
XL, YL and ZL	7:0	rw	Wake Up lower threshold Defines the lower threshold MSBs of the magnetic field density in the x, y and z-direction at or below which the sensor enables the /INT, if INT bit = 0_B. See Equation (3.2).

Back to TLE493D-W2B6 Bitmap.

Wake Up upper threshold MSBs

Register names	Address	Reset Value
XH, YH and ZH	08_H $0A_H$ $0C_H$	$7F_H$

7							0
XH, YH and ZH (11...4)							

Field	Bits	Type	Description
XH, YH and ZH	7:0	rw	Wake Up upper threshold Defines the upper threshold MSBs of the magnetic field in the x, y and z-direction at or above which the sensor enables the /INT, if INT bit = 0_B. See Equation (3.2).

Back to TLE493D-W2B6 Bitmap.

Wake Up X thresholds LSBs

Register name	Address	Reset Value
WU	$0D_H$	38_H

7	6	5 ... 3	2 ... 0
WA	**WU**	**XH** (3...1)	**XL** (3...1)

Field	Bits	Type	Description
WA	7	r	**Wake Up mode active** Flag that reports whether the Wake Up mode is disabled or enabled. If 0_B the Wake Up mode is disabled. If 1_B the Wake Up mode is enabled. This bit can be checked if the Wake Up function is disabled or enabled. As long as the WA bit = 0_B, the /INT will be asserted according Table 5.
WU	6	rw	**Enables Wake Up mode** If 0_B the Wake Up mode will be disabled. If 1_B the Wake Up mode will be enabled. The following conditions must be fulfilled: - Test modes must be disabled (T bit = 0_B) - CP parity bit (register 10_H) must be odd - Configuration parity must be flagged (CF bit = 1_B) Interrupts /INT will be sent when the measurement data is ≥ upper or ≤ lower Wake Up threshold.
XH	5:3	rw	**Wake Up X upper threshold** Defines the upper threshold LSBs of the magnetic field in the x-direction at or above the sensor enables the /INT, if INT bit = 0_B. See Equation (3.2).
XL	2:0	rw	**Wake Up X lower threshold** Defines the lower threshold LSBs of the magnetic field density in the x-direction at or below the sensor enables the /INT, if INT bit = 0_B. See Equation (3.2).

Back to TLE493D-W2B6 Bitmap.

Test Mode and Wake Up Y thresholds LSBs

Register name	Address	Reset Value
TMode	$0E_H$	38_H

7 ... 6	5 ... 3	2 ... 0
TST	**YH** (3...1)	**YL** (3...1)

Field	Bits	Type	Description
TST	7:6	rw	**Test mode** Different test modes can be enabled, see Table 3: If 00_B no test active (normal sensor operation and T bit = 0_B). In the following test modes the T bit = 1_B and the test result overwrites the measurement data register: If 01_B Vhall/Vext test starts: measure the Hall bias voltage on all Hall plates and V_{DD}. If 10_B Spintest starts: the PH bits select the channel to diagnose with the Spin-switch and Hall-offset test. If 11_B SAT test starts: a test of the whole digital path, generates patterns, defined by the PH bits during conversion.
YH	5:3	rw	**Wake Up Y upper threshold** Defines the upper threshold LSBs of the magnetic field in the y-direction at or above which the sensor enables the /INT, if INT bit = 0_B. See Equation (3.2).
YL	2:0	rw	**Wake Up Y lower threshold** Defines the lower threshold LSBs of the magnetic field density in the y-direction at or below which the sensor enables the /INT, if INT bit = 0_B. See Equation (3.2).

Back to TLE493D-W2B6 Bitmap.

Test Phase and Wake Up Z thresholds LSBs

Register name	Address	Reset Value
TPhase	$0F_H$	38_H

7	6	5		3	2		0
PH		**ZH** (3...1)			**ZL** (3...1)		

Field	Bits	Type	Description
PH	7:6	rw	**Test phase selection** In the Spintest these bits define the channel. In the digital test, specific patterns are defined. See Table 3. The PH bits have no effect in the voltage measurement test (Vext) and in normal operating mode TST bit = 00_B and T bit = 0_B).
ZH	5:3	rw	**Wake Up Z upper threshold** Defines the upper threshold LSBs of the magnetic field in the z-direction at or above which the sensor enables the /INT, if INT bit = 0_B. See Equation (3.2).

Field	Bits	Type	Description
ZL	2:0	rw	**Wake Up Z lower threshold** Defines the lower threshold LSBs of the magnetic field density in the z-direction at or below which the sensor enables the /INT, if INT bit = 0_B. See Equation (3.2).

Back to TLE493D-W2B6 Bitmap.

Table 3 Test mode interaction of TST, PH and X2 bits

TST bits	PH bits	X2 bit	Bx (11 ... 0)	By (11 ... 0)	Bz (11 ... 0)	T (11 ... 2)
00_B	don't care	0_B	Bx full-range	By full-range	Bz full-range	T full-range
00_B	don't care	1_B	Bx short-range	By short-range	Bz short-range	T full-range
01_B	don't care	don't care	Vhall X	Vhall Y	Vhall Z	Voltage V_{DD}
10_B	00_B	don't care	Spintest-Bx, spin-0 disabled	Spintest-Bx, spin-1 disabled	Spintest-Bx, spin-2 disabled	Spintest-Bx, spin-3 disabled
10_B	01_B	don't care	Spintest-By, spin-0 disabled	Spintest-By, spin-1 disabled	Spintest-By, spin-2 disabled	Spintest-By, spin-3 disabled
10_B	10_B	don't care	Spintest-Bz, spin-0 disabled	Spintest-Bz, spin-1 disabled	Spintest-Bz, spin-2 disabled	Spintest-Bz, spin-3 disabled
10_B	11_B	don't care	Spintest-T, setting1	Spintest-T, setting2	Spintest-T, setting2	Spintest-T, setting1
11_B	00_B	0_B	$79F_H$	806_H	$7FF_H$	200_H
11_B	01_B	0_B	806_H	$7F9_H$	800_H	$1FF_H$
11_B	10_B	0_B	$7FF_H$	800_H	$7F9_H$	203_H
11_B	11_B	0_B	800_H	$7FF_H$	806_H	$1FC_H$
11_B	00_B	1_B	$7F0_H$	$80F_H$	$7FF_H$	200_H
11_B	01_B	1_B	$80F_H$	$7F0_H$	800_H	$1FF_H$
11_B	10_B	1_B	$7FF_H$	800_H	$7F0_H$	203_H
11_B	11_B	1_B	800_H	$7FF_H$	$80F_H$	$1FC_H$

Configuration register

Register name	Address	Reset Value
Config	10_H	01_H

7	6	5	4	3	2	1	0
DT	AM	TRIG		X2	TL_mag		CP

Field	Bits	Type	Description
DT	7	rw	Disable Temperature If 0_B temperature measurement is enabled. If 1_B temperature measurement is disabled. This means the Bx, By and Bz channels are measured. The Temp channel is disabled and contains the reset value until a new conversion with Temp is done.
AM	6	rw	X/Y Angular Measurement If 0_B the Bz measurement is enabled. If 1_B and the DT bit = 1_B the Bz measurement is disabled. This means the Bx and By channel is measured. The channels Bz and Temp contain the reset values until a new conversion with Bz and Temp is done. Note: If the DT bit = 0_B, the AM bit don't care.
TRIG	5:4	rw	Trigger options If PR bit = 1_B (1-byte read protocol), the TRIG bits define the trigger mode of the device: If 00_B no trigger on read. If 01_B trigger on read of register address 00_H. If $1x_B$ trigger on read of register address 06_H. If PR bit = 0_B these bits have no effect.
X2	3	rw	Short-range sensitivity When this bit is set, the sensitivity of the Bx, By, and Bz ADC-conversion is doubled by a longer ADC integration time. The Temp result will not change, neither in sensitivity nor conversion time.
TL_mag	2:1	rw	Magnetic temperature compensation There are two bits for setting the sensitivity over temperature of the sensor to compensate a magnet temperature coefficient. If $00_B \rightarrow TC_0$ (no compensation) If $01_B \rightarrow TC_1$ If $10_B \rightarrow TC_2$ If $11_B \rightarrow TC_3$
CP	0	rw	Wake Up and configuration parity The registers 07_H through 10_H (including 10_H) without WA TST and PH bit are odd parity protected with this bit. On startup or reset this parity is false and the CF bit in the status register 06_H is cleared. Thus the CP bit has to be corrected once after startup or a reset. If this parity bit is incorrect during a write cycle, the Wake Up is disabled.

Back to TLE493D-W2B6 Bitmap.

1.2.4 Mode registers combined in the I^2C parity flag “FF”

The I^2C communication of the registers in this chapter is protected with the parity bit “FF”, described in the Diag register with the address 06_H. See also Figure 1 - parity bits and related registers.

Power mode, interrupt, address, parity

Register name	Address	Reset Value
MOD1	11_H	(Product Type A0) **00_H** (Product Type A1) **20_H** (Product Type A2) **40_H** (Product Type A3) **60_H**

7	6	5	4	3	2	1	0
FP	**IICadr**		**PR**	**CA**	**INT**	**MODE**	

Field	Bits	Type	Description
FP	7	rw	**Fuse parity** The registers 11_H and 13_H (bits 7:5) are odd parity protected with this bit. If this parity bit is incorrect please see FF bit. To exit this state a sensor reset is necessary.
IICadr	6:5	rw	**I^2C address** Bits can be set to 00_B, 01_B, 10_B or 11_B to define the slave address in bus configuration. See Table 4 and data sheet.
PR	4	rw	**I^2C 1-byte or 2-byte read protocol** If 0_B this is the 2-byte read protocol: <start> <I²Cadr.> <reg.adr.> <data of reg.adr.> <data of reg.adr.+1> …. <stop> If 1_B this is the 1-byte read protocol: <start> <I²Cadr.> <data of reg.00_H> <data of reg.01_H> …. <stop> See Chapter 2.1.3
CA	3	rw	**Collision avoidance** Clock stretching only in master-controlled and low-power mode, not in fast mode. The CA bit interacts with the INT bit, see Table 5 and Chapter 2.2.
INT	2	rw	**Interrupt enabled** If 1_B /INT disabled If 0_B /INT enabled: After a completed measurement and ADC-conversion, an /INT pulse will be generated. For bus configurations /INT timing constraints between I^2C data transfers and interrupt pulses must be monitored and aligned. In Wake Up mode /INT pulses can be disabled, see Figure 15. The INT bit interacts with the CA bit, see Table 5.

Field	Bits	Type	Description
MODE	1:0	rw	**Power mode** If 00_B Low Power Mode: Cyclic measurements and ADC-conversions with a update rate, defined in the PRD registers. If 01_B Master Controlled Mode (Power Down mode): Measurement triggering depends on the PR bit and is possible with I^2C sub address byte (see Table 4) or TRIG bits. If 10_B is reserved and must not be used. If 11_B Fast Mode: The measurements and ADC-conversions are running continuously. It is recommended to set INT = 0_B and use a I^2C clock speed ≥ 800 kHz.

Back to TLE493D-W2B6 Bitmap.

Table 4 Device address overview

The addresses are selected to ensure a minimum Hamming distance of 4 between them.

Product Type	Default address[1] write	Default address[1] read	IICadr (bit-6)	IICadr (bit-5)	ID (bit-5)	ID (bit-4)
A0	$6A_H$	$6B_H$	0_B	0_B	0_B	0_B
A1	44_H	45_H	0_B	1_B	0_B	1_B
A2	$F0_H$	$F1_H$	1_B	0_B	1_B	0_B
A3	88_H	89_H	1_B	1_B	1_B	1_B

1) See data sheet ordering information

Table 5 /INT (interrupt) and clock stretching

In case the microcontroller tries to read sensor data the clock stretching pulls the SCL /INT line to low, as long as the measurement and ADC-conversion is not finished.

CA	INT	Configuration
0_B	0_B	/INT is enabled and will not be transmitted between <START> and <STOP>. /INT collision avoidance active.
0_B	1_B	/INT disabled. Clock stretching enabled. Suppress sensor read out during ongoing ADC conversion.
1_B	0_B	/INT is enabled and will be transmitted between <START> and <STOP>. /INT may collide with I^2C clock from microcontroller.
1_B	1_B	/INT disabled. Clock stretching disabled. Unsynchronized sensor readouts may collide with ADC conversion.

Low Power Mode update rate

Register name	Address	Reset Value
MOD2	13_H	00_H

7–5	4–0
PRD	Reserved

Field	Bits	Type	Description
PRD	7:5	rw	Update rate settings If 000_B typ. update frequency f_{Update} ≈ 770 Hz. If 001_B typ. update frequency f_{Update} ≈ 97 Hz. If 010_B typ. update frequency f_{Update} ≈ 24 Hz. If 011_B typ. update frequency f_{Update} ≈ 12 Hz. If 100_B typ. update frequency f_{Update} ≈ 6 Hz. If 101_B typ. update frequency f_{Update} ≈ 3 Hz. If 110_B typ. update frequency f_{Update} ≈ 0.4 Hz. If 111_B typ. update frequency f_{Update} ≈ 0.05 Hz.
Reserved	4:0		Factory settings

Back to TLE493D-W2B6 Bitmap.

1.2.5 Diagnostic, status and version registers

The device provides diagnostic and status information in register 06_H and version information in register 16_H.

Sensor diagnostic and status register

Register name	Address	Reset Value
Diag	06_H	60_H

7	6	5	4	3	2	1–0
P	**FF**	**CF**	**T**	**PD3**	**PD0**	**FRM**

Field	Bits	Type	Description
P	7	r	Bus parity This bit adds up to an odd parity of the registers 00_H through 05_H (including 05_H), described in Chapter 1.2.2. The parity bit is generated during the I^{2}C readout. The address byte, register byte and acknowledge bits are not included in the parity sum. If the parity calculated by the microcontroller after I^{2}C reads is incorrect, these values must be treated as invalid.

Field	Bits	Type	Description
FF	6	r	Fuse parity flag Provides a flag from the internal fuse parity check of registers 11_H to 15_H. This parity check includes the FP bit. If 1_B parity is OK. If 0_B the parity is not correct. The sensor must be considered defective and must no longer be used. A sensor with an invalid fuse parity disconnects its SDA. It will automatically go to low-power mode and only uses the /INT signal to communicate the error (collision avoidance is enabled).
CF	5	r	Wake Up and configuration parity flag Provides a flag from the internal configuration and Wake Up parity check of registers 07_H through 10_H (including 10_H) without WA TST and PH bit. This parity check includes the CP bit. If 1_B parity is OK. If 0_B parity is not OK, or after startup or after reset the CP bit is false to indicate a reset of all registers. Thus the CP bit has to be corrected once after startup or a reset.
T	4	r	Test mode If 1_B test mode is enabled. Data in registers 00_H till 05_H are either test results or - after a "ADC restart" - invalid measurement data. If 0_B test mode is disabled, valid measurement data available.
PD3	3	r	Power-down flag 3 If 1_B ADC-conversion of Temp is completed and valid measurement data can be read out. Thus it must be 1_B at readout. If 0_B ADC-conversion of Temp is running and read measurement data are invalid. Any readout with PD3 bit = 0_B should be considered invalid. At startup, this is 0_B until one ADC conversion has been performed. The value then changes to 1_B.
PD0	2	r	Power-down flag 0 If 1_B the ADC conversion of Bx is completed and valid measurement data can be read out. Thus it must be 1_B at readout. If 0_B the ADC conversion of Bx is running and read measurement data are invalid. Any readout with PD0 bit = 0_B should be considered invalid. At startup, this is 0_B until one ADC conversion has been performed. The value then changes to 1_B.
FRM	1:0	r	Frame counter Increments at every updated ADC-conversion, once a X/Y/Z/T or X/Y/Z or X/Y conversion is completed and the new measurement data have been stored in the registers 00_H till 05_H. The microcontroller shall check if bits change in consecutive conversion runs.

Back to TLE493D-W2B6 Bitmap.

Version register

Register name	Address	Reset Value
Ver	16_H	$C9_H$, $D9_H$ or $E9_H$

7	6	5	4	3			0
Reserved		**TYPE**		**HWV**			

Field	Bits	Type	Description
Reserved	7:6		Factory settings
TYPE	5:4	r	Chip feature If 00_B, 10_B or 01_B: device with Wake Up feature.
HWV	3:0	r	Hardware revision If 9_H it is the B21 design step.

Back to TLE493D-W2B6 Bitmap.

2 I^2C Interface

The TLE493D-W2B6 uses Inter-Integrated Circuit (I^2C) as the communication interface with the microcontroller.

The I^2C interface has three main functions:

- Sensor configuration.
- Transmit measurement data.
- Interrupt handling.

This sensor provides two I^2C read protocols:

- 16-bit read frame (µC is driving data), so called 2-byte read command.
- 8-bit read frame (µC is driving data), so called 1-byte read command.

2.1 I^2C protocol description

The TLE493D-W2B6 provides one I^2C write protocol, based on 2 bytes and two I^2C read protocols. Default is the 2-byte read protocol. With the PR bit it can be selected, if the 1-byte read protocol or the 2-byte read protocol is used.

2.1.1 General description

- The interface conforms to the I^2C fast mode specification (400kBit/sec max.), but can be driven faster according to the data sheet.
- The TLE493D-W2B6 does not support "repeated starts". Each addressing requires a start condition.
- The interface can be accessed in any power mode.
- The data transmission order is Most Significant Bit (MSB) first, Least Significant Bit (LSB) last.
- A I^2C communication is always initiated with a start condition and concluded with a stop condition by the master (microcontroller). During a start or stop condition the SCL line must stay "high" and the SDA line must change its state: SDA line falling = start condition and SDA line rising = stop condition.
- Bit transfer occur when the SCL line is "high".
- Each byte is followed by one ACK bit. The ACK bit is always generated by the recipient of each data byte.
  - If no error occurs during the data transfer, the ACK bit will be set to "low".
  - If an error occurs during the data transfer, the ACK bit will be set to "high".

2.1.2 I^2C write command

Write I^2C communication description:

- The purpose of the sensor address is to identify the sensor with which communication should occur. The sensor address byte is required independently of the number of sensors connected to the microcontroller.
- The register address identifies the register in the bitmap (according to Figure 1) with which the first data byte will be written.
- Data bytes are transmitted as long as the SCL line generates pulses. Each additional data byte increments the register address until the stop condition occurs.
- Bytes transmitted beyond the register address frame are ignored and the corresponding ACK bit is sent "high", indicating an error.

The I^2C write communication frame consists of:

- The start condition.
- The sensor address, according to Table 4.
- Write command bit = "low" (read = "high").
- Acknowledge ACK.
- Trigger bits, according to Table 6.
- The register address, according to Figure 1.
- Acknowledge ACK.
- Writing of one or several bytes to the sensor, each byte followed by an acknowledge ACK.
- The stop condition.

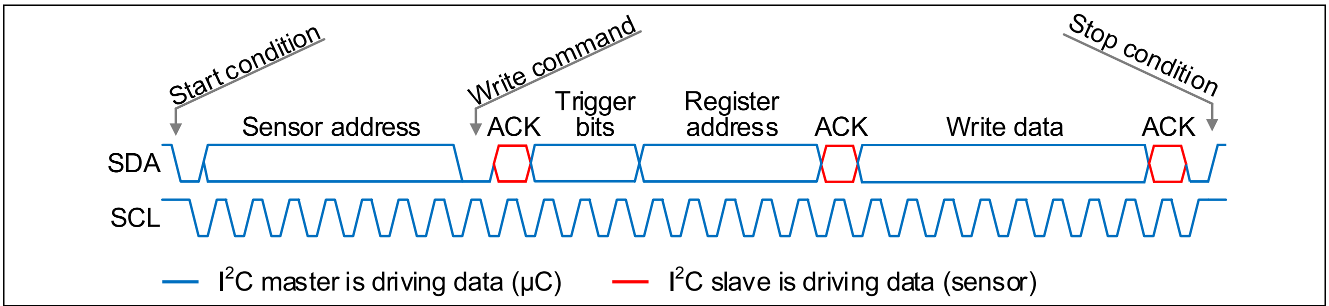

Figure 2 General I^2C write frame format: Write data from microcontroller to sensor

Trigger bits in the I^2C protocol

The trigger bits are used in Power Down Mode. The Power Down Mode is used in the Master Controlled Mode, when no measurement is running. Thus the trigger bits are relevant for the Master Controlled Mode as well.

For a more silent measurement environment it is recommended to separate the measurement and the communication by using the trigger bits = 100_B and communicate only between two measurements without any overlap of measurement and communication.

Table 6 I^2C trigger bits

Trigger-bit 7	Trigger-bit 6	Trigger-bit 5	Trigger command
0_B	0_B	0_B	no ADC trigger
0_B	0_B	1_B	ADC start after I^2C write frame is finished, Figure 4
0_B	1_B	0_B	ADC start before sending first MSB of data registers, Figure 3
0_B	1_B	1_B	no ADC trigger
1_B	0_B	0_B	ADC start after read out of register 06_H is finished, Figure 5
1_B	0_B	1_B	no ADC trigger
1_B	1_B	0_B	no ADC trigger
1_B	1_B	1_B	no ADC trigger

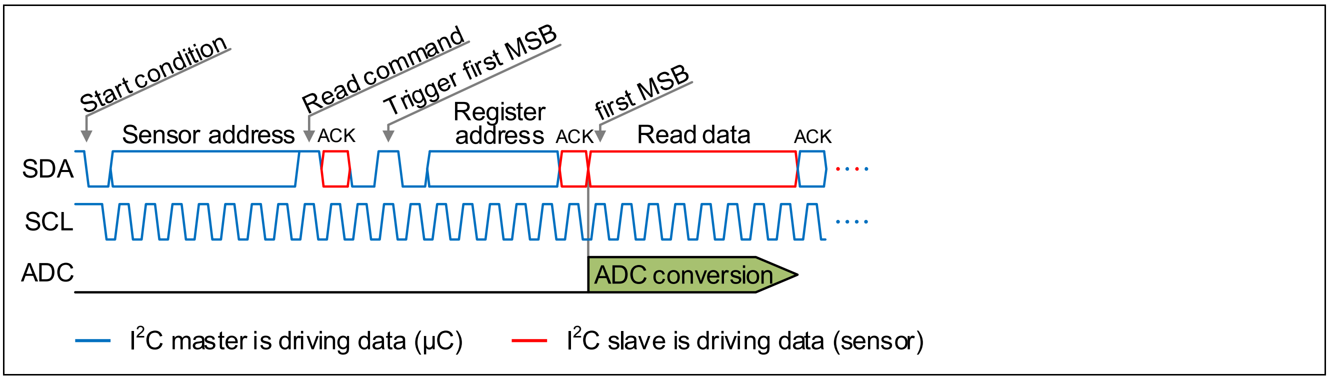

Figure 3 ADC start before sending first MSB of data registers, I^2C trigger bits 010_B.

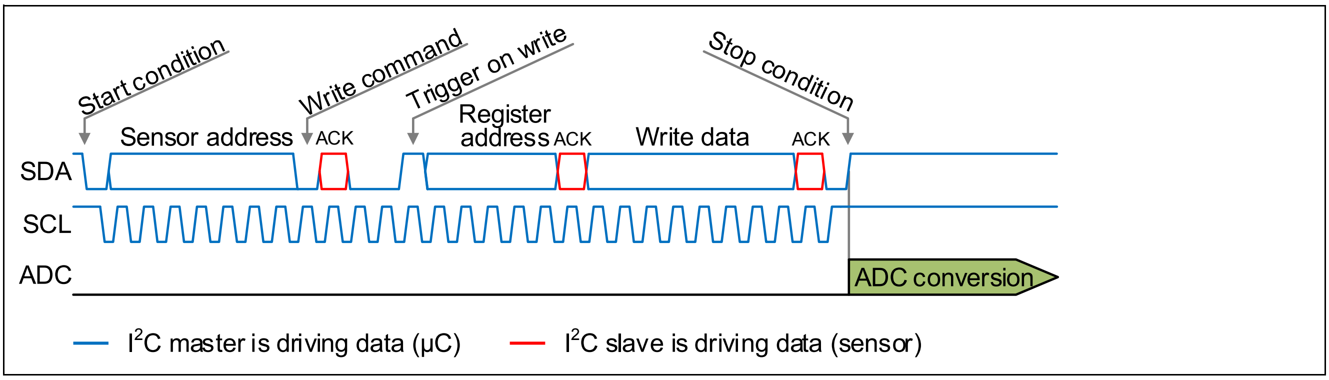

Figure 4 ADC start after I^2C write frame is finished, I^2C trigger bits 001_B.

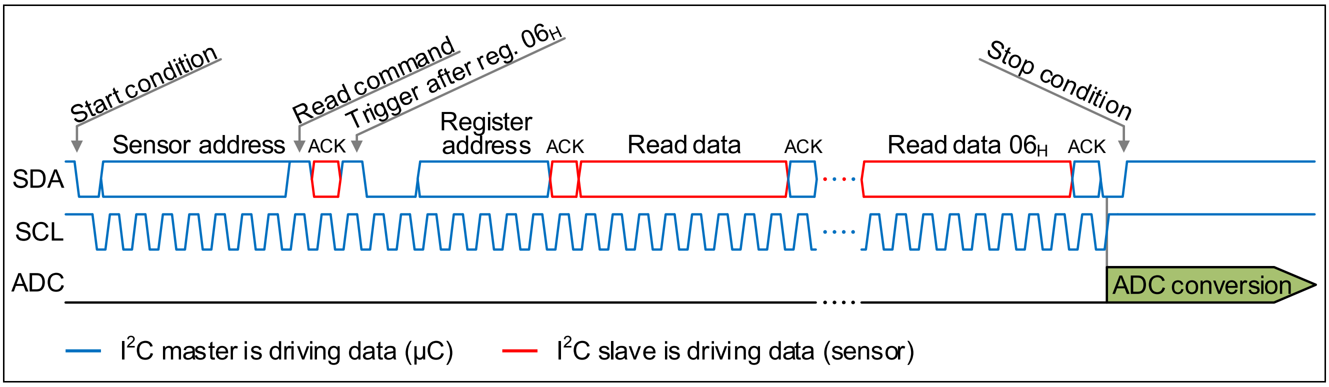

Figure 5 ADC start after read out of register 06_H is finished, I^2C trigger bits 100_B.

Example I^2C write communication

An example of a write communication is provided in Figure 6.

In this example the sensor with the address $6A_H$ / $6B_H$ (see Table 4) should be configured for:

- Master Controlled Mode,
- /INT disabled,
- Clock stretching enabled,
- No trigger of a measurement.
- Other settings should be kept as is.

Implementation:

- The microcontroller generates a start condition.
- Configuration changes can only be performed with a write command. The address for write operation of this sensor is $6A_H = 01101010_B$.
- If the sensor detects no error, the ACK = 0_B is transmitted back to the microcontroller.
- No measurement is performed if the trigger bits = 000_B.
- The register to change the required settings is 11_H according the bitmap Figure 1 = 10001_B.
- If the sensor detects no error, the ACK = 0_B is transmitted back to the microcontroller.
- The parity bit "FP" is the odd parity of the registers 11_H and 13_H (bits 7:5), see FP register, thus it is not possible to quantify it in this example.
- The sensor address should not be changed, i.e. the sensor address $6A_H$ / $6B_H$ should be kept. Thus the IICadr bits = 00_B, see IICadr registers.
- The 2-byte protocol should be kept as is. Thus the PR bit = 0_B.
- In order to enable clock stretching and disable /INT the CA bit must be set to 0_B and the INT bit must be set to 1_B (see Table 5).
- To use the Master Controlled Mode the MODE bits must be set to 01_B.
- If the sensor detects no error the ACK = 0_B is transmitted back to the microcontroller.
- The microcontroller generates the stop condition.

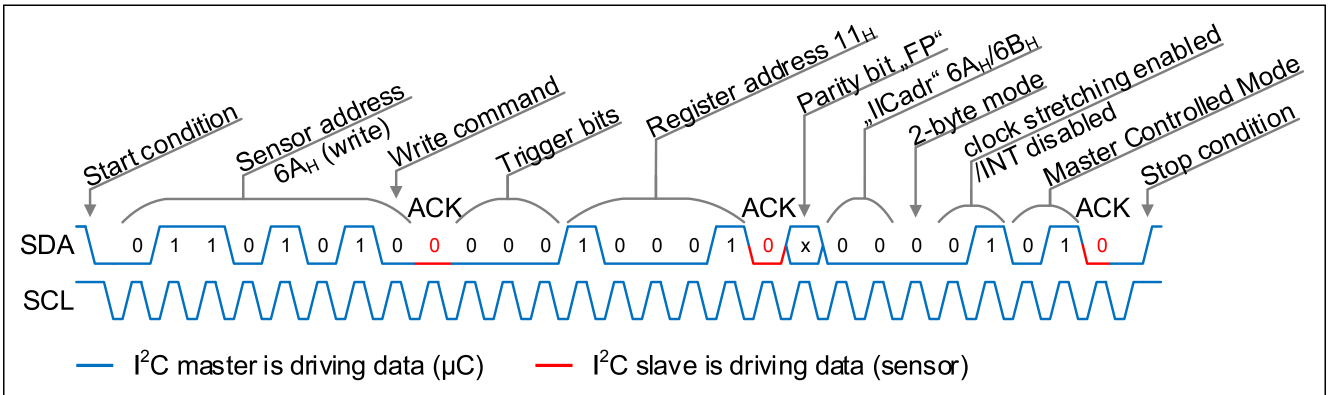

Figure 6 Example I^2C frame format 2-byte: Write data from microcontroller to sensor

2.1.3 I^2C read commands

Read I^2C communication description:

- The purpose of the sensor address is to identify the sensor with which communication should occur. The sensor address byte is required independently of the number of sensors connected to the microcontroller.
- Only available in the 2-byte read command: The register address identifies the register in the bitmap (according Figure 1) from which the first data byte will be read.
  In the 1-byte read command the read out starts always at the register address 00_H.
- As many data bytes will be transferred as long as pulses are generated by the SCL line. Each additional data byte increments the register address. Until the stop condition occurs.
- If bytes are read beyond the register address frame the sensor keeps the SDA = 1_B.
- If the microcontroller reads data and does not acknowledge the sensor data (ACK = 1_B) the sensor keeps the SDA = 1_B until the next stop condition.

2.1.3.1 2-byte read command

The I^2C read communication frame consists of:

- The start condition.
- The sensor address, according to Table 4.
- Read command bit = “high” (write = “low”).
- Acknowledge ACK.
- Trigger bits, according to Table 6.
- The register address, according to Figure 1.
- Acknowledge ACK.
- Reading of one or several bytes from the sensor, each byte followed by an acknowledge ACK.
- The stop condition.

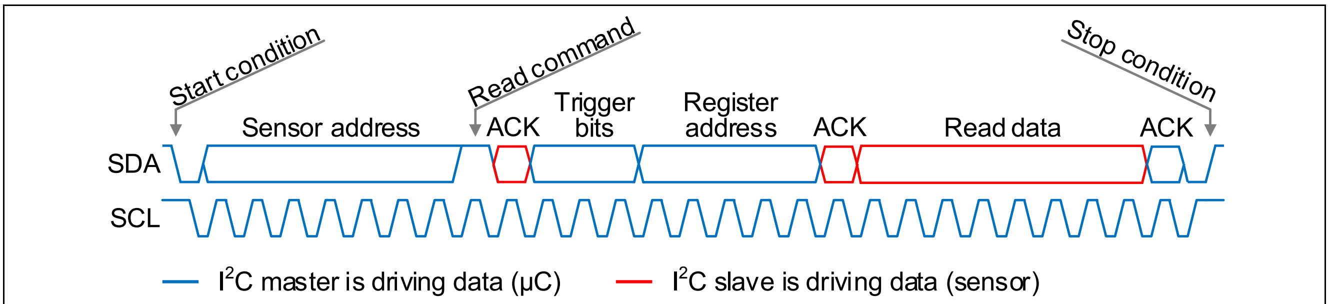

Figure 7 General I^2C frame format 2-byte: Read data from sensor to microcontroller

2.1.3.2 1-byte read command

The 1-byte read mode can be entered, by configuring the PR bit with an write communication. E.g. with the write cycle:

- start condition
- $6A_H$ (sensor address)
- 11_H (register address)
- $XXX1\ XXXX_B$ (PR bit = 1_B)
- stop condition

The I^2C communication frame consists of:

- The start condition.
- The sensor address, according to Table 4.
- Read command bit = “high” (write = “low”).
- Acknowledge ACK.
- Reading of one or several bytes from the sensor, each byte followed by an acknowledge ACK.
- The stop condition.

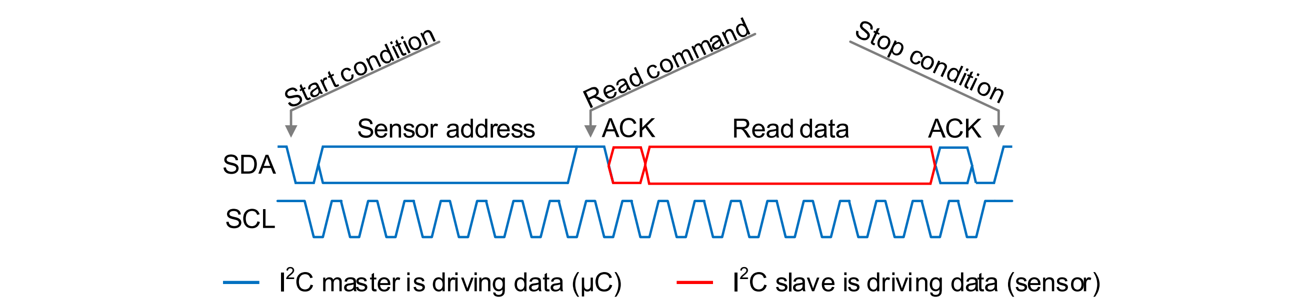

Figure 8 General I^2C frame format 1-byte: Read data from sensor to microcontroller

Example I^2C 1-byte read communication

An example of a read communication is provided in Figure 9.

In this example, the sensor with the address $F0_H$ / $F1_H$ (see Table 4) should read out the measurement values, registers 00_H - 05_H and the diagnostic register 06_H:

Implementation:

- The microcontroller generates a start condition.
- The address for read operation of this sensor is $F1_H = 11110001_B$. This address value must be transmitted by the microcontroller to the sensor.
- If the sensor detects no error, the ACK = 0_B is transmitted back to the microcontroller.
- The microcontroller must go on clocking the SCL line.
- The sensor transmits 8 data bits of register 00_H to the microcontroller.
- If the microcontroller detects no error the ACK = 0_B is transmitted back to the sensor.
- The microcontroller must go on clocking the SCL line.
- The sensor transmits 8 data bits of register 01_H to the microcontroller.
- ...
- After transmitting the register 06_H the microcontroller transmits a ACK.
- The microcontroller generates the stop condition.

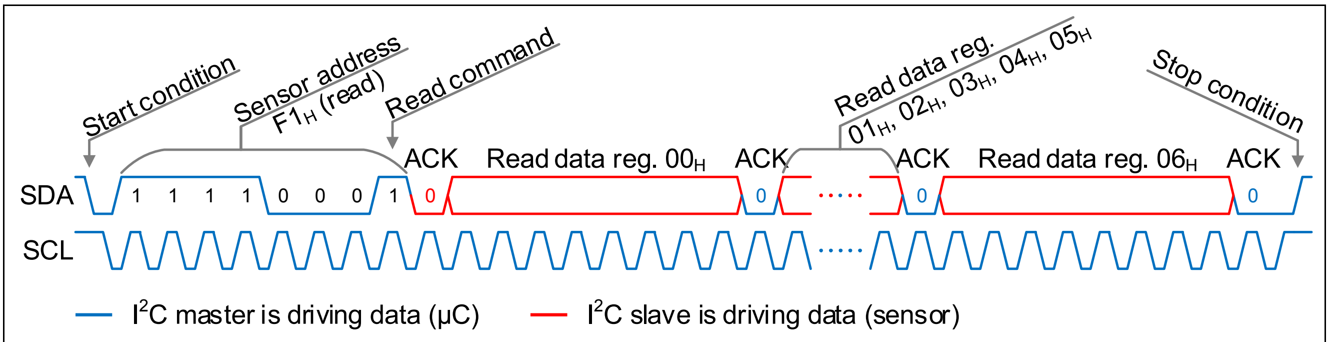

Figure 9 Example I^2C frame format 1-byte: Read data from sensor to microcontroller

2.2 Collision avoidance and clock stretching

Using the configuration bits CA and INT, collision avoidance and clock stretching can be configured. An overview is given in Table 5. An example without collision avoidance and clock stretching is shown in Figure 10. In this example:

- the sensor interrupt disturbs the I²C clock, causing an additional SCL pulse which shifts the data read out by one bit.
- the data read out starts when the ADC conversion is running.

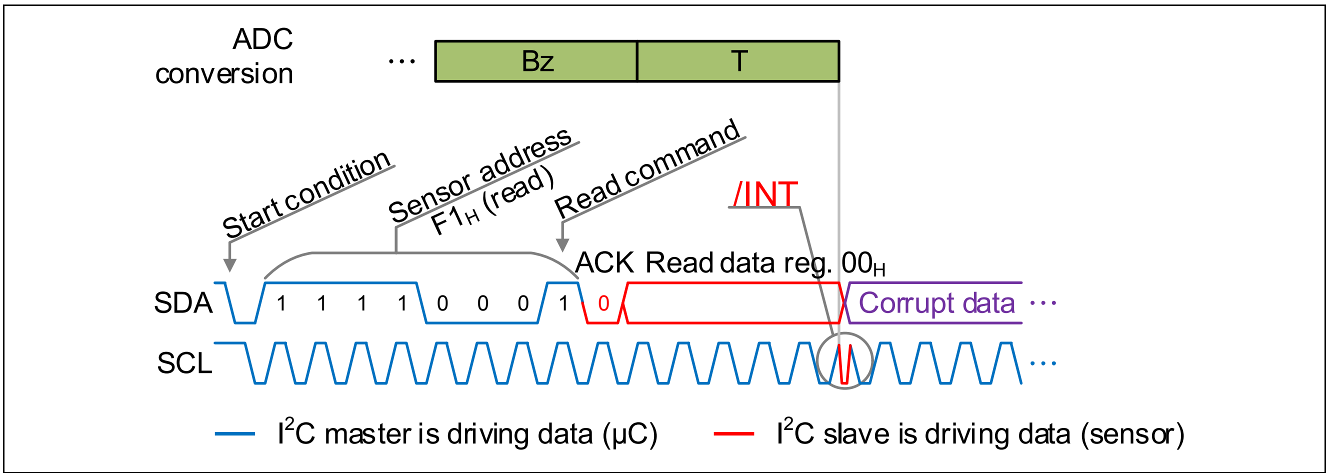

Figure 10 Example without collision avoidance CA bit =1_B and INT bit = 0_B

2.2.1 Collision avoidance (CA bit = 0_B and INT bit = 0_B)

In a bus configuration combined with an activated interrupt signal /INT it must be assured, that during any communication no interrupt /INT occurs. With collision avoidance enabled, the sensor monitors for any start/stop condition, even if it does not detect a valid bus address. The interrupt signal /INT is omitted whenever a start condition is detected, as shown in Figure 11, in contrast to Figure 10. Only after a stop condition is detected, the interrupt signal /INT is generated by the sensor.

It is strongly recommended to use the collision avoidance feature whenever the interrupt signal /INT is used.

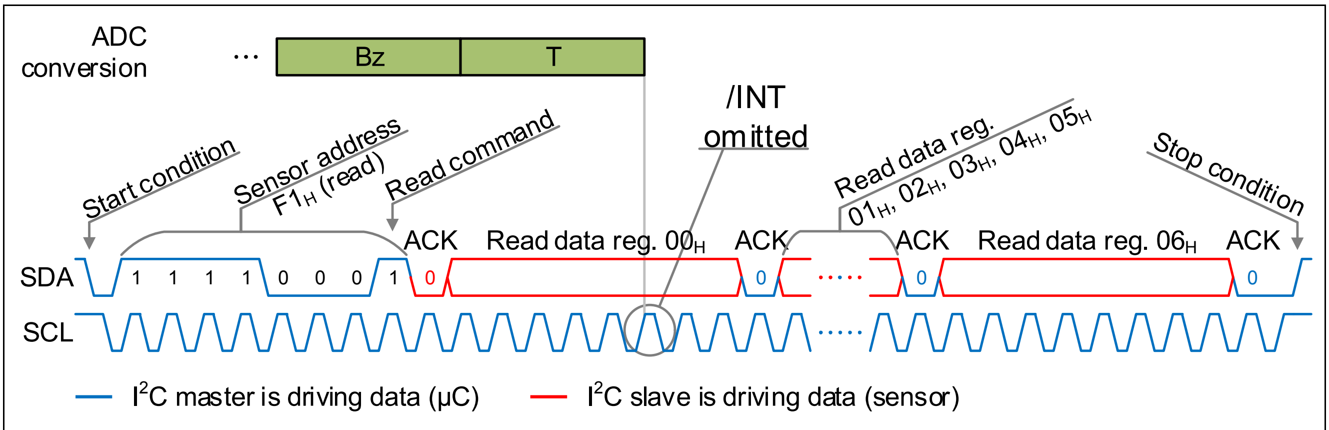

Figure 11 Example with collision avoidance CA bit =0_B and INT bit = 0_B

2.2.2 Clock stretching (CA bit = 0_B and INT bit = 1_B)

With the clock stretching feature, the data read out starts after the ADC conversion is finished. Thus it can be avoided that during an ADC conversion old or corrupted measurement results are read out, which may occur when the ADC is writing to a register while this is being read out by the microcontroller. The clock stretching feature is shown in Figure 12 in combination with a 1-byte read command. Clock stretching can also be used with a 2-byte read command.

The sensor pulls the SCL line to low during the following situation:

- An ADC conversion is in progress.
- The sensor is addressed for register read (writes are never affected by clock stretching).
- The sensor is about to transmit the valid ACK in response to the I²C addressing of the microcontroller.

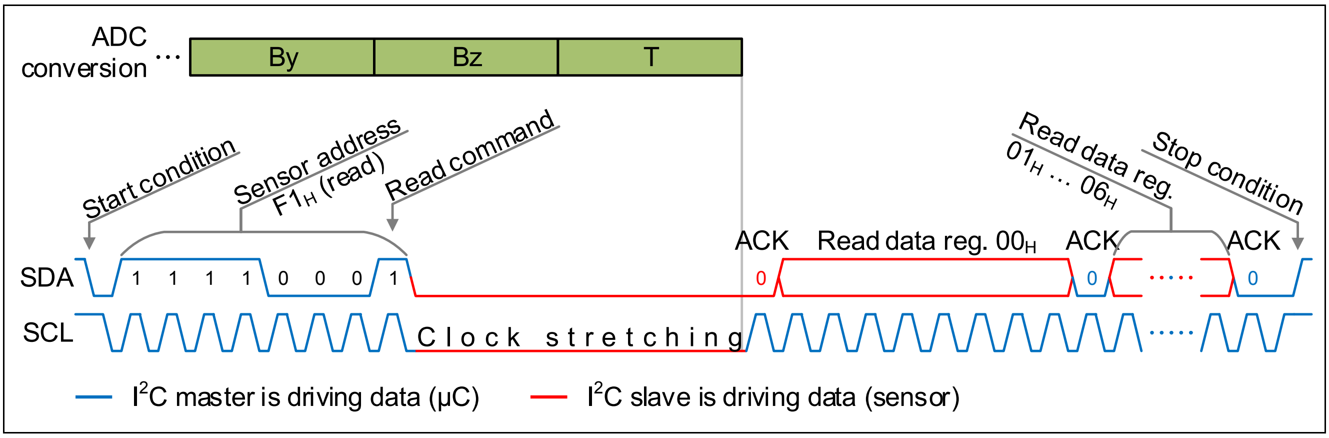

Figure 12 Example with clock stretching CA bit =0_B and INT bit = 1_B

2.3 Sensor reset by I²C

If the microcontroller is reset, the communication with the sensor may be corrupted, possibly causing the sensor to enter an incorrect state. The sensor can be reset via the I²C interface by sending the following command sequence from the microcontroller to the sensor:

- Start condition,
- sending FF_H,
- stop condition.
- Start condition,
- sending FF_H,
- stop condition.
- Start condition,
- sending 00_H,
- stop condition.
- Start condition,
- sending 00_H,
- stop condition.
- 30µs delay.

After a reset, the sensor must be reconfigured to the desired settings.

The reset sequence uses twice the identical data to assure a proper reset, even when an unexpected /INT pulse occurs.

Spikes can be interpreted as bus signals causing an action. E.g. when the collision avoidance feature is active and if the SDA line spikes together with SCL line this could be interpreted as start condition, blocking further /INT pulses until a stop condition appears on the bus. In such a case the sensor must be reset in order to initialize it. If the sensor does not respond after the reset, it must be considered defective.

Such spikes may occur as the sensor powers up. Because of this we recommend to using the reset sequence after each power up before configuring the sensor.

If the microcontroller resets during an ongoing I²C communication, the SDA line could get stuck low. This would block the I²C bus and is a well-known limitation of the I²C interface. To recover from this situation please use the reset sequence described in this chapter.

2.4 Sensor Initialization and Readout example

To ensure that both the microcontroller and the sensor are synchronized and properly initialized, it is recommended to apply the I^2C reset and upload the fuse and Wake Up register settings each time the microcontroller is reset, see Figure 13.

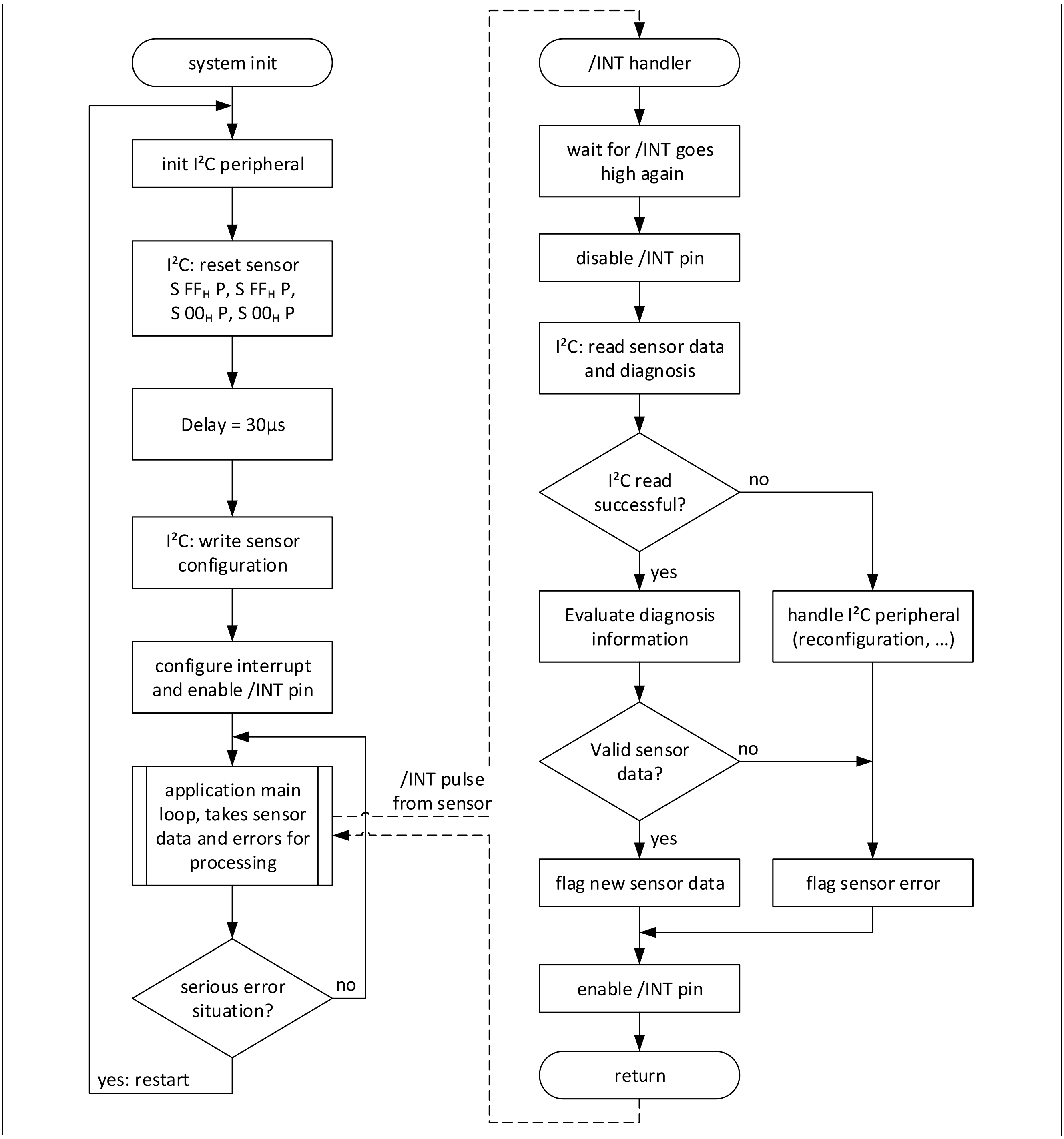

Figure 13 Microcontroller software flowchart for TLE493D-W2B6

2.5 Loss of V_{DD} impact on I^2C bus

If the SDA or SCL line is pulled "low" and the sensor is disconnected from the V_{DD} supply line, the affected I^2C line will most likely get a stuck in the Low state and will interfere with the communication on the bus.

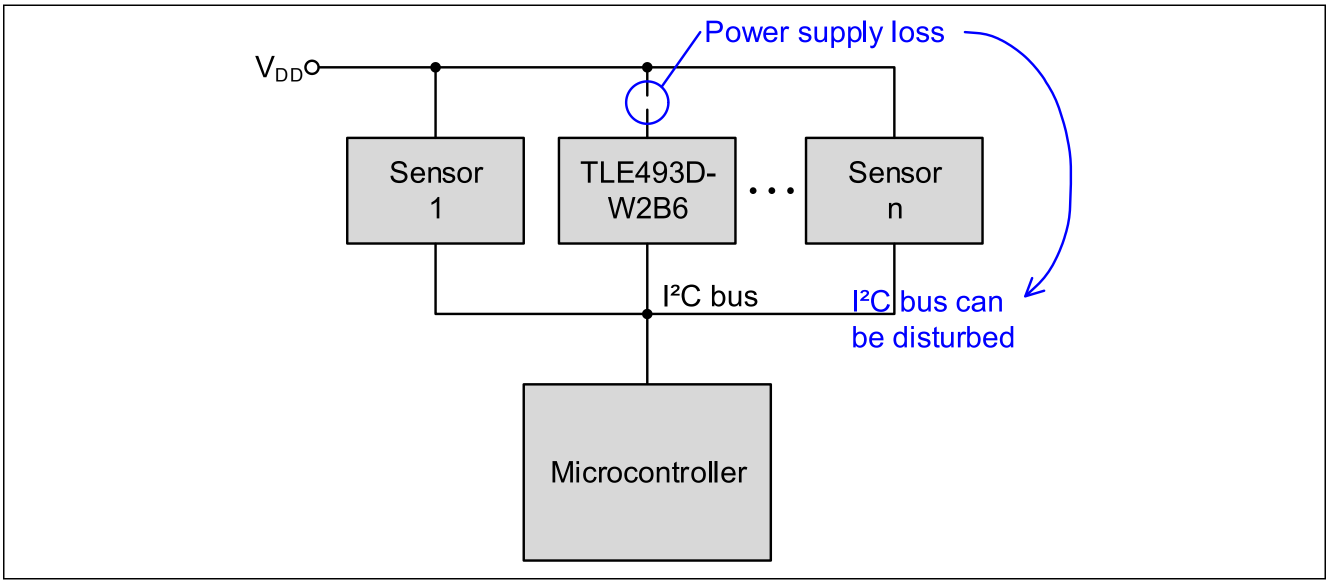

Figure 14 Example of I^2C bus and a TLE493D-W2B6 with disconnected V_{DD}

When V_{DD} is pulled to GND the SDA and SCL line will not disturb the bus.

3 Wake Up mode

The Wake Up mode (or short WU mode) is intended to be used together with the automated sensor modes (e.g. Low Power mode or Fast mode). In principle, it works with the Master Controlled mode as well, but it might not really be useful there because a controlled trigger usually implies the need to acquire a new measurement.

This WU mode can be used to allow the sensor to continue making magnetic field measurements while the µC is in the power-down state, which means the microcontroller will only consume power and access the sensor if relevant measurement data is available. This can be done either by using static thresholds (e.g. for applications where only movements of magnets away from a default position are relevant) or by using dynamic thresholds (where any movement over a specific uncertainty limit should be detected once). The figure below illustrates these two cases.

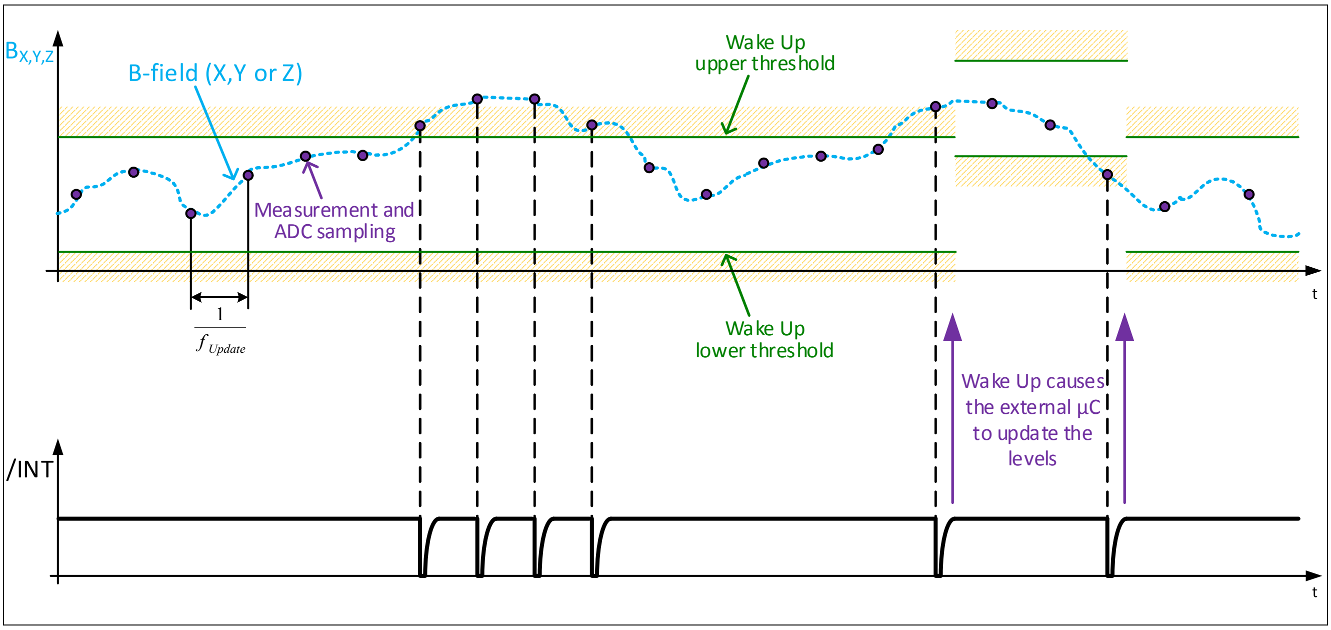

Figure 15 Static or Dynamic Wake Up Threshold Operation of the TLE493D-W2B6

This dynamic WU mode operation offers another option which is particularly useful in Fast mode with limited I²C bus capabilities and/or low bit rates. In this case, the WU mode can act as a "data filter" to reduce the bus load by preventing sensor data from being read that does not change significantly. So due to an interrupt, the new WU levels are adapted to the actual value read (for each X, Y, Z channel individually). This provides low latencies for detecting changes but reduces interrupts caused by similar values. If the collision avoidance feature is also used, the readout may take even longer than one conversion time (but this readout speed adds to the overall signal latency as well). As the thresholds also need to be set, a complete data read and set of new WU thresholds is not even feasible with the fastest specified bit rate within one sensor sample time in Fast mode.

The next figure illustrates this more clearly:

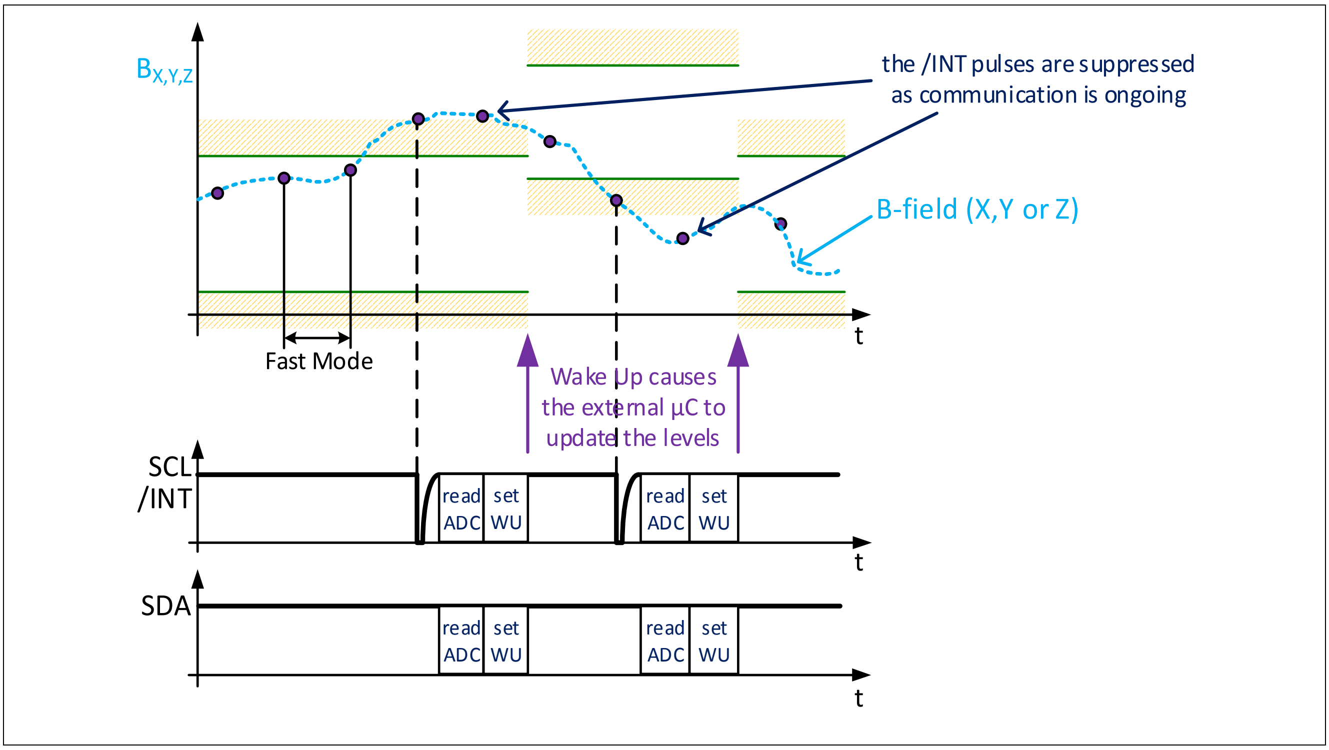

Figure 16 Dynamic Wake Up Threshold Operation of the TLE493D-W2B6 for Bandwidth Reduction

To sum this up, we can state that this dynamic WU mode operation together with the Fast mode set allows detecting and reading significant value changes with low latency, even if the bit rate of the I²C cannot be set fast enough to read the data for each set of sensor data generated.

3.1 Wake Up activation

The Wake Up function can be activated with the WU bit and by modifying at least one of the Wake Up threshold registers of address 07_H to $0F_H$, see Chapter 1.2.3.

Please note that the Wake Up registers cover bit 11 to bit 1. Bit 0 is not accessible, but internally set with 0_B to get a 12-bit value, for comparison with the 12-bit magnetic field value registers Bx, By and Bz.

3.2 Wake Up constraints

The Wake Up threshold range disabling /INT pulses between upper threshold and lower threshold is limited to a window of the half output range.

This window itself can be moved inside the full output range, as illustrated in Figure 17.

Equation (3.1)

$$\text{„}\textit{Wake Up upper threshold}\text{“}_D > \text{„}\textit{Wake Up lower threshold}\text{“}_D$$

Equation (3.2)

$$\text{„}\textit{Wake Up upper threshold}\text{“}_D - \text{„}\textit{Wake Up lower threshold}\text{“}_D < 2048_D LSB_{12}$$

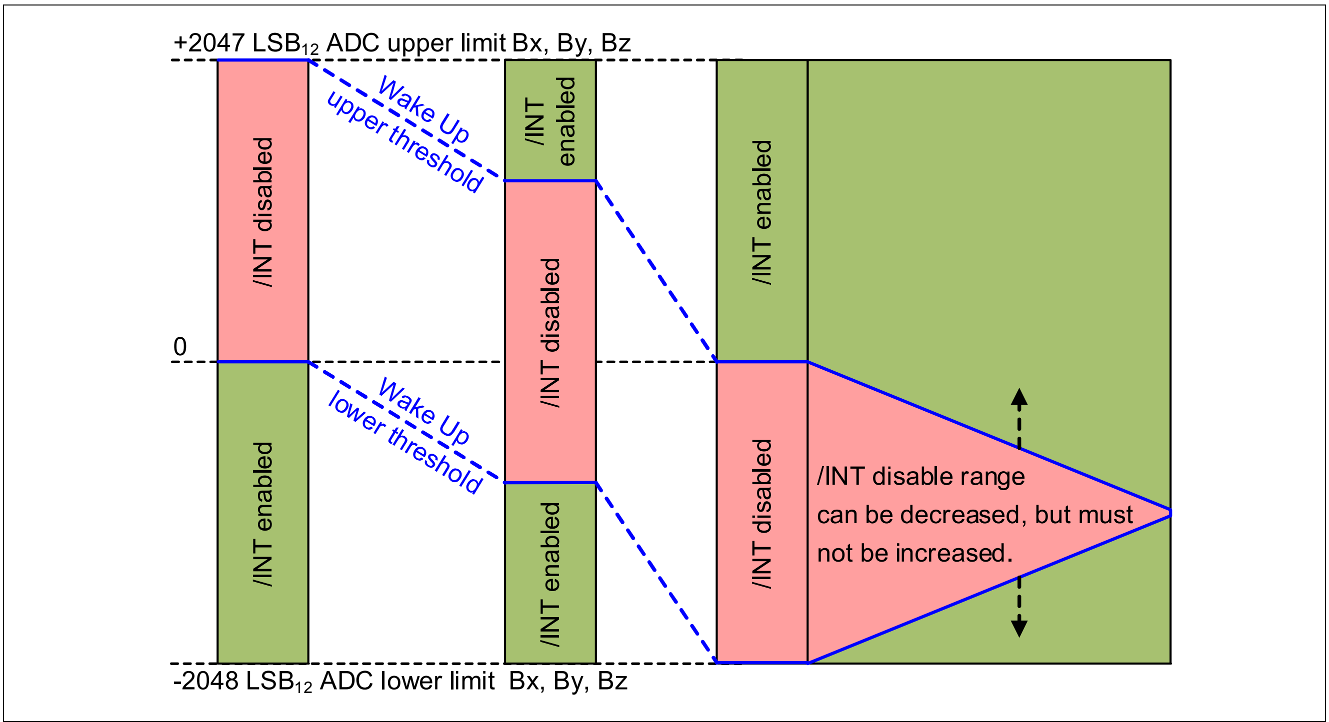

Figure 17 Wake Up enable and disable range examples

3.3 Wake Up in combination with the angular mode

In angular mode, see DT and AM bit, the

- “Wake Up Y upper threshold” must be written to the registers $0C_H$ and $0F_H$ (5 ... 3) (ZH in Figure 1).
- “Wake Up Y lower threshold” must be written to the registers $0B_H$ and $0F_H$ (3 ... 1) (ZL in Figure 1).

4 Diagnostic and tests

The sensor TLE493D-W2B6 provides diagnostic functions and test functions:

- Diagnostic functions Chapter 4.1:
  These functions are running in the background, providing results, which can be checked by the microcontroller for the verification of the measurement results.
- Test functions Chapter 4.2:
  These functions are only executed by the sensor following a request by the microcontroller. The test functions provides test values instead of measurement values, which can be used to check if the sensor is working properly.

4.1 Diagnostic functions

To ensure the integrity of received data the following diagnostic functions are available.

4.1.1 Parity bits and parity flags

Parity bits:

- FP (mode parity bit)
- CP (Wake Up and configuration parity bit)
- P (bus parity bit)

Parity flags:

- FF (mode parity flag)
- CF (Wake Up and configuration parity flag)

4.1.2 Test mode

The device is in test mode, this is indicated by the T register (Diag register 06_H bit 4).

4.1.3 Power-down flags

During measurements and during ADC conversion, the sensor monitors if the supply voltage is correct and if the conversion is finished. This is indicated by the PD3 and PD0 registers.

4.1.4 Frame Counter

The frame counter FRM registers is incremented by one when a conversion is completed.

4.1.5 Device address

The TLE493D-W2B6 can be ordered with different default addresses. This device address can be read out with the IICadr registers.

4.2 Test functions

The TLE493D-W2B6 includes three test functions which can be activated by the microcontroller, using the TST registers in combination with the PH registers:

- Vhall/Vext test: checks the whole signal path from sensor to microcontroller Chapter 4.2.1.
- Spintest: checks all Spin-switches, the Hall-offset and the ADC-offset Chapter 4.2.2.
- SAT-test: checks the whole digital path from sensor to microcontroller Chapter 4.2.3.

4.2.1 Vhall/Vext test mode

This test checks the whole signal path, including the Hall plates, Hall biasing, multiplexer, ADC, data registers, oscillator, power management unit, interface, and the bandgap reference voltage. It also detects whether any Hall switch for the spinning (also known as chopping) is open or short.

4.2.1.1 Test description

Instead of measuring the actual Hall voltages on the probe (which depend on the external magnetic field), a measurement cycle is performed where a voltage drop across the Hall probes is measured. For the temperature sensor, an external voltage (via the V_{DD} pin) is connected.

As the voltage drop across the Hall probes and the external voltage is known, any unexpected output would detect a malfunctioning of the internal Hall biasing or the signal path.

This test should be executed in module production test first. The values generated in this first test should be compared, if inside the limits listed in Table 7 and stored on module level. During module life time this stored values should be compared with additional life time tests and compared, if the values are inside the limits listed in Table 7.

4.2.1.2 Test implementation

The test is performed as described below:

- Set the TST registers according to Vhall/Vext test.
- Trigger a new measurement.
- Read the value of Bx, By, Bz and Temp.

Vhall test:

- Check that Bx, By, Bz and T have values inside the limits of Table 7.
- Testing one voltage reference is sufficient to cover the Vhall test.

Vext test:

- Make the microcontroller aware of the V_{DD}-pin voltage.
- Convert the Temp registers (11 ... 2) to Vext (11 ... 0) by multiplying the 10-bit Temp registers by 4_D.
- Check that the Vext value corresponds to the values listed in Table 7.

After the test:

- Continue with another test or leave the test mode by setting the TST registers accordingly.

Timing

- Typ. 0.5 ms are required for this implementation at an I^{2}C interface baud rate of 400 kbit/s.
- Typ. 0.3 ms are required for this implementation at an I^{2}C interface baud rate of 1 Mbit/s.

4.2.1.3 Test reference values

The test limits are different for production and life time. Both is shown in Table 7 and illustrated in Figure 18.

Table 7 Vhall/Vext diagnostic limits TLE493D-W2B6

Diagnostic test	Module production test. Checked and stored for product life time				Temperature and lifetime drift of stored product values		
	Unit	min.	typ.	max.	Unit	min.	max.
Vhall X @ 3.3V	LSB_{12}	400	630	900	%	-20	+20
Vhall Y @ 3.3V	LSB_{12}	400	630	900	%	-20	+20
Vhall Z @ 3.3V	LSB_{12}	500	830	1200	%	-30	+30
Vext @ 3.3V	LSB_{12}	1100	1370	1650	%	-15	+15

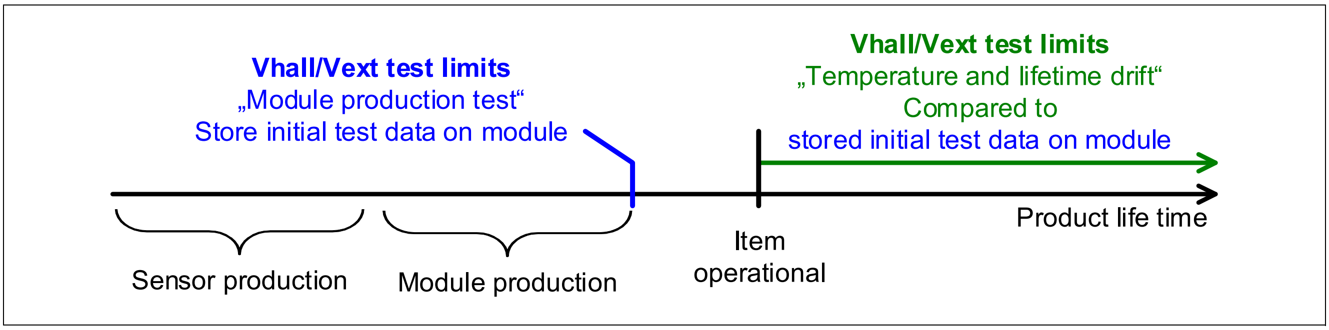

Figure 18 Vhall/Vext diagnostic limits vs. lifetime

4.2.2 Spintest mode

This test checks the correct spinning (also known as chopping) of all four phases of a Hall probe for the three channels Bx, By and Bz of the sensor and that the Hall probes offset and the ADC offset is within specified limits. Also offers diagnostic coverage for the multiplexer, ADC, oscillator and power management unit. Limited coverage for the biasing, registers and interface as well.

4.2.2.1 Test description

In a magnetic measurement run, the result of the four spins is:

Equation (4.1)

$$4V_H + (2V_{Oh} - 2V_{Oh} + 2V_{Oa} - 2V_{Oa}) = 4V_H$$

- V_H is the voltage at the Hall probes
- V_{Oh} is the voltage offset at the Hall probes
- V_{Oa} is the voltage offset at the ADC

By spinning the measurement four times at the Hall probes, the Hall offset and the ADC offset are eliminated in magnetic measurements. The Spintest can be used to measure these offsets.
The PH register selects, which Hall probe is measured by the Spintest, see Table 3. This Hall probe is then measured four times, and every time another spinning phase is disregarded, see Figure 19. Thus, four results are stored in the registers Bx (11 ... 0), By (11 ... 0), Bz (11 ... 0) and T (11 ... 2).

The ADC offset can be measured with PH = 11_B. In this Spintest, the ADC compares the temperature sensor with an internal reference voltage. During the test, the temperature and the reference are swapped (setting1 and setting2). The offset of the ADC can be calculated according to Equation (4.5). The temperature, including the offset, can be calculated according to Equation (4.4).

Each Spintest Bx, By, Bz and T has the same duration as a measurement cycle consisting of a Bx, By, Bz and T measurement.

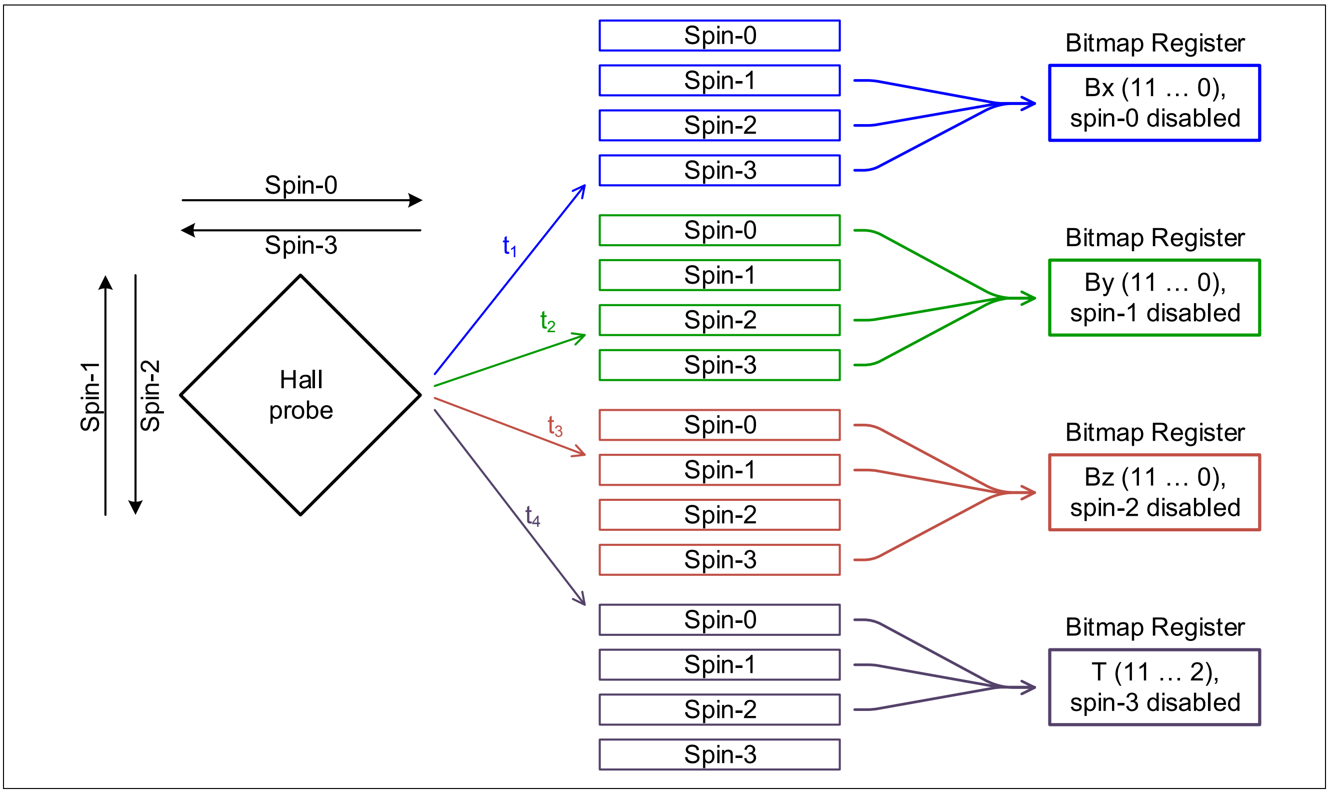

Figure 19 Spintest concept of one Hall probe, please see also Table 3

Disabling the first or the forth phase leads to the following result:

Equation (4.2)

$$3V_H + (1V_{Oh} - 2V_{Oh} + 1V_{Oa} - 2V_{Oa}) = 3V_H - 1V_{Oh} - 1V_{Oa}$$

Disabling the second or the third phase leads to the following result:

Equation (4.3)

$$3V_H + (2V_{Oh} - 1V_{Oh} + 2V_{Oa} - 1V_{Oa}) = 3V_H + 1V_{Oh} + 1V_{Oa}$$

Spintest magnetic field calculation:

Equation (4.4)

$$B_{X,Y,Z(Spin)} = \frac{B_X(11 \dots 0) + B_Y(11 \dots 0) + B_Z(11 \dots 0) + 4 \cdot Temp(11 \dots 2)}{3}$$

Spintest offset calculation:

Equation (4.5)

$$V_{Oh} = \frac{B_X(11 \dots 0) + 4 \cdot Temp(11 \dots 2) - B_Y(11 \dots 0) - B_Z(11 \dots 0)}{4} + 512$$

4.2.2.2 Test implementation

The test is performed as described below:

- Set the TST registers according "no test".
- Read and store the values of Bx, By and Bz of any magnetic measurement.
- Set the TST registers according Spintest.
- Set the PH registers to 00_B to test the Bx Hall probe.
- Trigger a new measurement.
- Read the value of Bx, By, Bz and Temp.
  Please note: The Temp (11 ... 2) needs to be multiplied by 4_D to get the 12-bit Temp-value.
- Calculate the offset with Equation (4.5) and check against the values listed in Table 8.
- For a proper test result the magnetic field must be stable during the test. This can be checked by calculating the magnetic field from the Spintest with Equation (4.4) and comparing the result with the latest "no test" measurement. If a difference in value is identified, the test can be run again to discard that the fault is due to a change of the magnetic field (instead of a chip fault).
- Repeat the last five steps (PH setting, measurement trigger, value read out, ...) with PH registers incrementing to 01_B, 10_B and 11_B, according Table 3.

After the test:

- Continue with another test or leave the test mode by setting the TST registers accordingly.

Timing

- Typ. 2.3 ms are required for this implementation at an I^2C interface baud rate of 400 kbits/s.
- Typ. 1.4 ms are required for this implementation at an I^2C interface baud rate of 1 Mbit/s.

4.2.2.3 Test reference values

The test limits are different for production and life time. Both is shown in Table 8 and illustrated in Figure 20. The spintest should be executed during the module production test first. The offset values (Equation (4.5)) generated in the first test should be compared to make sure that they are inside the limits specified in Table 8, section "Module production test" and stored on module level. During module lifetime these stored values must be compared in an additional Spintest to check if the values are inside the limits listed in Table 8, section "Temperature and lifetime drift".

Table 8 Spintest diagnostic limits TLE493D-W2B6

Diagnostic test	V_{Oh} module production test. Checked and stored for product life time			Temperature and lifetime drift of stored product V_{Oh} values		
	Unit	min.	max.	Unit	min.	max.
Spintest X @ 3.3V	LSB_{12}	-200	+200	LSB_{12}	-130	+130
Spintest Y @ 3.3V	LSB_{12}	-200	+200	LSB_{12}	-130	+130
Spintest Z @ 3.3V	LSB_{12}	-160	+160	LSB_{12}	-60	+60
Spintest T @ 3.3V	LSB_{12}	-160	+160	LSB_{12}	-60	+60

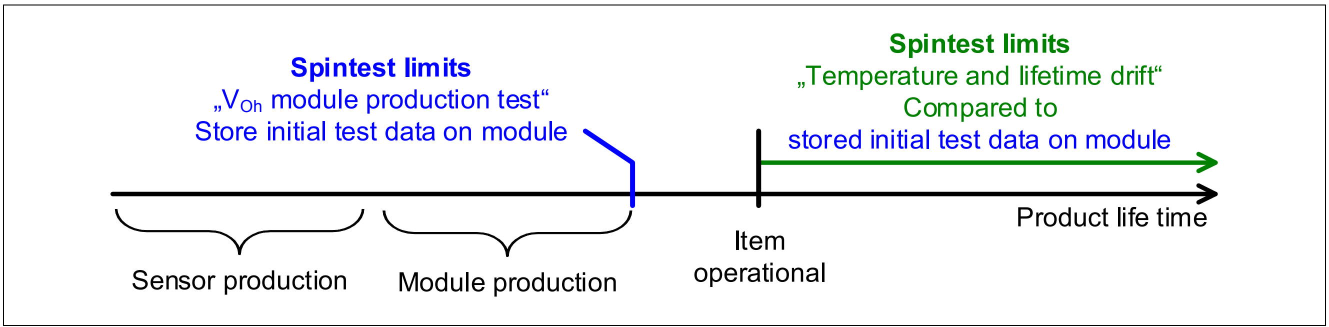

Figure 20 Spintest diagnostic limits vs. lifetime

4.2.3 SAT-test mode

This test checks the whole digital signal path from sensor to microcontroller. This includes the ADC's digital core, the data register, the I^2C interface and the I^2C bus as well.

4.2.3.1 Test description

This test checks the Successive Approximation and Tracking (SAT) mechanism used for the four spin phases of each data channel (Hall probes and temperature sensor).

The results, listed in Table 3 are outside of the specified linear range for Hall values and temperature. Thus, it is possible to easily distinguish between values from the test mode and values from normal operation. An unintended enabling of the test can therefore be identified.

4.2.3.2 Test implementation

The test is performed as described below:

- Set the test register TST accordingly.
- Select one combination of PH and X2 register out of Table 3.
  Please note: One combination is sufficient for a valid SAT-test.
- Trigger a new measurement.
- Read the values of Bx, By, Bz and Temp and compare if they are inside the limits specified inTable 3.

After the test:

- Continue with another test or leave the test mode by setting the TST registers accordingly.

Timing

This test requires one write command with three data bytes and one readout with seven data bytes and the measurement run time. The readouts may take place immediately after a new diagnostic is set and the measurement is triggered.

- Typ. 0.5 ms are required for this implementation at an I^2C interface baud rate of 400 kbit/s.
- Typ. 0.3 ms are required for this implementation at an I^2C interface baud rate of 1 Mbit/s.

4.3 Magnetic measurement implementation

A magnetic measurement can be performed as described below:

- Set the TST registers according “no test”.
- Trigger a measurement.
- Read the value of Bx, By, Bz and Temp.
  Please note: The Temp (11 ... 2) needs to be multiplied by 4_D to get the 12-bit Temp-value.

Timing

- Typ. 0.5 ms are required for this implementation at an I^2C interface baud rate of 400 kbit/s.
- Typ. 0.3 ms are required for this implementation at an I^2C interface baud rate of 1 Mbit/s.

5 Terminology

A	
ACK	Acknowledge
ADC	Analog/Digital Converter
adr	address
E	
EMC	Electromagnetic Compatibility
G	
GND	Ground
I	
ID	IDentification
I^2C (I2C)	Inter-Integrated Circuit
/INT	Interrupt pin, Interrupt signal
L	
LSB	Least Significant Bit
M	
Magnetic field	Magnetic flux density that the sensor measures.
min	minimum
MSB	Most Significant Bit
max	maximum
P	
PCB	Printed Circuit Board
R	
reg	register
S	
SCL	Clock pin
SDA	Data pin
Sensor	Refers to the TLE493D-W2B6 product
Sensor module	Refers to the TLE493D-W2B6 product and all the passive elements in the customer's module
Supply	Refers to the sensor supply pins V_{DD} and GND (the unused pins are assumed to be connected to GND as well).
V	
V_{DD}	Supply voltage
W	
WU	Wake Up
µ	
µC	Microcontroller

6 Revision history

Revision	Date	Changes
Ver. 0.4	2018-04-09	Chapter 4.2.2.2 updated. PRD bit description updated. Table 8 updated. Editorial changes.
Ver. 0.3	2018-03-14	Figure 1 updated CP bit related registers. CP and CF bit description.
Ver. 0.2	2018-03-09	Whole document: Editorial changes. Whole document: “usable-range” (old) replaced with “full-range” (new) and “half-range” (old) replaced with “short-range” (new). Chapter 2 I2C Interface added. Table 1 added. Register Table Power mode, interrupt, address, parity, Temp2 reset values updated, FP bit description updated, PR bit description updated and CA bit description updated. FP bit description updated. Table 4 updated. Table 5: table header updated. Table 8 updated. Chapter 4.2 test timings updated. Figure 19 updated. Chapter 4.2.2 updated. Chapter 4.3 added.
Ver. 0.1	2017-08-29	Initial release.

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2018-04-09
Published by
Infineon Technologies AG
81726 Munich, Germany

Do you have a question about any aspect of this document?
Email: erratum@infineon.com

Document reference